DALLAS SEMICONDUCTOR MAXIM

DS21Q50
Quad E1 Transceiver

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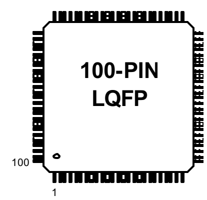
FEATURES

- Four complete E1 (CEPT) PCM-30/ISDN-PRI transceivers
- Long-haul and short-haul line interfaces
- 32-bit or 128-bit crystal-less jitter attenuator
- Frames to FAS, CAS, CCS, and CRC4 formats
- 4MHz/8MHz/16MHz clock synthesizer
- Flexible system clock with automatic source switching on loss of clock source
- Two-frame elastic-store slip buffer on the receive side
- Interleaving PCM bus operation up to 16.384MHz
- Configurable parallel and serial port operation
- Detects and generates remote and AIS alarms
- Fully independent transmit and receive functionality
- Four separate loopback functions
- PRBS generation/detection/error counting
- 3.3V low-power CMOS
- Large counters for bipolar and code violations, CRC4 code word errors, FAS word errors, and E bits
- Eight additional user-configurable output pins
- 100-pin LQFP package (14mm)

ORDERING INFORMATION

DS21Q50L	100-Pin, 14mm LQFP	(0°C to +70°C)
DS21Q50LN	100-Pin, 14mm LQFP	(-40°C to +85°C)



DESCRIPTION

The DS21Q50 E1 Quad Transceiver contains all of the necessary functions for connection to four E1 lines. The onboard clock/data recovery circuitry coverts the AMI/HDB3 E1 waveforms to an NRZ serial stream. The DS21Q50 automatically adjusts to E1 22AWG (0.6mm) twisted-pair cables from 0km to over 2km in length. The device can generate the necessary G.703 waveshapes for both 75O coax and 120O twisted-pair cables. The onboard jitter attenuators (selectable to either 32 bits or 128 bits) can be placed in either the transmit or receive data paths. The framers locate the frame and multiframe boundaries and monitor the data streams for alarms. The device contains a set of internal registers, from which the user can access and control the operation of the unit via the parallel control port or serial port. The device fully meets all of the latest E1 specifications including ITU-T G.703, G.704, G.706, G.823, G.732, and I.431 ETS 300 011, ETS 300 233, and ETS 300 166 as well as CTR12 and CTR4.

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: http://dbserv.maxim-ic.com/errata.cfm.

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3. INTRODUCTION

The DS21Q50 is optimized for high-density termination of E1 lines. Two significant features are included for this type of application: the Interleave Bus Option and a System Clock Synthesizer feature. The Interleave Bus Option allows up to eight E1 data streams to be multiplexed onto a single high-speed PCM bus without additional external logic. The System Clock Synthesizer feature allows any of the E1 lines to be selected as the master source of clock for the system and for all the transmitters. This is also accomplished without the need of external logic. Each of the four transceivers has a clock and data jitter attenuator that can be assigned to either the transmit or receive path. In addition there is a single, undedicated clock jitter attenuator that can be hardware configured as the user needs. Each transceiver also contains a PRBS pattern generator and detector. Figure 21-1 shows a simplified typical application which terminates 8 E1 lines (transmit and receive pairs) and combines the data into a single 16.384MHz PCM bus. The 16.384MHz system clock is derived and phased-locked to one of the eight E1 lines. On the receive side of each port, an elastic store provides logical management of any slip conditions due to the asynchronous relationship of the eight E1 lines. In this application all eight transmitters are timed to the selected E1 line.

4. FUNCTIONAL DESCRIPTION

The analog AMI/HDB3 waveform off of the E1 line is transformer coupled into the RRING and RTIP pins of the DS21Q50. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive framer where the digital serial stream is analyzed to locate the framing/multiframe pattern. The DS21Q50 contains an active filter that reconstructs the analog received signal for the nonlinear losses that occur in transmission. The device has a usable receive sensitivity of 0dB to -43dB, which allows the device to operate on cables over 2km in length. The receive framer locates FAS frame and CRC and CAS multiframe boundaries as well as detects incoming alarms including, carrier loss, loss of synchronization, AIS, and Remote Alarm. If needed, the receive elastic store can be enabled in order to absorb the phase and frequency differences between the recovered E1 data stream and an asynchronous backplane clock which is provided at the SYSCLK input. The clock applied at the SYSCLK input can be either a 2.048MHz/4.096MHz/8.192MHz, or 16.384MHz clock. The transmit framer is independent from the receive in both the clock requirements and characteristics. The transmit formatter will provide the necessary frame/multiframe data overhead for E1 transmission.

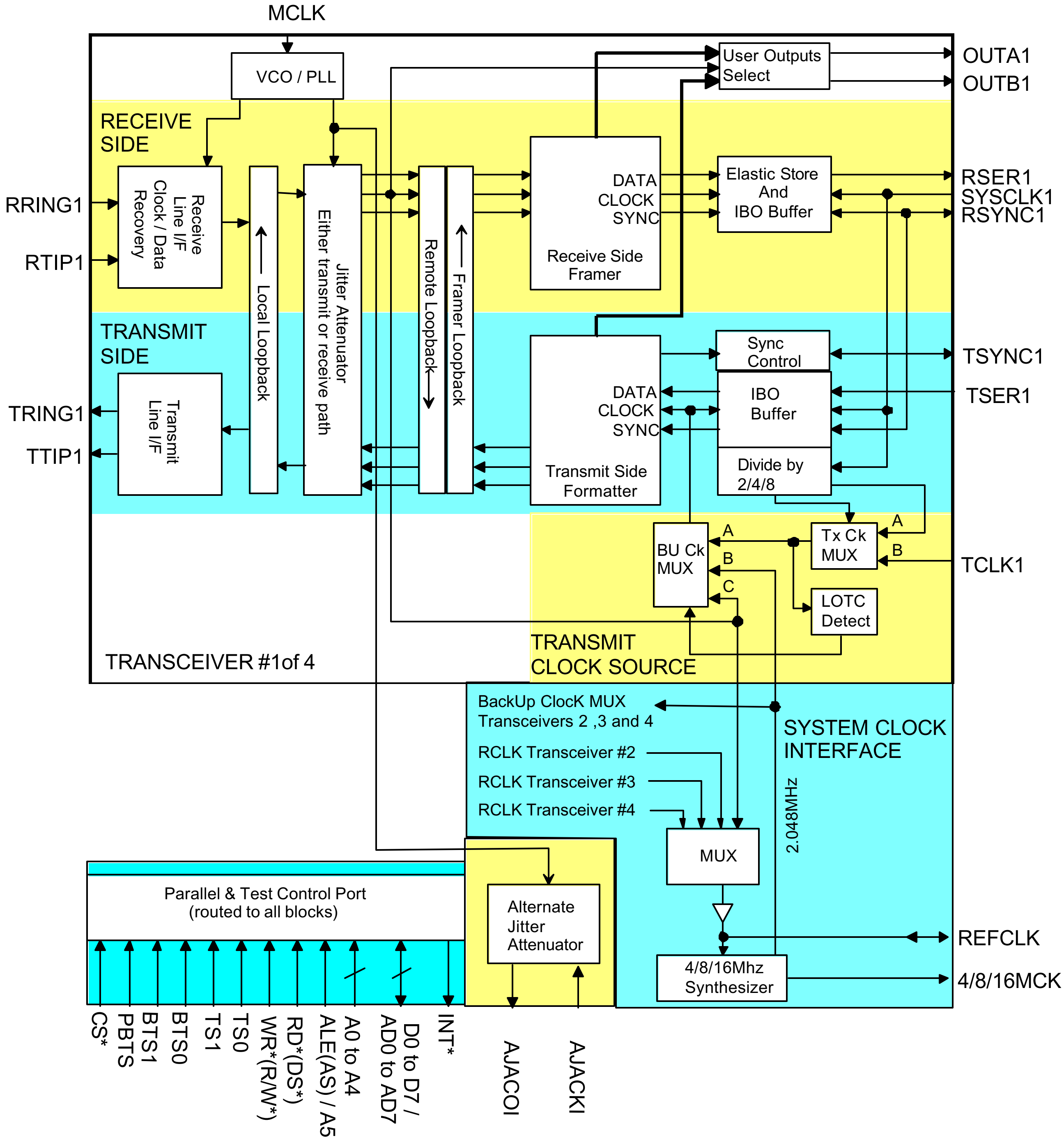
Note: This data sheet assumes a particular nomenclature of the E1 operating environment. In each 125µs frame, there are 32 8-bit timeslots numbered 0 to 31. Timeslot 0 is transmitted first and received first. These 32 timeslots are also referred to as channels with a numbering scheme of 1 to 32. Timeslot 0 is identical to channel 1, timeslot 1 is identical to channel 2, and so on. Each timeslot (or channel) is made up of eight bits that are numbered 1 to 8. Bit number 1, MSB, is transmitted first. Bit number 8, the LSB, is transmitted last. The term “locked” is used to refer to two clock signals that are phase-locked or frequency-locked or derived from a common clock (i.e., a 8.192MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component). Throughout this data sheet, the following abbreviations will be used:

FAS	Frame Alignment Signal
CAS	Channel Associated Signaling
MF	Multiframe
Si	International bits
CRC4	Cyclical Redundancy Check
CCS	Common Channel Signaling
Sa	Additional bits
E-Bit	CRC4 Error Bits
LOC	Loss of Clock
TCLK	This generally refers to the transmit rate clock and can reference an actual input signal to the device (TCLK) or an internally derived signal used for transmission.
RCLK	This generally refers to the recovered network clock and can be a reference to an actual output signal from the device or an internal signal.

4.1 DOCUMENT REVISION HISTORY

1) Initial release for external use, 010500.
2) Update with typographical corrections and clarifications, 110701.

DS21Q50 QUAD TRANSCEIVER Figure 4-1



5. PIN DESCRIPTION

PIN TABLE (By Function) Table 5-1

LQFP PIN	SIGNAL NAME PARALLEL PORT ENABLED	SIGNAL NAME SERIAL PORT ENABLED	TYPE	FUNCTION [Serial Port Mode In Brackets]
71	4/8/16MCK		O	4.096MHz, 8.192MHz, or 16.384 MHz Clock
45	A0	ICES	I	Address Bus Bit 0 / Serial Port [Input Clock Edge Select]
46	A1	OCES	I	Address Bus Bit 1 / Serial Port [Output Clock Edge Select]
47	A2		I	Address Bus Bit 2
48	A3		I	Address Bus Bit 3
49	A4		I	Address Bus Bit 4
70	AJACKI		I	Alternate Jitter Attenuator Clock Input
69	AJACKO		O	Alternate Jitter Attenuator Clock Output
50	ALE(AS)/A5		I	Address Latch Enable /Address Bus Bit 5
96	BTS0			Bus Type Select 0
97	BTS1			Bus Type Select 1
98	CS*		I	Chip Select
19	D0/AD0		I/O	Data Bus Bit0/ Address/Data Bus Bit 0
20	D1/AD1		I/O	Data Bus Bit1/ Address/Data Bus Bit 1
21	D2/AD2		I/O	Data Bus Bit 2/Address/Data Bus Bit2
22	D3/AD3		I/O	Data Bus Bit 3/Address/Data Bus Bit 3
23	D4/AD4		I/O	Data Bus Bit4/Address/Data Bus Bit 4
24	D5/AD5		I/O	Data Bus Bit 5/Address/Data Bus Bit 5
25	D6/AD6		I/O	Data Bus Bit 6/Address/Data Bus Bit 6
44	D7/AD7	SDO	I/O	Data Bus Bit 7/Address/Data Bus Bit 7 [Serial Data Output]
84	DVDD1		–	Digital Positive Supply
59	DVDD2		–	Digital Positive Supply
34	DVDD3		–	Digital Positive Supply
9	DVDD4		–	Digital Positive Supply
83	DVSS1		–	Digital Signal Ground
58	DVSS2		–	Digital Signal Ground
33	DVSS3		–	Digital Signal Ground
8	DVSS4		–	Digital Signal Ground
–	EQVSS1		–	Equalizer Analog Signal Ground
–	EQVSS2		–	Equalizer Analog Signal Ground
–	EQVSS3		–	Equalizer Analog Signal Ground
–	EQVSS4		–	Equalizer Analog Signal Ground
94	INT*		O	Interrupt
73	MCLK		I	Master Clock Input
61	OUTA1		O	User Selectable Output A
36	OUTA2		O	User Selectable Output A
11	OUTA3		O	User Selectable Output A
86	OUTA4		O	User Selectable Output A
60	OUTB1		O	User Selectable Output B
35	OUTB2		O	User Selectable Output B
10	OUTB3		O	User Selectable Output B
85	OUTB4		O	User Selectable Output B
95	PBTS		I	Parallel Bus Type Select
75	RD*(DS*)	SCLK	I	Read Input(Data Strobe) [Serial Port Clock]

72	REFCLK		I/O	Reference Clock
67	RRING1		I	Receive Analog Ring Input
42	RRING2		I	Receive Analog Ring Input
17	RRING3		I	Receive Analog Ring Input
92	RRING4		I	Receive Analog Ring Input
63	RSER1		O	Receive Serial Data
38	RSER2		O	Receive Serial Data
13	RSER3		O	Receive Serial Data
88	RSER4		O	Receive Serial Data
64	RSYNC1		I/O	Receive Sync
39	RSYNC2		I/O	Receive Sync
14	RSYNC3		I/O	Receive Sync
89	RSYNC4		I/O	Receive Sync
66	RTIP1		I	Receive Analog Tip Input
41	RTIP2		I	Receive Analog Tip Input
16	RTIP3		I	Receive Analog Tip Input
91	RTIP4		I	Receive Analog Tip Input
93	RVDD1		–	Receive Analog Positive Supply
68	RVDD2		–	Receive Analog Positive Supply
43	RVDD3		–	Receive Analog Positive Supply
18	RVDD4		–	Receive Analog Positive Supply
90	RVSS1		–	Receive Analog Signal Ground
65	RVSS2		–	Receive Analog Signal Ground
40	RVSS3		–	Receive Analog Signal Ground
15	RVSS4		–	Receive Analog Signal Ground
62	SYSCLK1		I	Transmit/Receive System Clock
37	SYSCLK2		I	Transmit/Receive System Clock
12	SYSCLK3		I	Transmit/Receive System Clock
87	SYSCLK4		I	Transmit/Receive System Clock
80	TCLK1		I	Transmit Clock
55	TCLK2		I	Transmit Clock
30	TCLK3		I	Transmit Clock
5	TCLK4		I	Transmit Clock
79	TRING1		O	Transmit Analog Ring Output
54	TRING2		O	Transmit Analog Ring Output
29	TRING3		O	Transmit Analog Ring Output
4	TRING4		O	Transmit Analog Ring Output
99	TS0		I	Transceiver Select 0
100	TS1		I	Transceiver Select 1
81	TSER1		I	Transmit Serial Data
56	TSER2		I	Transmit Serial Data
31	TSER3		I	Transmit Serial Data
6	TSER4		I	Transmit Serial Data
82	TSYNC1		I/O	Transmit Sync
57	TSYNC2		I/O	Transmit Sync
32	TSYNC3		I/O	Transmit Sync
7	TSYNC4		I/O	Transmit Sync
76	TTIP1		O	Transmit Analog Tip Output
51	TTIP2		O	Transmit Analog Tip Output
26	TTIP3		O	Transmit Analog Tip Output
1	TTIP4		O	Transmit Analog Tip Output
78	TVDD1		–	Transmit Analog Positive Supply
53	TVDD2		–	Transmit Analog Positive Supply
28	TVDD3		–	Transmit Analog Positive Supply
3	TVDD4		–	Transmit Analog Positive Supply
77	TVSS1		–	Transmit Analog Signal Ground

52	TVSS2		–	Transmit Analog Signal Ground
27	TVSS3		–	Transmit Analog Signal Ground
2	TVSS4		–	Transmit Analog Signal Ground
74	WR*(R/W*)	SDI	I	Write Input(Read/Write) [Serial Data Input]

Note: EQVSS lines are tied to RVSS lines in the 100-pin LQFP package.

PIN TABLE (By LQFP Pin Number) Table 5-2

LQFP PIN	SIGNAL NAME PARALLEL PORT ENABLED	SIGNAL NAME SERIAL PORT ENABLED	TYPE	FUNCTION [Serial Port Mode In Brackets]
1	TTIP4		O	Transmit Analog Tip Output
2	TVSS4		–	Transmit Analog Signal Ground
3	TVDD4		–	Transmit Analog Positive Supply
4	TRING4		O	Transmit Analog Ring Output
5	TCLK4		I	Transmit Clock
6	TSER4		I	Transmit Serial Data
7	TSYNC4		I/O	Transmit Sync
8	DVSS4		–	Digital Signal Ground
9	DVDD4		–	Digital Positive Supply
10	OUTB3		O	User Selectable Output B
11	OUTA3		O	User Selectable Output A
12	SYSCLK3		I	Transmit/Receive System Clock
13	RSER3		O	Receive Serial Data
14	RSYNC3		I/O	Receive Sync
15	RVSS4		–	Receive Analog Signal Ground
16	RTIP3		I	Receive Analog Tip Input
17	RRING3		I	Receive Analog Ring Input
18	RVDD4		–	Receive Analog Positive Supply
19	D0/AD0		I/O	Data Bus Bit0/ Address/Data Bus Bit 0
20	D1/AD1		I/O	Data Bus Bit1/ Address/Data Bus Bit 1
21	D2/AD2		I/O	Data Bus Bit 2/Address/Data Bus Bit2
22	D3/AD3		I/O	Data Bus Bit 3/Address/Data Bus Bit 3
23	D4/AD4		I/O	Data Bus Bit4/Address/Data Bus Bit 4
24	D5/AD5		I/O	Data Bus Bit 5/Address/Data Bus Bit 5
25	D6/AD6		I/O	Data Bus Bit 6/Address/Data Bus Bit 6
26	TTIP3		O	Transmit Analog Tip Output
27	TVSS3		–	Transmit Analog Signal Ground
28	TVDD3		–	Transmit Analog Positive Supply
29	TRING3		O	Transmit Analog Ring Output
30	TCLK3		I	Transmit Clock
31	TSER3		I	Transmit Serial Data
32	TSYNC3		I/O	Transmit Sync
33	DVSS3		–	Digital Signal Ground
34	DVDD3		–	Digital Positive Supply
35	OUTB2		O	User Selectable Output B
36	OUTA2		O	User Selectable Output A
37	SYSCLK2		I	Transmit/Receive System Clock
38	RSER2		O	Receive Serial Data
39	RSYNC2		I/O	Receive Sync
40	RVSS3		–	Receive Analog Signal Ground
41	RTIP2		I	Receive Analog Tip Input
42	RRING2		I	Receive Analog Ring Input
43	RVDD3		–	Receive Analog Positive Supply
44	D7/AD7	SDO	I/O	Data Bus Bit 7/Address/Data Bus Bit 7 [Serial Data Output]
45	A0	ICES	I	Address Bus Bit 0 / Serial Port [Input Clock Edge Select]
46	A1	OCES	I	Address Bus Bit 1 / Serial Port [Output Clock Edge Select]
47	A2		I	Address Bus Bit 2

48	A3		I	Address Bus Bit 3
49	A4		I	Address Bus Bit 4
50	ALE(AS)/A5		I	Address Latch Enable /Address Bus Bit 5
51	TTIP2		O	Transmit Analog Tip Output
52	TVSS2		–	Transmit Analog Signal Ground
53	TVDD2		–	Transmit Analog Positive Supply
54	TRING2		O	Transmit Analog Ring Output
55	TCLK2		I	Transmit Clock
56	TSER2		I	Transmit Serial Data
57	TSYNC2		I/O	Transmit Sync
58	DVSS2		–	Digital Signal Ground
59	DVDD2		–	Digital Positive Supply
60	OUTB1		O	User Selectable Output B
61	OUTA1		O	User Selectable Output A
62	SYSCLK1		I	Transmit/Receive System Clock
63	RSER1		O	Receive Serial Data
64	RSYNC1		I/O	Receive Sync
65	RVSS2		–	Receive Analog Signal Ground
66	RTIP1		I	Receive Analog Tip Input
67	RRING1		I	Receive Analog Ring Input
68	RVDD2		–	Receive Analog Positive Supply
69	AJACKO		O	Alternate Jitter Attenuator Clock Output
70	AJACKI		I	Alternate Jitter Attenuator Clock Input
71	4/8/16MCK		O	4.096, 8.192 or 16.384 MHz Clock
72	REFCLK		I/O	Reference Clock
73	MCLK		I	Master Clock Input
74	WR*(R/W*)	SDI	I	Write Input(Read/Write) [Serial Data Input]
75	RD*(DS*)	SCLK	I	Read Input(Data Strobe) [Serial Port Clock]
76	TTIP1		O	Transmit Analog Tip Output
77	TVSS1		–	Transmit Analog Signal Ground
78	TVDD1		–	Transmit Analog Positive Supply
79	TRING1		O	Transmit Analog Ring Output
80	TCLK1		I	Transmit Clock
81	TSER1		I	Transmit Serial Data
82	TSYNC1		I/O	Transmit Sync
83	DVSS1		–	Digital Signal Ground
84	DVDD1		–	Digital Positive Supply
85	OUTB4		O	User Selectable Output B
86	OUTA4		O	User Selectable Output A
87	SYSCLK4		I	Transmit/Receive System Clock
88	RSER4		O	Receive Serial Data
89	RSYNC4		I/O	Receive Sync
90	RVSS1		–	Receive Analog Signal Ground
91	RTIP4		I	Receive Analog Tip Input
92	RRING4		I	Receive Analog Ring Input
93	RVDD1		–	Receive Analog Positive Supply
94	INT*		O	Interrupt
95	PBTS		I	Parallel Bus Type Select
96	BTS0			Bus Type Select 0
97	BTS1			Bus Type Select 1
98	CS*		I	Chip Select
99	TS0		I	Transceiver Select 0
100	TS1		I	Transceiver Select 1
–	EQVSS1		–	Equalizer Analog Signal Ground

–	EQVSS2		–	Equalizer Analog Signal Ground
–	EQVSS3		–	Equalizer Analog Signal Ground
–	EQVSS4		–	Equalizer Analog Signal Ground

Note: EQVSS lines are tied to RVSS lines in the 100-pin LQFP package.

5.1 PIN FUNCTION DESCRIPTION

5.1.1 System (Backplane) Interface Pins

Signal Name: **TCLK**
Signal Description: **Transmit Clock**
Signal Type: **Input**
A 2.048MHz primary clock. Used to clock data through the transmit formatter.

Signal Name: **TSER**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLK when IBO disabled. Sampled on the falling edge of SYSCLK when the IBO function is enabled.

Signal Name: **TSYNC**
Signal Description: **Transmit Sync**
Signal Type: **Input/Output**
As an input, pulse at this pin will establish either frame or multiframe boundaries for the transmitter. As an output, can be programmed to output either a frame or multiframe pulse.

Signal Name: **RSER**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on rising edges of RCLK when the receive elastic store is disabled. Updated on the rising edges of SYSCLK when the receive elastic store is enabled.

Signal Name: **RSYNC**
Signal Description: **Receive Sync**
Signal Type: **Input/Output**
An extracted pulse, one RCLK wide, is output at this pin which identifies either frame or CAS/CRC4 multiframe boundaries. If the receive elastic store is enabled, then this pin can be enabled to be an input at which a frame boundary pulse synchronous with SYSCLK is applied.

Signal Name: **SYSCLK**
Signal Description: **System Clock**
Signal Type: **Input**
2.048MHz clock that is used to clock data out of the receive elastic store. When the Interleave Bus Option is enable this can be a 4.096MHz, 8.192MHz or 16.384MHz clock.

Signal Name: **OUTA**
Signal Description: **User Selectable Output A**
Signal Type: **Output**
A multifunction pin that can be programmed by the host to output various alarms, clocks or data, or used to control external circuitry.

Signal Name: **OUTB**
Signal Description: **User Selectable Output B**
Signal Type: **Output**
A multifunction pin that can be programmed by the host to output various alarms, clocks or data, or used to control external circuitry.

5.1.2 Alternate Jitter Attenuator

Signal Name: **AJACKI**
Signal Description: **Alternate Jitter Attenuator Clock Input**
Signal Type: **Input**
Clock input to alternate jitter attenuator

Signal Name: **AJACKO**
Signal Description: **Alternate Jitter Attenuator Clock Output**
Signal Type: **Output**
Clock output of alternate jitter attenuator

5.1.3 Clock Synthesizer

Signal Name: **4/8/16MCK**
Signal Description: **4.096MHz/8.192MHz/16.384MHz Clock Output**
Signal Type: **Output**
A 4.096MHz, 8.192MHz, or 16.384MHz clock output that is referenced to one of the 4 recovered line clocks (RCLKs) or to an external 2.048MHz reference.

Signal Name: **REFCLK**
Signal Description: **Reference Clock**
Signal Type: **Input/Output**
Can be configured as an output to source a 2.048MHz reference clock or as an input to supply a 2.048MHz reference clock from an external source to the clock synthesizer.

5.1.4 Parallel Port Control Pins

Signal Name: **INT***
Signal Description: **Interrupt**
Signal Type: **Output**
Flags host controller during conditions and change of conditions defined in the Status Registers 1 and 2 and the HDLC Status Register. Active low, open-drain output.

Signal Name: **BTS0**
Signal Description: **Bus Type Select Bit 0**
Signal Type: **Input**
Used with BTS1 to select between muxed, nonmuxed, serial bus operation, and output High-Z mode.

Signal Name: **BTS1**
Signal Description: **Bus Type Select Bit 0**
Signal Type: **Input**
Used with BTS0 to select between muxed, nonmuxed, serial bus operation, and output High-Z mode.

Signal Name: **TS0**
Signal Description: **Transceiver Select Bit 0**
Signal Type: **Input**
Used with TS1 to select one of four transceivers.

Signal Name: **TS1**
Signal Description: **Transceiver Select Bit 0**
Signal Type: **Input**
Used with TS0 to select one of four transceivers.

Signal Name: **PBTS**
Signal Description: **Parallel Bus Type Select**
Signal Type: **Input**
Used to select between Motorola and Intel parallel bus types.

Signal Name: **AD0 to AD7/SDO**
Signal Description: **Data Bus or Address/Data Bus[D0 to D6]**
Data Bus or Address/Data bus[D7]/Serial Port Output
Signal Type: **Input/Output**
In nonmultiplexed bus operation (MUX = 0), serves as the data bus. In multiplexed bus operation (MUX = 1), serves as an 8-bit multiplexed address/data bus.

Signal Name: **A0 to A4**
Signal Description: **Address Bus**
Signal Type: **Input**
In nonmultiplexed bus operation, this serves as the address bus. In multiplexed bus operation, these pins are not used and should be tied low.

Signal Name: **RD*(DS*)/SCLK**
Signal Description: **Read Input - Data Strobe/Serial Port Clock**
Signal Type: **Input**
RD* and DS* are active low signals. DS active HIGH when in multiplexed mode. See bus timing diagrams.

Signal Name: **CS***
Signal Description: **Chip Select**
Signal Type: **Input**
Must be low to read or write to the device. CS* is an active low signal.

Signal Name: **ALE(AS)/A5**
Signal Description: **Address Latch Enable(Address Strobe) or A6**
Signal Type: **Input**
In nonmultiplexed bus operation, this serves as the upper address bit. In multiplexed bus operation, this serves to demultiplex the bus on a positive-going edge.

Signal Name: **WR*(R/W*)/SDI**
Signal Description: **Write Input(Read/Write)/Serial Port Data Input**
Signal Type: **Input**
WR* is an active low signal.

5.1.5 Serial Port Control Pins

Signal Name: **SDO**
Signal Description: **Serial Port Output**
Signal Type: **Output**
Data at this output can be updated on the rising or falling edge of SCLK.

Signal Name: **SDI**
Signal Description: **Serial Port Data Input**
Signal Type: **Input**
Data at this input can be sampled on the rising or falling edge of SCLK.

Signal Name: **ICES**
Signal Description: **Input Clock Edge Select**
Signal Type: **Input**
Used to select which SCLK clock edge will sample data at SDI.

Signal Name: **OCES**
Signal Description: **Output Clock Edge Select**
Signal Type: **Input**
Used to select which SCLK clock edge will update data at SDO.

Signal Name: **SCLK**
Signal Description: **Serial Port Clock**
Signal Type: **Input**
Used to clock data into and out of the serial port.

5.1.6 Line Interface Pins

Signal Name: **MCLK**
Signal Description: **Master Clock Input**
Signal Type: **Input**
A 2.048MHz (±50ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation.

Signal Name: **RTIP & RRING**
Signal Description: **Receive Tip and Ring**
Signal Type: **Input**
Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the E1 line. See Section 19 for details.

Signal Name: **TTIP & TRING**
Signal Description: **Transmit Tip and Ring**
Signal Type: **Output**
Analog line driver outputs. These pins connect via a 1:2 stepup transformer to the E1 line. See Section 19 for details.

5.1.7 Supply Pins

Signal Name: **DV_{DD}**
Signal Description: **Digital Positive Supply**
Signal Type: **Supply**
3.3V ±5%. Should be tied to the RV_{DD} and TV_{DD} pins.

Signal Name: **RV_{DD}**
Signal Description: **Receive Analog Positive Supply**
Signal Type: **Supply**
3.3V ±5%. Should be tied to the DV_{DD} and TV_{DD} pins.

Signal Name: **TV_{DD}**
Signal Description: **Transmit Analog Positive Supply**
Signal Type: **Supply**
3.3V ±5%. Should be tied to the RV_{DD} and DV_{DD} pins.

Signal Name: **DV_{SS}**
Signal Description: **Digital Signal Ground**
Signal Type: **Supply**
0V. Should be tied to the RV_{SS} and TV_{SS} pins.

Signal Name: **RV_{SS}**
Signal Description: **Receive Analog Signal Ground**
Signal Type: **Supply**
0V. Should be tied to DV_{SS} and TV_{SS}.

Signal Name: **EQV_{SS}**
Signal Description: **Receiver Equalizer Analog Signal Ground**
Signal Type: **Supply**
0V. Should be tied to DV_{SS} and TV_{SS}. Not accessible in the 100-pin LQFP package.

Signal Name: **TV_{SS}**
Signal Description: **Transmit Analog Signal Ground**
Signal Type: **Supply**
0V. Should be tied to DV_{SS} and RV_{SS}.

6. HOST INTERFACE PORT

The DS21Q50 is controlled via either a nonmultiplexed bus, a multiplexed bus or serial interface bus by an external microcontroller or microprocessor. The device can operate with either Intel or Motorola bus timing configurations. See Table 6-1 for a description of the bus configurations. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the *AC Electrical Characteristics* in Section 22 for more details.

BUS MODE SELECT Table 6-1

PBTS	BTS1	BTS0	PARALLEL PORT MODE
0	0	0	Intel Multiplexed
0	0	1	Intel Nonmultiplexed
1	0	0	Motorola Multiplexed
1	0	1	Motorola Nonmultiplexed
X	1	0	Serial
X	1	1	TEST (Outputs High-Z)

6.1 Parallel Port Operation

When using the parallel interface on the DS21Q50 (BTS1 = 0) the user has the option for either multiplexed bus operation (BTS1 = 0, BTS0 = 0) or nonmultiplexed bus operation (BTS1 = 0, BTS0 = 1). The DS21Q50 can operate with either Intel or Motorola bus timing configurations. If the PBTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in Section 24 for more details.

6.2 Serial Port Operation

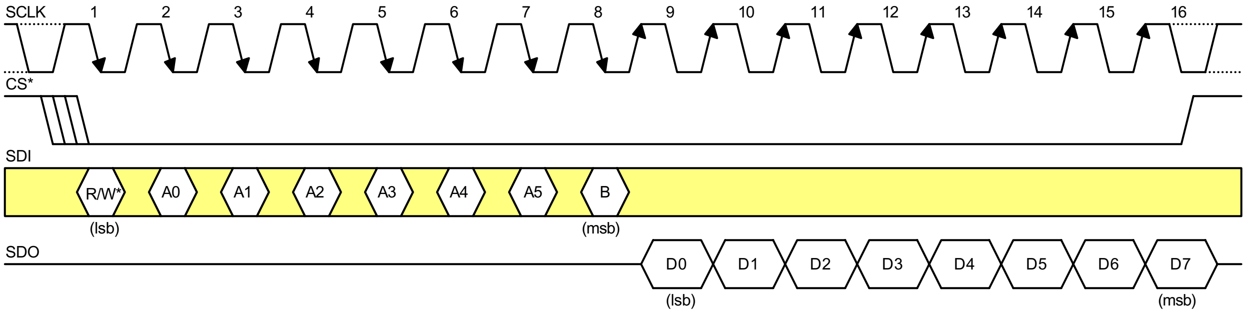
Setting BTS1 pin = 1 and the BTS0 pin = 0 enables the serial bus interface on the DS21Q50. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads or writes by the host. See Section 24 for the AC timing of the serial port. All serial port accesses are LSB first. See Figure 6-1, Figure 6-2, Figure 6-3, and Figure 6-4 for more details.

Reading or writing to the internal registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command byte specifies whether the access is a read (1) or a write (0). The next five bits identify the register address. The next bit is reserved and must be set to 0 for proper operation. The last bit (MSB) of the address/command byte enables the burst mode when set to 1. The burst mode causes all registers to be consecutively written or read.

All data transfers are initiated by driving the CS* input low. When Input Clock-Edge Select (ICES) is low, input data is latched on the rising edge of SCLK and when ICES is high, input data is latched on the falling edge of SCLK. When Output Clock-Edge Select (OCES) is low, data is output on the falling edge of SCLK and when OCES is high, data is output on the rising edge of SCLK. Data is held until the next falling or rising edge. All data transfers are terminated if the CS* input transitions high. Port control logic is disabled and SDO is 3-stated when CS* is high.

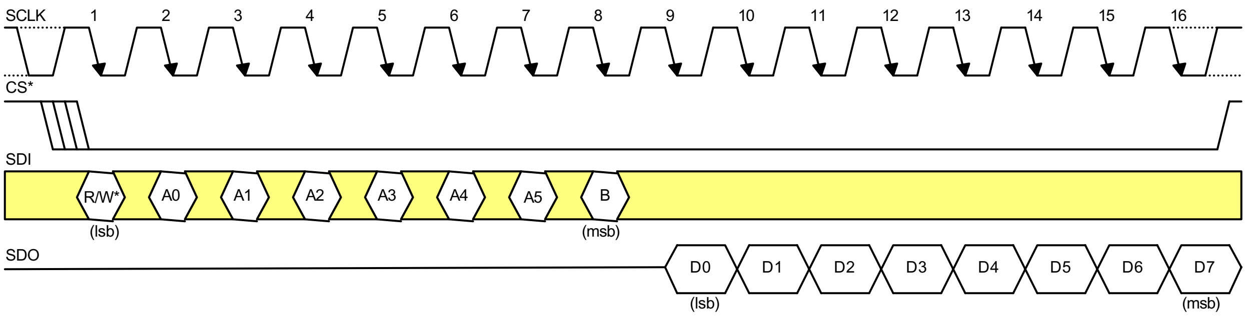
SERIAL PORT OPERATION MODE 1 Figure 6-1

ICES = 1 (sample SDI on the falling edge of SCLK)
OCES = 1 (update SDO on rising edge of SCLK)



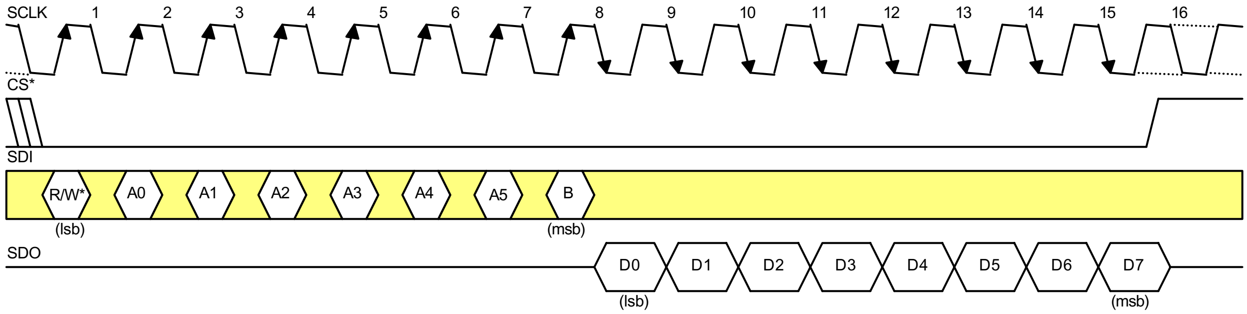
SERIAL PORT OPERATION MODE 2 Figure 6-2

ICES = 1 (sample SDI on the falling edge of SCLK)
OCES = 0 (update SDO on falling edge of SCLK)



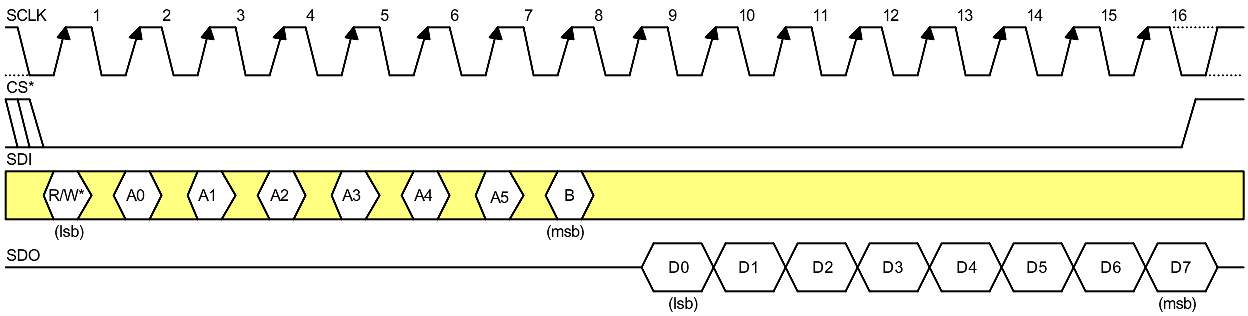
SERIAL PORT OPERATION MODE 3 Figure 6-3

ICES = 0 (sample SDI on the rising edge of SCLK)
OCES = 0 (update SDO on falling edge of SCLK)



SERIAL PORT OPERATION MODE 4 Figure 6-4

ICES = 0 (sample SDI on the rising edge of SCLK)
OCES = 1 (update SDO on rising edge of SCLK)



6.3 Register Map

REGISTER MAP SORTED BY ADDRESS Table 6-2

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
00	R	BPV or Code Violation Count 1	VCR1
01	R	BPV or Code Violation Count 2	VCR2
02	R	CRC4 Error Count 1	CRCCR1
03	R	CRC4 Error Count 2	CRCCR2
04	R	E-Bit Count 1 / PRBS Error Count 1	EBCR1
05	R	E-Bit Count 2 / PRBS Error Count 2	EBCR2
06	R	FAS Error Count 1	FASCR1
07	R	FAS Error Count 2	FASCR2
08	R/W	Receive Information	RIR
09	R	Synchronizer Status	SSR
0A	R/W	Status 1	SR1
0B	R/W	Status 2	SR2
0C	-	Unused	-
0D	-	Unused	-
0E	-	Unused	-
0F	R	Device ID **(Note 2)**	IDR
10	R/W	Receive Control	RCR
11	R/W	Transmit Control 1	TCR
12	R/W	Common Control 1	CCR1
13	R/W	Common Control 2	CCR2
14	R/W	Common Control 3	CCR3
15	R/W	Common Control 4	CCR4
16	R/W	Common Control 5	CCR5
17	R/W	Line Interface Control Register	LICR
18	R/W	Interrupt Mask 1	IMR1
19	R/W	Interrupt Mask 2	IMR2
1A	R/W	Output A Control	OUTAC
1B	R/W	Output B Control	OUTBC
1C	R/W	Interleave Bus Operation Register	IBO
1D	R/W	System Clock Interface Control Register (**Note 2)**	SCICR
1E	R/W	Test 2 **(Note 1)**	TEST2 (set to 00h)
1F	R/W	Test 3 **(Note 1)**	TEST3 (set to 00h)
20	R/W	Transmit Align Frame	TAF
21	R/W	Transmit Nonalign Frame	TNAF
22	R	Transmit DS0 Monitor	TDS0M
23	R/W	Transmit Idle Definition	TIDR
24	R/W	Transmit Idle 1	TIR1
25	R/W	Transmit Idle 2	TIR2
26	R/W	Transmit Idle 3	TIR3
27	R/W	Transmit Idle 4	TIR4
28	R	Receive Align Frame	RAF
29	R	Receive Nonalign Frame	RNAF
2A	R	Receive DS0 Monitor	RDS0M
2B	R/W	Per-Channel Loopback Control 1	PCLB1
2C	R/W	Per-Channel Loopback Control 2	PCLB2
2D	R/W	Per-Channel Loopback Control 3	PCLB3
2E	R/W	Per-Channel Loopback Control 4	PCLB4
2F	R/W	Test 1 **(Note 1)**	TEST1 (set to 00h)

NOTES:

1) Test registers are used only by the factory; these registers must be cleared (set to all zeros) on power-up initialization to ensure proper operation.
2) The Device ID register and the System Clock Interface Control register exist in Transceiver #1 only. (TS0, TS1 = 0).

7. CONTROL, ID, AND TEST REGISTERS

The operation of the DS21Q50 is configured via a set of seven control registers. Typically, the control registers are only accessed when the system is first powered up. Once the device has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There is one Receive Control Register (RCR), one Transmit Control Registers (TCR), and five Common Control Registers (CCR1 to CCR5). Each of these registers is described in this section.

There is a device identification register (IDR) at address 0Fh. The MSB of this read-only register is fixed to a one, indicating that an E1 quad transceiver is present. The next three MSBs are reserved for future use. The lower 4 bits of the device ID register are used to identify the revision of the device. This register exists in Transceiver #1 only. (TS0, TS1 = 0)

The test registers at addresses 1E, 1F, and 2F hex are used by the factory in testing the DS21Q50. On power-up, the test registers should be set to 00h in order for the DS21Q50 to operate properly.

Register Name: **IDR**
Register Description: **Device Identification Register**
Register Address: **0F Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	1	0	0	0	ID3	ID2	ID1	ID0

SYMBOL	BIT	NAME AND DESCRIPTION
1	7	**Bit 7.**
0	6	**Bit 6.**
0	5	**Bit 5.**
0	4	**Bit 4.**
ID3	3	**Chip Revision Bit 3.** MSB of a decimal code that represents the chip revision.
ID2	1	**Chip Revision Bit 2.**
ID1	2	**Chip Revision Bit 1.**
ID0	0	**Chip Revision Bit 0.** LSB of a decimal code that represents the chip revision.

7.1 Power-Up Sequence

On power-up and after the supplies are stable, the DS21Q50 should be configured for operation by writing to all of the internal registers (this includes setting the Test Registers to 00h) since the contents of the internal registers cannot be predicted on power-up. The LIRST (CCR5.4) should be toggled from zero to one to reset the line interface circuitry (it will take the device about 40ms to recover from the LIRST bit being toggled). Finally, after the SYSCLK input is stable, the ESR bits (CCR4.5 and CCR4.6) should be toggled from a zero to a one (this step can be skipped if the elastic store is disabled).

Register Name: **RCR**
Register Description: **Receive Control Register**
Register Address: **10 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	RSMF	RSM	RSIO	RESE	-	FRC	SYNC	RESYNC

SYMBOL	BIT	NAME AND DESCRIPTION
RSMF	7	**RSYNC Multiframe Function.** Only used if the RSYNC pin is programmed in the multiframe mode (RCR.6 = 1). 0 = RSYNC outputs CAS multiframe boundaries 1 = RSYNC outputs CRC4 multiframe boundaries
RSM	6	**RSYNC Mode Select.** 0 = frame mode (See the timing in Section 22.1) 1 = multiframe mode (See the timing in Section 22.1)
RSIO	5	**RSYNC I/O Select.** (Note: This bit must be set to zero when RCR .4 = 0). 0 = RSYNC is an output (depends on RCR.6) 1 = RSYNC is an input (only valid if elastic store enabled)
RESE	4	**Receive Elastic Store Enable.** 0 = elastic store is bypassed 1 = elastic store is enabled
-	3	**Unused.** Should Be set = 0 for proper operation
FRC	2	**Frame Resync Criteria.** 0 = resync if FAS received in error three consecutive times 1 = resync if FAS or bit 2 of non-FAS is received in error three consecutive times
SYNCE	1	**Sync Enable.** 0 = auto resync enabled 1 = auto resync disabled
RESYNC	0	**Resync.** When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.

SYNC/RESYNC CRITERIA Table 7-1

FRAME OR MULTIFRAME LEVEL	SYNC CRITERIA	RESYNC CRITERIA	ITU SPEC.
FAS	FAS present in frame N and N + 2, and FAS not present in frame N + 1	Three consecutive incorrect FAS received Alternate (RCR1.2 = 1) the above criteria is met or three consecutive incorrect bit 2 of non-FAS received	G.706 4.1.1 4.1.2
CRC4	Two valid MF alignment words found within 8ms	915 or more CRC4 code words out of 1000 received in error	G.706 4.2 and 4.3.2
CAS	Valid MF alignment word found and previous timeslot 16 contains code other than all zeros	Two consecutive MF alignment words received in error	G.732 5.2

Register Name: **TCR**
Register Description: **Transmit Control Register**
Register Address: **11 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	IFSS	TFPT	AEBE	TUA1	TSiS	TSA1	TSM	TSIO

SYMBOL	BIT	NAME AND DESCRIPTION
IFSS	7	**Internal Frame Sync Select.** 0 = TSYNC normal 1 = If TSYNC is in the INPUT mode (TSIO = 0) then TSYNC is internally replaced by the recovered receive frame sync. The TSYNC pin is ignored 1 = If TSYNC is in the OUTPUT mode (TSIO = 1) then TSYNC outputs the recovered multiframe frame sync.
TFPT	6	**Transmit Timeslot 0 Pass Through.** 0 = FAS bits/Sa bits/Remote Alarm sourced internally from the TAF and TNAF registers 1 = FAS bits/Sa bits/Remote Alarm sourced from TSER
AEBE	5	**Automatic E–Bit Enable.** 0 = E–bits not automatically set in the transmit direction 1 = E–bits automatically set in the transmit direction
TUA1	4	**Transmit Unframed All Ones.** 0 = transmit data normally 1 = transmit an unframed all one's code
TSiS	3	**Transmit International Bit Select.** 0 = sample Si bits at TSER pin 1 = source Si bits from TAF and TNAF registers (in this mode, TCR.6 must be set to 0)
TSA1	2	**Transmit Signaling All Ones.** 0 = normal operation 1 = force timeslot 16 in every frame to all ones
TSM	1	**TSYNC Mode Select.** 0 = frame mode (see the timing in Section 22.2) 1 = CAS and CRC4 multiframe mode (see the timing in Section 22.2)
TSIO	0	**TSYNC I/O Select.** 0 = TSYNC is an input 1 = TSYNC is an output

Note: See Figure 22-9 for more details about how the Transmit Control Register affects the operation of the DS21Q50.

Register Name: **CCR1**
Register Description: **Common Control Register 1**
Register Address: **12 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	FLB	THDB3	TIBE	TCRC4	RSMS	RHDB3	PCLMS	RCRC4

SYMBOL	BIT	NAME AND DESCRIPTION
FLB	7	**Framer Loopback.** See Section 7.2 for details 0 = loopback disabled 1 = loopback enabled
THDB3	6	**Transmit HDB3 Enable.** 0 = HDB3 disabled 1 = HDB3 enabled
TIBE	5	**Transmit Insert Bit Error.** A zero to one transition causes a single bit error to be inserted in the transmit path
TCRC4	4	**Transmit CRC4 Enable.** 0 = CRC4 disabled 1 = CRC4 enabled
RSMS	3	**Receive Signaling Mode Select.** 0 = CAS signaling mode. Receiver will search for the CAS MF alignment signal 1 = CCS signaling mode. Receiver will not search for the CAS MF alignment signal
RHDB3	2	**Receive HDB3 Enable.** 0 = HDB3 disabled 1 = HDB3 enabled
PCLMS	1	**Per Channel Loopback Mode Select.** See Section 0 for details 0 = Remote Per Channel Loopback 1 = Local Per Channel Loopback
RCRC4	0	**Receive CRC4 Enable.** 0=CRC4 disabled 1=CRC4 enabled

7.2 Framer Loopback

When CCR1.7 is set to a one, the DS21Q50 will enter a Framer Loopback (FLB) mode (Figure 4-1). This loopback is useful in testing and debugging applications. In FLB, the SCT will loop data from the transmitter back to the receiver. When FLB is enabled, the following will occur:

1) Data will be transmitted as normal at TPOSO and TNEGO.
2) Data input via RPOSI and RNEGI will be ignored.
3) The RCLK output will be replaced with the TCLK input.

Register Name: **CCR2**
Register Description: **Common Control Register 2**
Register Address: **13 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	RCUS	VCRFS	AAIS	ARA	RSERC	LOTCMC	RCLA	TCSS

SYMBOL	BIT	NAME AND DESCRIPTION
ECUS	7	**Error Counter Update Select.** See Section 9 for details. 0 = update error counters once a second 1 = update error counters every 62.5ms (500 frames)
VCRFS	6	**VCR Function Select.** See Section 9 for details. 0 = count BiPolar Violations (BPVs) 1 = count Code Violations (CVs)
AAIS	5	**Automatic AIS Generation.** 0 = disabled 1 = enabled
ARA	4	**Automatic Remote Alarm Generation.** 0 = disabled 1 = enabled
RSERC	3	**RSER Control.** 0 = allow RSER to output data as received under all conditions 1 = force RSER to one under loss of frame alignment conditions
LOTCMC	2	**Loss of Transmit Clock Mux Control.** Determines whether the transmit formatter should switch to the ever present RCLK if the TCLK should fail to transition 0 = do not switch to RCLK if TCLK stops 1 = switch to RCLK if TCLK stops
RCLA	1	**Receive Carrier Loss (RCL) Alternate Criteria.** 0 = RCL declared upon 255 consecutive zeros (125µs) 1 = RCL declared upon 2048 consecutive zeros (1ms)
TCSS	0	**Transmit Clock Source Select.** This function allows the user to internally select RCLK as the clock source for the transmit formatter. 0 = Source of transmit clock determined by CCR2.2 (LOTCMC) 1 = Force transmitter to internally switch to RCLK as source of transmit clock. Signal at TCLK pin is ignored

7.3 Automatic Alarm Generation

The device can be programmed to automatically transmit AIS or Remote Alarm. When automatic AIS generation is enabled (CCR2.5 = 1), the device monitors the receive framer to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all one's) reception, or loss of receive carrier (or signal). If any one (or more) of the above conditions is present, then the framer will either force an AIS alarm.

When automatic RAI generation is enabled (CCR2.4 = 1), the framer monitors the receive to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all one's) reception, or loss of receive carrier (or signal) or if CRC4 multiframe synchronization cannot be found within 128ms of FAS synchronization (if CRC4 is enabled). If any one (or more) of the above conditions is present, then the framer will either transmit a RAI alarm. RAI generation conforms to ETS 300 011 specifications and a constant Remote Alarm will be transmitted if the DS21Q50 cannot find CRC4 multiframe synchronization within 400ms as per G.706.

Register Name: **CCR3**
Register Description: **Common Control Register**
Register Address: **14 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	RLB	LLB	LIAIS	TCM4	TCM3	TCM2	TCM1	TCM0

SYMBOL	BIT	NAME AND DESCRIPTION
RLB	7	**Remote Loopback.** See Section 7.4 for details 0 = loopback disabled 1 = loopback enabled
LLB	6	**Local Loopback.** See Section 7.5 for details 0=loopback disabled 1=loopback enabled
LIAIS	5	**Line Interface AIS Generation Enable.** 0=allow normal data to be transmitted at TTIP and TRING 1=force unframed all ones to be transmitted at TTIP and TRING at the MCLK rate
TCM4	4	**Transmit Channel Monitor Bit 4**. MSB of a channel decode that determines which transmit channel data will appear in the TDS0M register. See Section 9 or details.
TCM3	3	**Transmit Channel Monitor Bit 3.**
TCM2	2	**Transmit Channel Monitor Bit 2.**
TCM1	1	**Transmit Channel Monitor Bit 1.**
TCM0	0	**Transmit Channel Monitor Bit 0.** LSB of the channel decode.

7.4 Remote Loopback

When CCR4.7 is set to a one, the DS21Q50 will be forced into Remote Loopback (RLB). In this loopback, data input via the RPOSI and RNEGI pins will be transmitted back to the TPOSO and TNEGO pins. Data will continue to pass through the receive framer of the DS21Q50 as it would normally and the data from the transmit formatter will be ignored (Figure 4-1).

7.5 Local Loopback

When CCR4.6 is set to a one, the DS21Q50 will be forced into Local Loopback (LLB). In this loopback, data will continue to be transmitted as normal. Data being received at RTIP and RRING will be replaced with the data being transmitted. Data in this loopback will pass through the jitter attenuator (Figure 4-1).

Register Name: **CCR4**
Register Description: **Common Control Register 4**
Register Address: **15 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	LIRST	RESA	RESR	RCM4	RCM3	RCM2	RCM1	RCM0

SYMBOL	BIT	NAME AND DESCRIPTION
LIRST	7	**Line Interface Reset.** Setting this bit from a zero to a one will initiate an internal reset that affects the clock recovery state machine and jitter attenuator. Normally this bit is only toggled on power-up. Must be cleared and set again for a subsequent reset.
RESA	6	**Receive Elastic Store Align.** Setting this bit from a zero to a one may force the receive elastic store's write/read pointers to a minim separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less then half a frame, the command will be executed and data will be disrupted. Should be toggled after SYSCLK has been applied and is stable. Must be cleared and set again for a subsequent align. See Section 16 for details.
RESR	5	**Receive Elastic Store Reset.** Setting this bit from a zero to a one will force the receive elastic store to a depth of one frame. Receive data is lost during the reset. Should be toggled after SYSCLK has been applied and is stable. Must be cleared and set again for a subsequent reset. See Section 16 for details.
RCM4	4	**Receive Channel Monitor Bit 4.** MSB of a channel decode that determines which receive channel data will appear in the RDS0M register. See Section 9 for details.
RCM3	3	**Receive Channel Monitor Bit 3.**
RCM2	2	**Receive Channel Monitor Bit 2.**
RCM1	1	**Receive Channel Monitor Bit 1.**
RCM0	0	**Receive Channel Monitor Bit 0.** LSB of the channel decode.

Register Name: **CCR5**
Register Description: **Common Control Register 5**
Register Address: **16 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	LIUODO	CDIG	LIUSI	IRTSEL	TPRBS1	TPRBS0	RPRBS1	RPRBS0

SYMBOL	BIT	NAME AND DESCRIPTION
LIUODO	7	**Line Interface Open-Drain Option.** This control bit determines whether the TTIP and TRING outputs will be open drain or not. The line driver outputs can be forced open drain to allow 6Vpeak pulses to be generated or to allow the creation of a very low power interface. 0 = allow TTIP and TRING to operate normally 1 = force the TTIP and TRING outputs to be open drain
CDIG	6	**Customer Disconnect Indication Generator.** This control bit determines whether the Line Interface will generate an unframed ...1010... pattern at TTIP and TRING instead of the normal data pattern. 0 = generate normal data at TTIP & TRING 1 = generate a ...1010... pattern at TTIP and TRING
LIUSI	5	**Line Interface G.703 Synchronization Interface Enable.** This control bit determines whether the line receiver should handle a normal E1 signal (Section 6 of G.703) or a 2.048MHz synchronization signal (Section 10 of G.703). This control has no affect on the line interface transmitter. 0 = line receiver configured to support a normal E1 signal 1 = line receiver configured to support a synchronization signal
IRTSEL	4	**Receive Termination Select.** This function applies internal parallel resistance to the normal 120O external termination to create a 75O termination. 0 = normal 120O external termination 1 = internally adjust receive termination to 75O
TPRBS1	3	**Transmit PRBS Mode Bit 1.**
TPRBS0	2	**Transmit PRBS Mode Bit 0.**.
RPRBS1	1	**Receive PRBS Mode Bit 1.**
RPRBS0	0	**Receive PRBS Mode Bit 0.**

8. STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real-time status of a framer in the DS21Q50: Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register (RIR), and Synchronizer Status Register (SSR).

When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a one. All of the bits in SR1, SR2, and RIR1 registers operate in a latched fashion. The Synchronizer Status Register contents are not latched. This means that if an event or an alarm occurs and a bit is set to a one in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again (or in the case of the RUA1, RRA, RCL, and RLOS alarms, the bit will remain set if the alarm is still present).

The user will always precede a read of the SR1, SR2 and RIR registers with a write. The byte written to the register will inform the framer which bits the user wishes to read and have cleared. The user will write a byte to one of these registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with the latest information. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write-read-write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21Q50 with higher order software languages.

The SSR register operates differently than the other three. It is a read only register and it reports the status of the synchronizer in real time. This register is not latched and it is not necessary to precede a read of this register with a write.

The SR1and SR2 registers have the unique ability to initiate a hardware interrupt via the INT* output pin. Each of the alarms and events in SR1 and SR2 can be either masked or unmasked from the interrupt pin via Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2).

The interrupts caused by alarms in SR1 (namely RUA1, RRA, RCL, and RLOS) act differently than the interrupts caused by events in SR1 and SR2 (namely RSA1, RDMA, RSA0, RSLIP, RMF, TMF, SEC, TAF, LOTC, and RCMF). The alarm caused interrupts will force the INT* pin low whenever the alarm changes state (i.e., the alarm goes active or inactive according to the set/clear criteria in Table 8-1). The INT* pin will be allowed to return high (if no other interrupts are present) when the user reads the alarm bit that caused the interrupt to occur even if the alarm is still present.

The event-based interrupts force the INT pin low when the event occurs. The INT pin will return high () when the user reads the event bit that caused the interrupt to occur. Furthermore, some event-based interrupts will occur continuously as long as the event is occurring (RSLIP, SEC, TMF, RMF, TAF, RAF, RCMF). Other event-based interrupts force the INT pin low only once when the event is first detected (LOTC, PRSBD, RDMA, RSA1, RSA0), i.e., the PRBSD interrupt will fire once when the receiver detects the PRBS pattern. IF the receiver continues to receive the PRBS pattern, no more interrupts will fire. If the receiver then detects that PRBS is no longer being sent, the receiver will reset and when it receives the PRBS pattern again, another interrupt will fire.

Register Name: **RIR**
Register Description: **Receive Information Register**
Register Address: **08 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	RGM1	RGM0	JALT	RESF	RESE	CRCRC	FASRC	CASRC

SYMBOL	BIT	NAME AND DESCRIPTION
RGM1	7	**Receive Gain Monitor Bit 1.** See table below for level indication.*
RGM0	6	**Receive Gain Monitor Bit 0.** See table below for level indication.*
JALT	5	**Jitter Attenuator Limit Trip**. Set when the jitter attenuator FIFO reaches to within 4 bits of its limit; useful for debugging jitter attenuation operation.
RESF	4	**Receive Elastic Store Full.** Set when the receive elastic store buffer fills and a frame is deleted.
RESE	3	**Receive Elastic Store Empty.** Set when the receive elastic store buffer empties and a frame is repeated.
CRCRC	2	**CRC Resync Criteria Met.** Set when 915/1000 code words are received in error.
FASRC	1	**FAS Resync Criteria Met.** Set when three consecutive FAS words are received in error.
CASRC	0	**CAS Resync Criteria Met.** Set when two consecutive CAS MF alignment words are received in error.

***LEVEL INDICATION**

RGM1	RGM0	LEVEL (dB)
0	0	0 to 10
0	1	10 to 20
1	0	20 to 30
1	1	>30

Register Name: **SSR**
Register Description: **Synchronizer Status Register**
Register Address: **09 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	CSC5	CSC4	CSC3	CSC2	CSC0	FASSA	CASSA	CRC4SA

SYMBOL	BIT	NAME AND DESCRIPTION
CSC5	7	**CRC4 Sync Counter Bit 5.** MSB of the 6-bit counter.
CSC4	6	**CRC4 Sync Counter Bit 4.**
CSC3	5	**CRC4 Sync Counter Bit 3.**
CSC2	4	**CRC4 Sync Counter Bit 2.**
CSC0	3	**CRC4 Sync Counter Bit 0.** LSB of the 6-bit counter. Counter Bit 1 is not accessible.
FASSA	2	**FAS Sync Active.** Set while the synchronizer is searching for alignment at the FAS level.
CASSA	1	**CAS MF Sync Active.** Set while the synchronizer is searching for the CAS MF alignment word.
CRC4SA	0	**CRC4 MF Sync Active.** Set while the synchronizer is searching for the CRC4 MF alignment word.

8.1 CRC4 Sync Counter

The CRC4 Sync Counter increments each time the 8ms CRC4 multiframe search times out. The counter is cleared when the framer has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (CCR1.0 = 0). This counter is useful for determining the amount of time the framer has been searching for synchronization at the CRC4 level. ITU G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400ms, then the search should be abandoned and proper action taken. The CRC4 Sync Counter will rollover.

ALARM CRITERIA Table 8-1

ALARM	SET CRITERIA	CLEAR CRITERIA	ITU SPEC.
RSA1 (receive signaling all ones)	Over 16 consecutive frames (one full MF) timeslot 16 contains less than three zeros	Over 16 consecutive frames (one full MF) timeslot 16 contains three or more zeros	G.732 4.2
RSA0 (receive signaling all zeros)	Over 16 consecutive frames (one full MF) timeslot 16 contains all zeros	Over 16 consecutive frames (one full MF) timeslot 16 contains at least a single one	G.732 5.2
RDMA (receive distant multiframe alarm)	Bit 6 in timeslot 16 of frame 0 set to one for two consecutive MF	Bit 6 in timeslot 16 of frame 0 set to zero for two consecutive MF	O.162 2.1.5
RUA1 (receive unframed all ones)	Less than three zeros in two frames (512 bits)	More than two zeros in two frames (512 bits)	O.162 1.6.1.2
RRA (receive remote alarm)	Bit 3 of nonalign frame set to one for three consecutive occasions	Bit 3 of nonalign frame set to zero for three consecutive occasions	O.162 2.1.4
RCL (receive carrier loss)	255 (or 2048) consecutive zeros received	In 255-bit times, at least 32 ones are received	G.775/ G.962

Register Name: **SR1**
Register Description: **Status Register 1**
Register Address: **0A Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS

SYMBOL	BIT	NAME AND DESCRIPTION
RSA1	7	**Receive Signaling All Ones.** Set when the contents of timeslot 16 contains less than three zeros over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode. Both RSA1 and RSA0 will be set if a change in signaling is detected.
RDMA	6	**Receive Distant MF Alarm.** Set when bit–6 of timeslot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.
RSA0	5	**Receive Signaling All Zeros.** Set when over a full MF, timeslot 16 contains all zeros. Both RSA1 and RSA0 will be set if a change in signaling is detected.
RSLIP	4	**Receive Elastic Store Slip.** Set when the elastic store has either repeated or deleted a frame of data.
RUA1	3	**Receive Unframed All Ones.** Set when an unframed all ones code is received at RPOSI and RNEGI.
RRA	2	**Receive Remote Alarm.** Set when a remote alarm is received at RPOSI and RNEGI.
RCL	1	**Receive Carrier Loss.** Set when 255 (or 2048 if CCR2.1=1) consecutive zeros have been detected at RTIP and RRING. (note: a receiver carrier loss based on data received at RPOSI and RNEGI is available in the HSR register)
RLOS	0	**Receive Loss of Sync.** Set when the device is not synchronized to the receive E1 stream.

Register Name: **IMR1**
Register Description: **Interrupt Mask Register 1**
Register Address: **18 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS

SYMBOL	BIT	NAME AND DESCRIPTION
RSA1	7	**Receive Signaling All Ones.** 0=interrupt masked 1=interrupt enabled
RDMA	6	**Receive Distant MF Alarm.** 0=interrupt masked 1=interrupt enabled
RSA0	5	**Receive Signaling All Zeros.** 0=interrupt masked 1=interrupt enabled
RSLIP	4	**Receive Elastic Store Slip Occurrence.** 0=interrupt masked 1=interrupt enabled
RUA1	3	**Receive Unframed All Ones.** 0=interrupt masked 1=interrupt enabled
RRA	2	**Receive Remote Alarm.** 0=interrupt masked 1=interrupt enabled
RCL	1	**Receive Carrier Loss.** 0=interrupt masked 1=interrupt enabled
RLOS	0	**Receive Loss of Sync.** 0=interrupt masked 1=interrupt enabled

Register Name: **SR2**
Register Description: **Status Register 2**
Register Address: **0B Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	PRBSD

SYMBOL	BIT	NAME AND DESCRIPTION
RMF	7	**Receive CAS Multiframe**. Set every 2ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries.
RAF	6	**Receive Align Frame.** Set every 250µs at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.
TMF	5	**Transmit Multiframe.** Set every 2ms (regardless if CRC4 is enabled) on transmit multiframe boundaries.
SEC	4	**One Second Timer.** Set on increments of one second based on RCLK. If CCR2.7=1, then this bit will be set every 62.5ms instead of once a second.
TAF	3	**Transmit Align Frame.** Set every 250µs at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.
LOTC	2	**Loss of Transmit Clock.** Set when the TCLK pin has not transitioned for one channel time (or 3.9ms).
RCMF	1	**Receive CRC4 Multiframe.** Set on CRC4 multiframe boundaries; will continue to be set every 2ms on an arbitrary boundary if CRC4 is disabled.
PRBSD	0	**Pseudo Random Bit Sequence Detect.** When receive PRBS is enabled this bit will be set when the 2^{15}-1 PRBS pattern is detected at RPOS and RNEG. The PRBS pattern can be framed, un-framed, or in a specific time slot.

Register Name: **IMR2**
Register Description: **Interrupt Mask Register 2**
Register Address: **19 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	PRBSD

SYMBOL	BIT	NAME AND DESCRIPTION
RMF	7	**Receive CAS Multiframe.** 0=interrupt masked 1=interrupt enabled
RAF	6	**Receive Align Frame.** 0=interrupt masked 1=interrupt enabled
TMF	5	**Transmit Multiframe.** 0=interrupt masked 1=interrupt enabled
SEC	4	**One Second Timer.** 0=interrupt masked 1=interrupt enabled
TAF	3	**Transmit Align Frame.** 0=interrupt masked 1=interrupt enabled
LOTC	2	**Loss Of Transmit Clock.** 0=interrupt masked 1=interrupt enabled
RCMF	1	**Receive CRC4 Multiframe.** 0=interrupt masked 1=interrupt enabled
PRBSD	0	**Pseudo Random Bit Sequence Detect.** 0=interrupt masked 1=interrupt enabled

9. ERROR COUNT REGISTERS

There are a set of four counters in each transceiver of the DS21Q50 that record bipolar or code violations, errors in the CRC4 SMF code words, E bits as reported by the far end, and word errors in the FAS. The E-bit counter is reconfigured for counting errors in the PRBS pattern if receive PRBS is enabled. Each of these four counters are automatically updated on either one second boundaries (CCR2.70 = 0) or every 62.5ms (CCR2.7 = 1) as determined by the timer in Status Register 2 (SR2.4). Hence, these registers contain performance data from either the previous second or the previous 62.5ms. The user can use the interrupt from the one second timer to determine when to read these registers. The user has a full second (or 62.5ms) to read the counters before the data is lost. All four counters will saturate at their respective maximum counts and they will not rollover.

9.1 BPV or Code Violation Counter

Violation Count Register 1 (VCR1) is the most significant word and VCR2 is the least significant word of a 16–bit counter that records either BiPolar Violations (BPVs) or Code Violations (CVs). If CCR2.6=0, then the VCR counts bipolar violations. Bipolar violations are defined as consecutive marks of the same polarity. In this mode, if the HDB3 mode is set for the receiver via CCR1.2, then HDB3 code words are not counted as BPVs. If CCR2.6=1, then the VCR counts code violations as defined in ITU O.161. Code violations are defined as consecutive bipolar violations of the same polarity. In most applications, the framer should be programmed to count BPVs when receiving AMI code and to count CVs when receiving HDB3 code. This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit error rate on an E1 line would have to be greater than 10^{-2} before the VCR would saturate.

Register Name: **VCR1, VCR2**
Register Description: **BiPolar Violation Count Registers**
Register Address: **00 Hex, 01 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	V15	V14	V13	V12	V11	V10	V9	V8
SYM	V7	V6	V5	V4	V3	V2	V1	V0

SYMBOL	BIT	NAME AND DESCRIPTION
V15	VCR1.7	**MSB of the 16-bit code violation count**
V0	VCR2.0	**LSB of the 16-bit code violation count**

9.2 CRC4 Error Counter

CRC4 Count Register 1 (CRCCR1) is the most significant word and CRCCR2 is the least significant word of a 16–bit counter that records word errors in the Cyclic Redundancy Check 4 (CRC4). Since the maximum CRC4 count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level. CRCCR1 and CRCCR2 have an alternate function.

Register Name: **CRCCR1, CRCCR2**
Register Description: **CRC4 Count Registers**
Register Address: **02 Hex, 03 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9	CRC8
SYM	CRC7	CRC6	CRC5	CRC4	CRC/3	CRC2	CRC1	CRC0

SYMBOL	BIT	NAME AND DESCRIPTION
CRC15	CRCCR1.7	**MSB of the 16–Bit CRC4 error count**
CRC0	CRCCR2.0	**LSB of the 16–Bit CRC4 error count**

9.3 E-Bit/PRBS Bit Error Counter

E-bit Count Register 1 (EBCR1) is the most significant word and EBCR2 is the least significant word of a 16-bit counter that records Far End Block Errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These error count registers will increment once each time the received E–bit is set to zero. Since the maximum E–bit count in a one-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

Alternately, this counter will count bit errors in the received PRBS pattern when the receive PRBS function is enabled. In this mode, the counter is active when the receive PRBS detector can synchronize to the PRBS pattern. This pattern may be framed, unframed or in any time slot. See Section 11 for more details.

Register Name: **EBCR1, EBCR2**
Register Description: **E-Bit Count Registers**
Register Address: **04 Hex, 05 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	EB15	EB14	EB13	EB12	EB11	EB10	EB9	EB8
SYM	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0

SYMBOL	BIT	NAME AND DESCRIPTION
EB15	EBCR1.7	**MSB of the 16-Bit E-Bit Error Count**
EB0	EBCR2.0	**LSB of the 16-Bit E-Bit Error Count**

9.4 FAS Error Counter

FAS Count Register 1 (FASCR1) is the most significant word and FASCR2 is the least significant word of a 16-bit counter that records word errors in the Frame Alignment Signal in timeslot 0. This counter is disabled when RLOS is high. FAS errors will not be counted when the framer is searching for FAS alignment and/or synchronization at either the CAS or CRC4 multiframe level. Since the maximum FAS word error count in a one-second period is 4000, this counter cannot saturate.

Register Name: **FASCR1, FASCR2**
Register Description: **FAS Error Count Registers**
Register Address: **06 Hex, 07 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	FAS15	FAS14	FAS13	FAS12	FAS11	FAS10	FAS9	FAS8
SYM	FAS7	FAS6	FAS5	FAS4	FAS3	FAS2	FAS1	FAS0

SYMBOL	BIT	NAME AND DESCRIPTION
FAS15	FASCR1.7	**MSB of the 16-Bit FAS Error Count**
FAS0	FASCR2.0	**LSB of the 16-Bit FAS Error Count**

10. DS0 MONITORING FUNCTION

Each framer in the DS21Q50 has the ability to monitor one DS0 (64kbps) channel in the transmit direction and one DS0 channel in the receive direction at the same time. In the transmit direction the user will determine which channel is to be monitored by properly setting the TCM0 to TCM4 bits in the CCR3 register. In the receive direction, the RCM0 to RCM4 bits in the CCR4 register need to be properly set. The DS0 channel pointed to by the TCM0 to TCM4 bits will appear in the Transmit DS0 Monitor (TDS0M) register and the DS0 channel pointed to by the RCM0 to RCM4 bits will appear in the Receive DS0 (RDS0M) register. The TCM4 to TCM0 and RCM4 to RCM0 bits should be programmed with the decimal decode of the appropriate E1 channel. For example, if DS0 channel 6 in the transmit direction and DS0 channel 15 in the receive direction needed to be monitored, then the following values would be programmed into CCR4 and CCR5:

TCM4 = 0 RCM4 = 0
TCM3 = 0 RCM3 = 1
TCM2 = 1 RCM2 = 1
TCM1 = 0 RCM1 = 1
TCM0 = 1 RCM0 = 0

Register Name: **CCR3** (Repeated here from Section 6 for convenience)
Register Description: **Common Control Register 3**
Register Address: **14 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	RLB	LLB	LIAIS	TCM4	TCM3	TCM2	TCM1	TCM0

SYMBOL	BIT	NAME AND DESCRIPTION
RLB	7	**Remote Loopback.**
LLB	6	**Local Loopback.**
LIAIS	5	**Line Interface AIS Generation Enable.**
TCM4	4	**Transmit Channel Monitor Bit 4**. MSB of a channel decode that determines which transmit channel data will appear in the TDS0M register. See Section 9 or details.
TCM3	3	**Transmit Channel Monitor Bit 3.**
TCM2	2	**Transmit Channel Monitor Bit 2.**
TCM1	1	**Transmit Channel Monitor Bit 1.**
TCM0	0	**Transmit Channel Monitor Bit 0.** LSB of the channel decode.

Register Name: **TDS0M**
Register Description: **Transmit Ds0 Monitor Register**
Register Address: **22 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	B1	B2	B3	B4	B5	B6	B7	B8

SYMBOL	BIT	NAME AND DESCRIPTION
B1	7	**Transmit DS0 Channel Bit 1.** MSB of the DS0 channel (first bit to be transmitted).
B2	6	**Transmit DS0 Channel Bit 2.**
B3	5	**Transmit DS0 Channel Bit 3.**
B4	4	**Transmit DS0 Channel Bit 4.**
B5	3	**Transmit DS0 Channel Bit 5.**
B6	2	**Transmit DS0 Channel Bit 6.**
B7	1	**Transmit DS0 Channel Bit 7.**
B8	0	**Transmit DS0 Channel Bit 8.** LSB of the DS0 channel (last bit to be transmitted).

Register Name: **CCR4** (Repeated here from Section 6 for convenience)
Register Description: **Common Control Register 4**
Register Address: **15 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	LIRST	RESA	RESR	RCM4	RCM3	RCM2	RCM1	RCM0

SYMBOL	BIT	NAME AND DESCRIPTION
LIRST	7	**Line Interface Reset.**
RESA	6	**Receive Elastic Store Align.**
RESR	5	**Receive Elastic Store Reset.**
RCM4	4	**Receive Channel Monitor Bit 4.** MSB of a channel decode that determines which receive channel data will appear in the RDS0M register. See Section 9 for details.
RCM3	3	**Receive Channel Monitor Bit 3.**
RCM2	2	**Receive Channel Monitor Bit 2.**
RCM1	1	**Receive Channel Monitor Bit 1.**
RCM0	0	**Receive Channel Monitor Bit 0.** LSB of the channel decode.

Register Name: **RDS0M**
Register Description: **Receive Ds0 Monitor Register**
Register Address: **2A Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	B1	B2	B3	B4	B5	B6	B7	B8

SYMBOL	BIT	NAME AND DESCRIPTION
B1	7	**Receive DS0 Channel Bit 1.** MSB of the DS0 channel (first bit received).
B2	6	**Receive DS0 Channel Bit 2.**
B3	5	**Receive DS0 Channel Bit 3.**
B4	4	**Receive DS0 Channel Bit 4.**
B5	3	**Receive DS0 Channel Bit 5.**
B6	2	**Receive DS0 Channel Bit 6.**
B7	1	**Receive DS0 Channel Bit 7.**
B8	0	**Receive DS0 Channel Bit 8.** LSB of the DS0 channel (last bit received).

11. PRBS GENERATION AND DETECTION

The DS21Q50 can transmit and receive the 2^{15} - 1 PRBS pattern. This PRBS pattern complies with ITU-T O.151 specifications. The PRBS pattern can be unframed (in all 256 bits of the frame), framed (in all time slots except TS0), or in any single time slot. Register CCR5 contains the control bits for configuring the transmit and receives PRBS functions. Refer to Table 11-1 and Table 11-2 for selecting the transmit and receive modes of operation. In transmit and receive mode 1 operation, the Transmit Channel Monitor and Receive Channel Monitor select bits of registers CCR3 and CCR4 have an alternate use. When this mode is selected, these bits will determine which time slot will transmit and/or receive the PRBS pattern.

SR2.0 will indicate when the receiver has synchronized to the PRBS pattern. The PRBS synchronizer will remain in sync until it experiences 6-bit errors or more within a 64-bit span. Choosing any receive mode, other than NORMAL, will cause the 16-bit E-Bit error counter, EBCR1 and EBCR2, to be re-configured for counting PRBS errors.

User definable outputs OUTA or OUTB may be configured to output a pulse for every bit error received. See Section 18 and Table 18-1 for details. This signal can be used with external circuitry to keep track of bit error rates during PRBS testing. Once synchronized, any bit errors received will cause a positive going pulse, synchronous with RCLK.

TRANSMIT PRBS MODE SELECT Table 11-1

TPRBS1 (CCR5.3)	TPBRS0 (CCR5.2)	MODE
0	0	**Mode 0**: Normal (PRBS disabled)
0	1	**Mode 1**: PRBS in TSx. PRBS pattern is transmitted in a single time slot (TS). In this mode the Transmit Channel Monitor select bits in register CCR3 are used to select a time slot in which to transmit the PRBS pattern.
1	0	**Mode 2**: PRBS in all but TS0. PRBS pattern is transmitted in time slots 1 through 31.
1	1	**Mode 3**: PRBS unframed. PRBS pattern is transmitted in all time slots.

RECEIVE PRBS MODE SELECT Table 11-2

RPRBS1 (CCR5.1)	RPBRS0 (CCR5.0)	MODE
0	0	**Mode 0**: Normal (PRBS disabled),
0	1	**Mode 1**: PRBS in TSx. PRBS pattern is received in a single time slot (TS). In this mode the Receive Channel Monitor select bits in register CCR4 are used to select a time slot in which to receive the PRBS pattern.
1	0	**Mode 2**: PRBS in all but TS0. PRBS pattern is received in time slots 1 through 31.
1	1	**Mode 3**: PRBS unframed. PRBS pattern is received in all time slots.

12. SYSTEM CLOCK INTERFACE

A single System Clock Interface (SCI) is common to all four transceivers on the DS21Q50. The SCI is designed to allow any one of the four receivers to act as the master reference clock for the system. When multiple DS21Q50s are used to build an N port system, the SCI will allow any one of the N ports to be the master. The selected reference is then distributed to the other DS21Q50s via the REFCLK pin. The REFCLK pin acts as an output on the DS21Q50, which has been selected to provide the reference clock from one of its four receivers. On DS21Q50s not selected to source the reference clock, this pin becomes an input by writing zeros to the SCSx bits. The reference clock is also passed to the clock synthesizer PLL to generate a 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz clock. This clock can then be used with the IBO function in order to merge up to eight E1 lines on to a single high-speed PCM bus. In the event that the master E1 port fails (enters a Receive Carrier Loss condition) that port will automatically switch to the clock present on the MCLK pin. Therefore, MCLK acts as the backup source of master clock. The host can then find and select a functioning E1 port as the master. Because the selected port's clock is passed to the other DS21Q50s in a multiple device configuration, one DS21Q50's synthesizer can always be the source of the high-speed clock. This allows smooth transitions when clock source switching occurs. The System Clock Interface Control register exists in transceiver #1 only. (TS0, TS1 = 0)

Register Name: **SCICR**
Register Description: **System Clock Interface Control Register** (Note: This register is valid only for transceiver #1 (TS0 = 0, TS1 = 0.)
Register Address: **1D Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	AJACKE	BUCS	SOE	CSS1	CSS0	SCS2	SCS1	SCS0

SYMBOL	BIT	NAME AND DESCRIPTION
AJACKE	7	**AJACK Enable.** This bit enables the Alternate Jitter Attenuator.
BUCS	6	**Back-Up Clock Select.** Selects which clock source to switch to automatically during a Loss Of Transmit Clock event. 0 = During a LOTC event, switch to MCLK 1 = During a LOTC event, switch to system reference clock
SOE	5	**Synthesizer Output Enable.** 0 = 2/4/8/16MCK pin in high-z mode 1 = 2/4/8/16MCK pin active
CSS1	4	**Clock Synthesizer Select Bit 1.** See *Clock Synthesizer Output* table below.
CSS0	3	**Clock Synthesizer Select Bit 0.** See *Clock Synthesizer Output* table below.
SCS2	2	**System Clock Select Bit 2.** See *System Clock Select* table below.
SCS1	1	**System Clock Select Bit 1.** See *System Clock Select* table below.
SCS0	0	**System Clock Select Bit 0.** See *System Clock Select* table below.

MASTER PORT SELECTION Table 12-1

SCS2	SCS1	SCS0	PORT SELECTED AS MASTER
0	0	0	None (Master Port may be derived from another DS21Q50 in the system)
0	0	1	Transceiver #1
0	1	0	Transceiver #2
0	1	1	Transceiver #3
1	0	0	Transceiver #4
1	0	1	Reserved for future use
1	1	0	Reserved for future use
1	1	1	Reserved for future use

SYNTHESIZER OUTPUT SELECT Table 12-2

CSS1	CSS0	SYNTHESIZER OUTPUT FREQUENCY (MHz)
0	0	2.048
0	1	4.096
1	0	8.192
1	1	16.384

13. TRANSMIT CLOCK SOURCE

Depending on the operating mode of the DS21Q50, the Transmit Clock can be derived from different sources. In a basic configuration, where the IBO function is disabled, the transmit clock is normally sourced from the TCLK pin. In this mode a 2.048MHz clock with ±50ppm accuracy is applied to the TCLK pin. If the signal at TCLK is lost, the DS21Q50 will automatically switch to either the system reference clock present on the REFCLK pin, or to the recovered clock off the same port depending on which source the host at assigned as the backup clock. At the same time the host can be notified of the loss of transmit clock via an interrupt. The host can at any time force a switch over to one of the two backup clock sources regardless of the state of the TCLK pin.

When the IBO function is enabled, the transmit clock must be synchronous to the system clock since slips are not allowed in the transmit direction. In this mode, the TCLK pin is ignored and a transmit clock is automatically provided by the IBO circuit by dividing the clock present on the SYSCLK pin by 2, 4, or 8. In this configuration, if the signal present on the SYSCLK pin is lost, the DS21Q50 will automatically switch to either the system reference clock or to the recovered clock off the same port depending on which source the host at assigned as the backup clock. The host can at any time force a switchover to one of the two backup clock sources regardless of the state of the SYSCLK pin.

14. IDLE CODE INSERTION

The Transmit Idle Registers (TIR1/2/3/4) determine which of the 32 E1 channels should be overwritten with the code placed in the Transmit Idle Definition Register (TIDR). This allows the same 8-bit code to be placed into any of the 32 E1 channels.

Each of the bit positions in the Transmit Idle Registers represents a DS0 channel in the outgoing frame. When these bits are set to a one, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR).

Register Name: **TIR1, TIR2, TIR3, TIR4**
Register Description: **Transmit Idle Registers**
Register Address: **24 Hex, 25 Hex, 26 Hex, 27 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
SYM	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
SYM	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
SYM	CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25

SYMBOLS	BIT	NAME AND DESCRIPTION
CH1 to CH32	TIR1.0 to 4.7	**Transmit Idle Code Insertion Control Bits.** 0 = do not insert the Idle Code in the TIDR into this channel 1 = insert the Idle Code in the TIDR into this channel

Register Name: **TIDR**
Register Description: **Transmit Idle Definition Register**
Register Address: **23 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOL	BIT	NAME AND DESCRIPTION
TIDR7	7	MSB of the Idle Code (this bit is transmitted first)
TIDR6	6	
TIDR5	5	
TIDR4	4	
TIDR3	3	
TIDR2	2	
TIDR1	1	
TIDR0	0	LSB of the Idle Code (this bit is transmitted last)

15. PER-CHANNEL LOOPBACK

The DS21Q50 has per-channel loopback capability that can operate in one of two modes: Remote Per-Channel Loopback or Local Per-Channel Loopback. PCLB1/2/3/4 are used for both modes to determine which channels will be looped back. In Remote Per-Channel Loopback mode, PCLB1/2/3/4 will determine which channels (if any) in the transmit direction should be replaced with the data from the receiver or in other words, off of the E1 line. In Local Per-Channel Loop Back mode, PCLB1/2/3/4 will determine which channels (if any) in the receive direction should be replaced with the data from the transmit. If either mode is enabled, then transmit and receive clocks and frame syncs must be synchronized. There are no restrictions on which channels can be looped back or on how many channels can be looped back.

Register Name: **PCLB1, PCLB2, PCLB3, PCLB4**
Register Description: **Per-Channel Loopback Registers**
Register Address: **2B Hex, 2C Hex, 2D Hex, 2E Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
SYM	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
SYM	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17
SYM	CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25

SYMBOLS	BIT	NAME AND DESCRIPTION
CH1 to CH32	PCLB1.0 to 4.7	**Per-Channel Loopback Control Bits.** 0 = do not loopback this channel 1 = loopback this channel

16. ELASTIC STORE OPERATION

The DS21Q50 contains a two-frame (512 bits) elastic store for the receive direction. The elastic store is used to absorb the differences in frequency and phase between the E1 data stream and an asynchronous (i.e., not frequency locked) backplane clock that can be 2.048MHz for normal operation or 4.096MHz, 8.192MHz, or 16.384MHz when using the Interleave Bus Option. The elastic store contains full controlled slip capability.

If the receive elastic store is enabled (RCR.4 = 1), then the user must provide a 2.048MHz clock to the SYSCLK pin. If the IBO function is enabled then a 4.096MHz, 8.192MHz, or 16.384MHz clock must be provided at the SYSCLK pin. The user has the option of either providing a frame/multiframe sync at the RSYNC pin (RCR.5 = 1) or having the RSYNC pin provide a pulse on frame/multiframe boundaries (RCR.5 = 0). If the user wishes to obtain pulses at the frame boundary, then RCR1.6 must be set to zero and if the user wishes to have pulses occur at the multiframe boundary, then RCR1.6 must be set to one. If the elastic store is enabled, then either CAS (RCR.7 = 0) or CRC4 (RCR.7 = 1) multiframe boundaries will be indicated via the RSYNC output. See Section 22.1 for timing details. If the 512-bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (256-bits) will be repeated at RSER and the SR1.4 and RIR.3 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR.4 bits will be set to a one.

17. ADDITIONAL (SA) AND INTERNATIONAL (SI) BIT OPERATION

On the receiver, the RAF and RNAF registers will always report the data as it received in the Additional and International bit locations. The RAF and RNAF registers are updated with the setting of the Receive Align Frame bit in Status Register 2 (SR2.6). The host can use the SR2.6 bit to know when to read the RAF and RNAF registers. It has 250µs to retrieve the data before it is lost.

On the transmitter, data is sampled from the TAF and TNAF registers with the setting of the Transmit Align Frame bit in Status Register 2 (SR2.3). The host can use the SR2.3 bit to know when to update the TAF and TNAF registers. It has 250µs to update the data or else the old data will be retransmitted. Data in the Si bit position will be overwritten if either the framer is programmed: (1) to source the Si bits from the TSER pin, (2) in the CRC4 mode, or (3) have automatic E-bit insertion enabled. Data in the Sa bit position will be overwritten if any of the TCR.3 to TCR.7 bits are set to one. Please see the register descriptions for TCR for more details.

Register Name: **RAF**
Register Description: **Receive Align Frame Register**
Register Address: **28 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	Si	0	0	1	1	0	1	1

SYMBOL	BIT	NAME AND DESCRIPTION
Si	7	**International Bit.**
0	6	**Frame Alignment Signal Bit.**
0	5	**Frame Alignment Signal Bit.**
1	4	**Frame Alignment Signal Bit.**
1	3	**Frame Alignment Signal Bit.**
0	2	**Frame Alignment Signal Bit.**
1	1	**Frame Alignment Signal Bit.**
1	0	**Frame Alignment Signal Bit.**

Register Name: **RNAF**
Register Description: **Receive Nonalign Frame Register**
Register Address: **29 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	BIT	NAME AND DESCRIPTION
Si	7	**International Bit.**
1	6	**Frame Nonalignment Signal Bit.**
A	5	**Remote Alarm.**
Sa4	4	**Additional Bit 4.**
Sa5	3	**Additional Bit 5.**
Sa6	2	**Additional Bit 6.**
Sa7	1	**Additional Bit 7.**
Sa8	0	**Additional Bit 8.**

Register Name: **TAF**
Register Description: **Transmit Align Frame Register**
Register Address: **20 Hex**
(Must be programmed with the seven bit FAS word; the DS21Q50 does not automatically set these bits.)

Bit #	7	6	5	4	3	2	1	0
Name	Si	0	0	1	1	0	1	1

SYMBOL	BIT	NAME AND DESCRIPTION
Si	7	**International Bit.**
0	6	**Frame Alignment Signal Bit.** Set this bit = 0.
0	5	**Frame Alignment Signal Bit.** Set this bit = 0.
1	4	**Frame Alignment Signal Bit.** Set this bit = 1.
1	3	**Frame Alignment Signal Bit.** Set this bit = 1.
0	2	**Frame Alignment Signal Bit.** Set this bit = 0.
1	1	**Frame Alignment Signal Bit.** Set this bit = 1.
1	0	**Frame Alignment Signal Bit.** Set this bit = 1.

Register Name: **TNAF**
Register Description: **Transmit Nonalign Frame Register**
Register Address: **21 Hex**
(Bit 6 must be programmed to one; the DS21Q50 does not automatically set this bit)

Bit #	7	6	5	4	3	2	1	0
SYM	Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	BIT	NAME AND DESCRIPTION
Si	7	**International Bit.**
1	6	**Frame Nonalignment Signal Bit.** Set this bit = 1.
A	5	**Remote Alarm (used to transmit the alarm).**
Sa4	4	**Additional Bit 4.**
Sa5	3	**Additional Bit 5.**
Sa6	2	**Additional Bit 6.**
Sa7	1	**Additional Bit 7.**
Sa8	0	**Additional Bit 8.**

18. USER-CONFIGURABLE OUTPUTS

There are two user configurable output pins for each transceiver, OUTA and OUTB. These pins can be programmed to output various clocks, alarms for line monitoring, logic 0 and 1 levels to control external circuitry or access transmit data between the framer and transmit line interface unit. OUTA and OUTB can be active low or active high when operating as clock and alarm outputs. OUTA is active high if OUTAC.4 =1, and active low if OUTAC.3 = 0. OUTB is active high if OUTBC.4 = 1, and active low if OUTBC.4 = 0 (Table 18-1). For controlling external circuitry, mode 0000 is selected. In this configuration, the OUTA pin will follow OUTAC.4 and the OUTB pin will follow OUTBC.4.

The OUTAC register also contains a control bit for CMI operation. Please see Section 19 for details on CMI operation.

Register Name: **OUTAC**
Register Description: **OUTA Control Register**
Register Address: **1A Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	TTLIE	CMII	CMIE	OA4	OA3	OA2	OA1	OA0

SYMBOL	BIT	NAME AND DESCRIPTION
TTLIE	7	**TTL Input Enable.** When this bit is set, the receiver can accept TTL positive and negative data at the RTIP and RRING inputs. The data is clocked in on the falling edge of MCLK.
CMII	6	**CMI Invert.** See Section 20 for details. 0 = CMI input data not inverted 1 = CMI input data inverted
CMIE	5	**CMI Enable.** See Section 20 for details. 0 = CMI disabled 1 = CMI enabled
OA4	4	**OUTA Control Bit 4.** Inverts OUTA output
OA3	3	**OUTA Control Bit 3.** See Table 18-1 for details.
OA2	2	**OUTA Control Bit 2.** See Table 18-1 for details.
OA1	1	**OUTA Control Bit 1.** See Table 18-1 for details.
OA0	0	**OUTA Control Bit 0.** See Table 18-1 for details.

Register Name: **OUTBC**
Register Description: **OUTB Control Register**
Register Address: **1B Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	NRZE	-	-	OB4	OB3	OB2	OB1	OB0

SYMBOL	BIT	NAME AND DESCRIPTION
NRZE	7	**NRZ Enable.** When this bit is set, the receiver can accept TTL type NRZ data at the RTIP input. RRING becomes a clock input. 0 = RTIP and RRING are in normal mode 1 = RTIP becomes an NRZ TTL type input and RRING is its associated clock input. Data at RTIP is clocked in on the falling edge of the clock present on RRING.
-	6	**Unused.** Should Be set = 0 for proper operation.
-	5	**Unused.** Should Be set = 0 for proper operation.
OB4	4	**OUTB Control Bit 4.** Inverts OUTB output.
OB3	3	**OUTB Control Bit 3.**
OB2	2	**OUTB Control Bit 2.**
OB1	1	**OUTB Control Bit 1.**
OB0	0	**OUTB Control Bit 0.**

OUTA AND OUTB FUNCTION SELECT Table 18-1

OA3 OB3	OA2 OB2	OA1 OB1	OA0 OB0	FUNCTION
0	0	0	0	**External Hardware Control Bit**. In this mode OUTA and OUTB can be used as simple control pins for external circuitry. Use OA4 and OB4 to toggle OUTA and OUTB.
0	0	0	1	**RCLK**. Receive Recovered Clock
0	0	1	0	**Receive Loss Of Sync Indicator**. Real-time hardware version of SR1.0 (Table 18-1).
0	0	1	1	**Receive Loss Of Carrier Indicator**. Real-time hardware version of SR1.1 (Table 18-1).
0	1	0	0	**Receive Remote Alarm Indicator**. Real-time hardware version of SR1.2 (Table 18-1).
0	1	0	1	**Receive Unframed All Ones Indicator**. Real-time hardware version of SR1.3 (Table 18-1)
0	1	1	0	**Receive Slip Occurrence Indicator**. One clock wide pulse for every slip of the receive elastic store. Hardware version of SR1.4.
0	1	1	1	**Receive CRC Error Indicator**. One clock wide pulse for every multiframe that contains a CRC error. Output forced to 0 during loss of sync.
1	0	0	0	**Loss Of Transmit Clock Indicator**. Real-time hardware version SR2.2 (Table 18-1).
1	0	0	1	**RFSYNC**. Recovered frame sync pulse.
1	0	1	0	**PRBS Bit Error**. A half clock wide pulse for every bit error in the received PRBS pattern.
1	0	1	1	**TDATA/RDATA**. OUTB will output an NRZ version of the transmit data stream

				(TDATA) prior to the transmit line interface. OUTA will output the received serial data stream (RDATA) prior to the Elastic Store.
1	1	0	0	**Receive CRC4 Multiframe Sync**. Recovered CRC4 MF sync pulse.
1	1	0	1	**Receive CAS Multiframe Sync.** Recovered CAS MF sync pulse.
1	1	1	0	**Transmit Current Limit.** Real-time indicator that the TTIP and TRING outputs have reached their 50ma current limit.
1	1	1	1	**TPOS/TNEG Output**. This mode outputs the AMI/HDB3 encoded transmit data. OUTA will output TNEG data. OUTB will output TPOS data.

19. LINE INTERFACE UNIT

The line interface unit in the DS21Q50 contains three sections: the receiver, which handles clock and data recovery; the transmitter, which waveshapes and drives the E1 line; and the jitter attenuator. The Line Interface Control Register (LICR), described below, controls each of these three sections.

Register Name: **LICR**
Register Description: **Line Interface Control Register**
Register Address: **17 Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	L2	L1	L0	EGL	JAS	JABDS	DJA	TPD

SYMBOL	BIT	NAME AND DESCRIPTION
L2	7	**Line Build Out Select Bit 2.** Sets the transmitter build out.
L1	6	**Line Build Out Select Bit 1.** Sets the transmitter build out.
L0	5	**Line Build Out Select Bit 0.** Sets the transmitter build out.
EGL	4	**Receive Equalizer Gain Limit.** 0 = -12dB 1 = -43dB
JAS	3	**Jitter Attenuator Select.** 0 = place the jitter attenuator on the receive side 1 = place the jitter attenuator on the transmit side
JABDS	2	**Jitter Attenuator Buffer Depth Select.** 0 = 128 bits 1 = 32 bits (use for delay sensitive applications)
DJA	1	**Disable Jitter Attenuator.** 0 = jitter attenuator enabled 1 = jitter attenuator disabled
TPD	0	**Transmit Power Down.** 0 = powers down the transmitter and 3-states the TTIP and TRING pins 1 = normal transmitter operation

19.1 Receive Clock and Data Recovery

The DS21Q50 contains a digital clock recovery system. See Figure 4-1 and Figure 19-1 for more details. The device couples to the receive E1 shielded twisted pair or COAX via a 1:1 transformer (Table 19-2). The 2.048MHz clock attached at the MCLK pin is internally multiplied by 16 via an internal PLL and fed to the clock recovery system. The clock recovery system uses the clock from the PLL circuit to form a 16 times over-sampler, which is used to recover the clock and data. This over-sampling technique offers outstanding jitter tolerance (Figure 19-4).

Normally, RCLK is the recovered clock from the E1 AMI/HDB3 waveform presented at the RTIP and RRING inputs. When no AMI signal is present at RTIP and RRING, a Receive Carrier Loss (RCL) condition will occur and the RCLK will be sourced from the clock applied at the MCLK pin. If the jitter attenuator is either placed in the transmit path or is disabled, RCLK can exhibit slightly shorter high cycles of the clock. This is due to the highly over-sampled digital clock recovery circuitry. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to being close to 50% duty cycle. See the *Receive AC Timing Characteristics* in Section 24.4 for more details.

19.1.1 Termination

The DS21Q50 is designed to be fully software-selectable for 75O and 120O termination without the need to change any external resistors. The user can configure the DS21Q50 for 75O or 120O receive termination by setting the IRTSEL (CCR5.4) bit. When using the internal termination feature, the external termination resistance should be120O (typically two 60O resistors). Setting IRTSEL = 1 will cause the DS21Q50 to internally apply parallel resistance to the external resistors in order to adjust the termination to 75O. See Figure 19-2 for details.

19.2 Transmit Waveshaping and Line Driving

The DS21Q50 uses a set of laser–trimmed delay lines along with a precision digital-to-analog converter (DAC) to create the waveforms that are transmitted onto the E1 line. The waveforms meet the ITU G.703 specifications (Figure 19-3). The user will select which waveform is to be generated by properly programming the L2/L1/L0 bits in the Line Interface Control Register (LICR). The DS21Q50 can set up in a number of various configurations depending on the application (Table 19-1).

LINE BUILD OUT SELECT IN LICR Table 19-1

L2	L1	L0	APPLICATION	TRANSFORMER	RETURN LOSS*	RT**(O)
0	0	0	75O normal	1:2 stepup	NM	0
0	0	1	120O normal	1:2 stepup	NM	0
0	1	0	75O w/ protection resistors	1:2 stepup	NM	2.5
0	1	1	120O w/ protection resistors	1:2 stepup	NM	2.5
1	0	0	75O w/ high return loss	1:2 stepup	21dB	6.2
1	0	1	120O w/ high return loss	1:2 stepup	21dB	11.6

* NM = Not Meaningful (Return Loss value too low for significance)

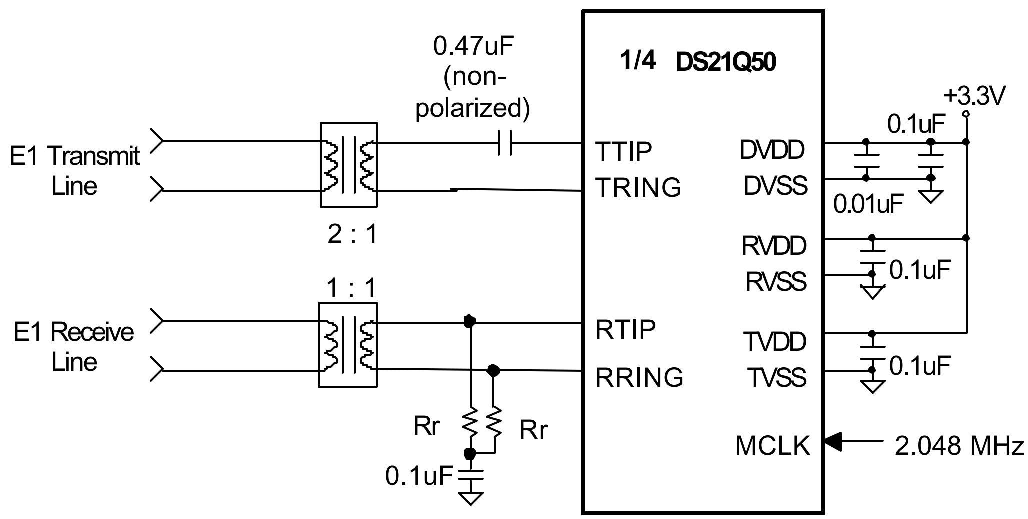
** See separate application note for details on E1 line interface design

Due to the nature of the design of the transmitter in the DS21Q50, very little jitter (less then 0.005 UIpp broadband from 10Hz to 100kHz) is added to the jitter present on TCLK (or source used for transmit clock). Also, the waveform created is independent of the duty cycle of TCLK. The transmitter in the device couples to the E1 transmit shielded twisted pair or COAX via a 1:2 stepup transformer as shown in Figure 19-1. In order for the devices to create the proper waveforms, the transformer used must meet the specifications listed in Table 19-2. The line driver in the device contains a current limiter that will prevent more than 50mA (RMS) from being sourced in a 1O load.

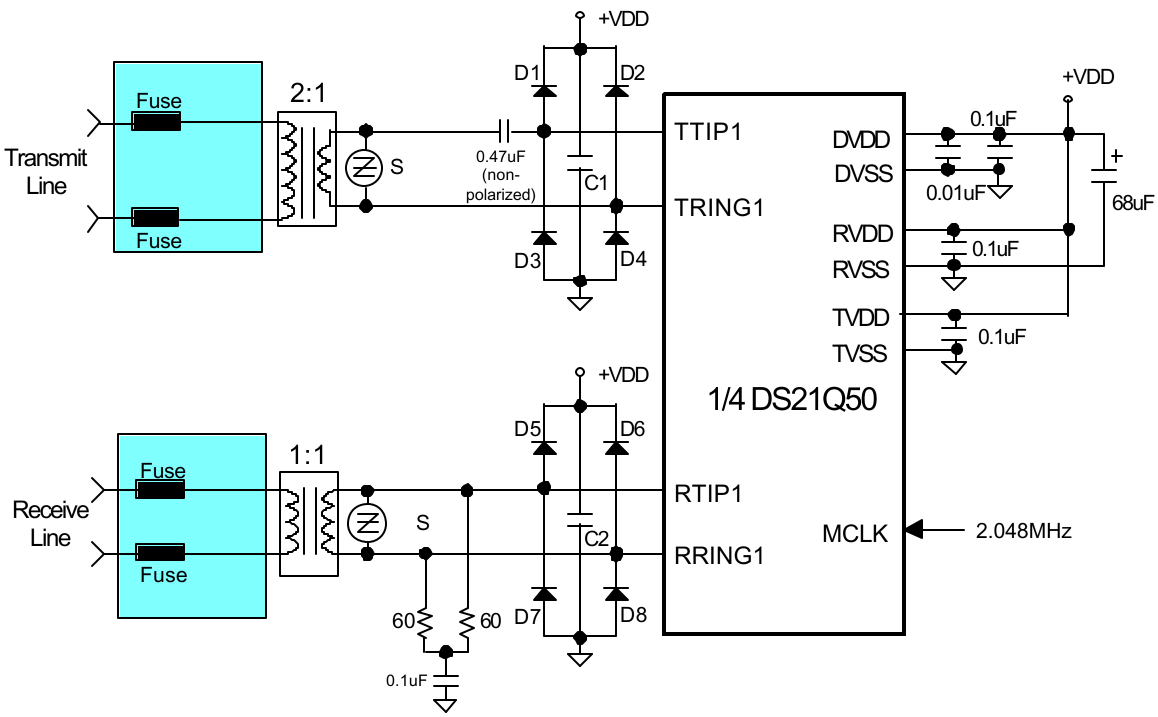
TRANSFORMER SPECIFICATIONS Table 19-2

SPECIFICATION	RECOMMENDED VALUE
Turns Ratio	1:1 (receive) and 1:2 (transmit) ±3%
Primary Inductance	600µH minimum
Leakage Inductance	1.0µH maximum
Intertwining Capacitance	40pF maximum
DC Resistance	1.2O maximum

EXTERNAL ANALOG CONNECTIONS (BASIC CONFIGURATION) Figure 19-1



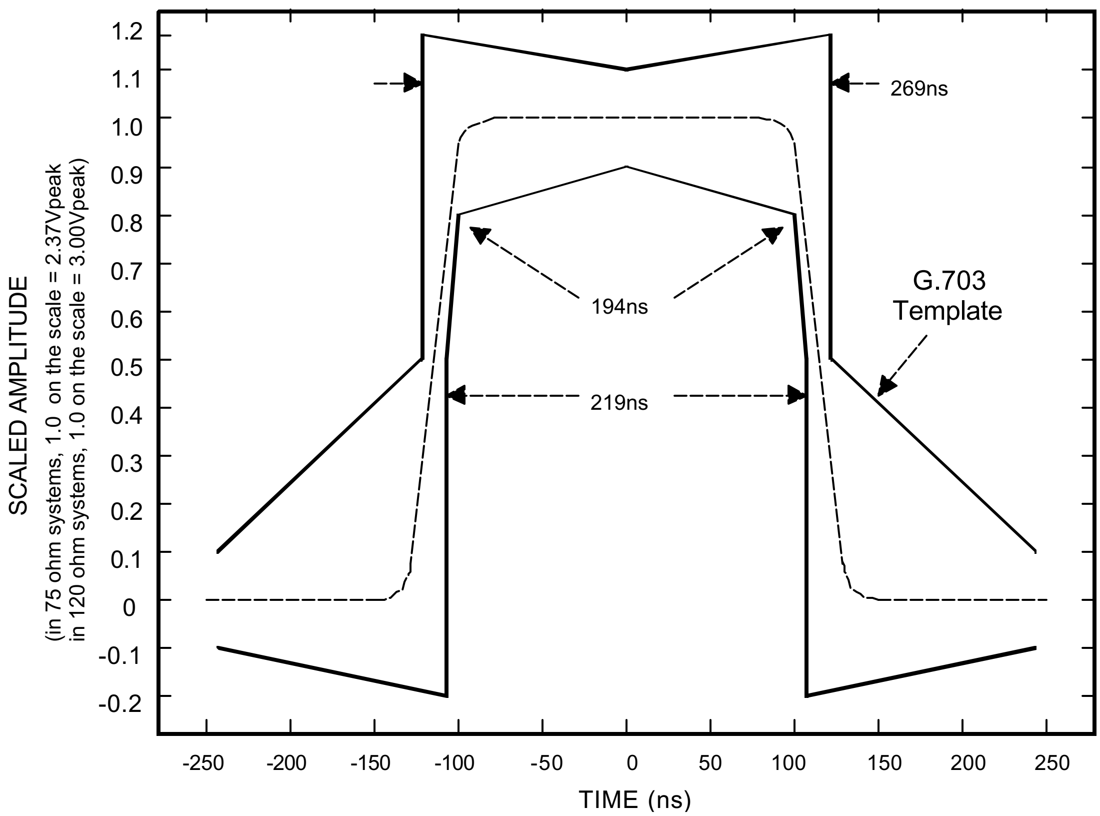
EXTERNAL ANALOG CONNECTIONS (PROTECTED INTERFACE) Figure 19-2



NOTES:

1) All resistor values are ±1%.
2) C1 = C2 = 0.1µ.
3) S is a 6V transient suppressor.
4) D1 to D8 are Schottky diodes.
5) The fuses are optional to prevent AC power line crosses from compromising the transformers.
6) The 68µF is used to keep the local power plane potential within tolerance during a surge.

TRANSMIT WAVEFORM TEMPLATE Figure 19-3



19.3 Jitter Attenuators

The DS21Q50 contains an onboard clock and data jitter attenuator for each transceiver and a single, undedicated "clock only" jitter attenuator. This undedicated jitter attenuator is shown in the block diagram of Figure 4-1 as the Alternate Jitter Atteunator.

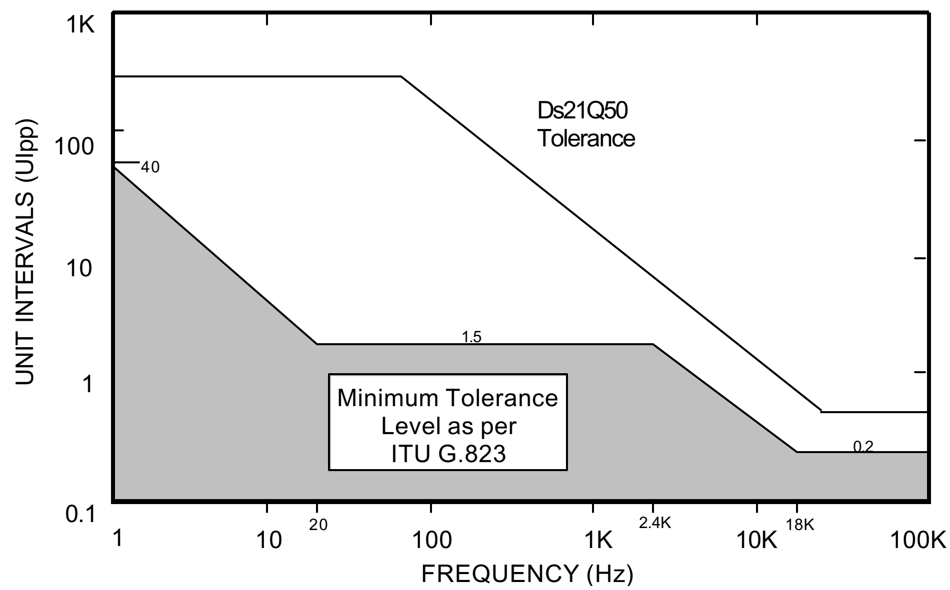
19.3.1 Clock and Data Jitter Attenuators

The clock and data jitter attenuators can be mapped into the receive or transmit paths and can be set to buffer depths of either 32 or 128 bits via the Line Interface Control Register (LICR). The 128–bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay sensitive applications. The characteristics of the attenuators are shown in . The jitter attenuators can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit in the LICR. Also, the jitter attenuator can be disabled (in effect, removed) by setting the DJA bit in the LICR. In order for the jitter attenuator to operate properly, a 2.048MHz clock (±50ppm) must be applied at the MCLK pin. Onboard circuitry adjusts either the recovered clock from the clock/data recovery block or the clock applied at the TCLKI pin to create a smooth jitter free clock that is used to clock data out of the jitter attenuator FIFO. It is acceptable to provide a gapped/bursty clock at the TCLKI pin if the jitter attenuator is placed on the transmit side. If the incoming jitter exceeds either 120 UIpp (buffer depth is 128 bits) or 28 UIpp (buffer depth is 32 bits), then the DS21Q50 will divide the internal nominal 32.768MHz clock by either 15 or 17 instead of the normal 16 to keep the buffer from overflowing. When the device divides by either 15 or 17, it also sets the Jitter Attenuator Limit Trip (JALT) bit in the Receive Information Register (RIR.5).

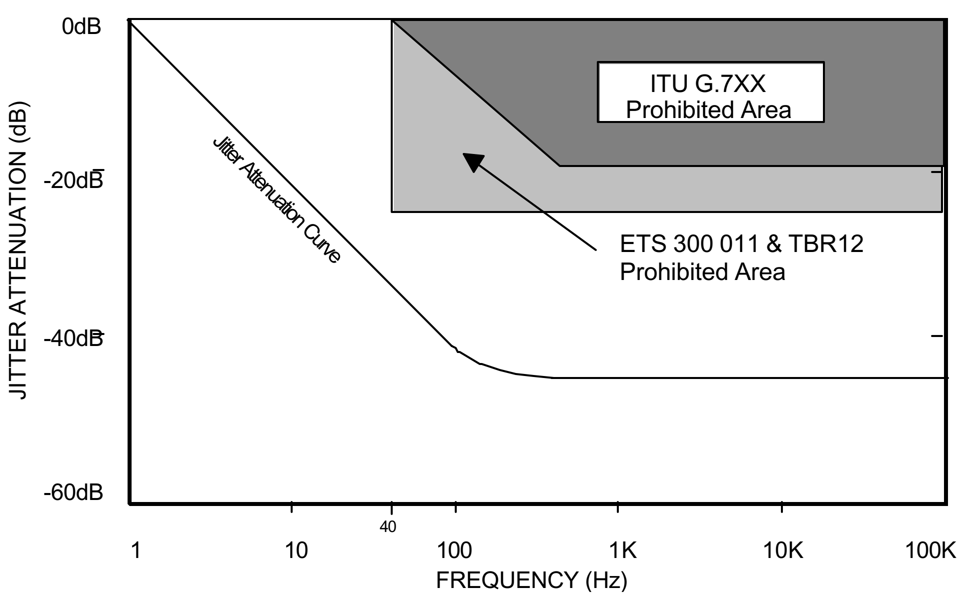
19.3.2 Undedicated Clock Jitter Attenuator

The undedicated jitter attenuator is useful for preparing a user-supplied clock for use as a transmission clock (TCLK). AJACKI is the input pin and AJCAKO is the output pin. Clocks generated by certain types of PLL or other synthesizers may contain too much jitter to be appropriate for transmission. Network requirements limit the amount of jitter that may be transmitted onto the network. This feature is enabled by setting SC1CR.7 = 1 in transceiver #1.

JITTER TOLERANCE Figure 19-4



JITTER ATTENUATION Figure 19-5



20. CMI (CODE MARK INVERSION)

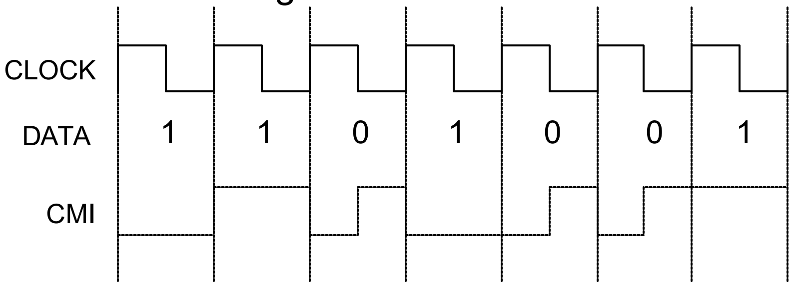
The DS21Q50 provides a CMI interface for connection to optical transports. This interface is a unipolar 1T2B coded signal. Ones are alternately encoded as a logical one or zero level for the full duration of the clock period. Zeros are encode as a zero to one transition at the middle of the clock period. Figure 20-1 shows an example data pattern and its CMI result. The control bit for enabling CMI is in the OUTAC register as shown below.

Register Name: **OUTAC** (Reproduced here for clarity)
Register Description: **OUTA CONTROL REGISTER**
Register Address: **1A Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	TTLIE	CMII	CMIE	OA4	OA3	OA2	OA1	OA0

SYMBOL	BIT	NAME AND DESCRIPTION
TTLIE	7	**TTL Input Enable.** When this bit is set, the receiver can accept TTL positive and negative data at the RTIP and RRING inputs. The data is clocked in on the falling edge of MCLK.
CMII	6	**CMI Invert.** 0 = CMI input data not inverted 1 = CMI input data inverted
CMIE	5	**Transmit and Receive CMI Enable.** 0 = Transmit and Receive line interface operates in normal AMI/HDB3 mode 1 = Transmit and Receive line interface operate in CMI mode. TTIP is CMI output and RTIP is CMI input. In this mode of operation TRING and RRING are no-connects.
OA4	4	**OUTA Control Bit 4.** Inverts OUTA output.
OA3	3	**OUTA Control Bit 3.** See Table 18-1 for details.
OA2	2	**OUTA Control Bit 2.** See Table 18-1 for details.
OA1	1	**OUTA Control Bit 1.** See Table 18-1 for details.
OA0	0	**OUTA Control Bit 0.** See Table 18-1 for details.

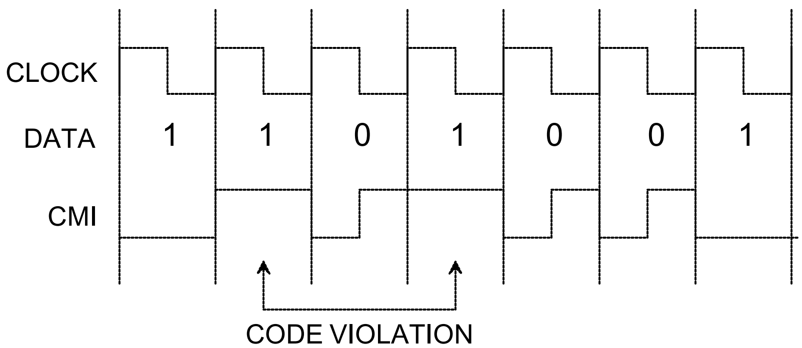
CMI CODING Figure 20-1



Transmit and Receive CMI is enabled via OUTAC.7. When this register bit is set, the TTIP pin will output CMI coded data at normal TTL type levels. This signal can be used to directly drive an optical interface. When CMI is enabled, the user may also use HDB3 coding.

When this register bit is set, the RTIP pin will become a unipolar CMI input. The CMI signal will be processed to extract and align the clock with data. The BiPolar code violation counter will count CVs (Code Violations) in the CMI signal. CVs are defined as consecutive ones of the same polarity as shown in Figure 20-2. If HDB3 pre-coding is enabled then the CVs generated by HDB3 will not be counted as errors.

EXAMPLE OF CMI CODE VIOLATION (CV) Figure 20-2



21. INTERLEAVED PCM BUS OPERATION

In many architectures, the PCM outputs of individual framers are combined into higher speed PCM buses to simplify transport across the system backplane. The DS21Q50 can be configured to allow PCM data buses to be multiplexed into higher speed data buses eliminating external hardware, saving board space and cost. The DS21Q50 uses a channel interleave method. See Figure 22-4 and Figure 22-7 for details of the channel interleave.

The interleaved PCM bus option (IBO) supports three bus speeds. The 4.096MHz bus speed allows two PCM data streams to share a common bus. The 8.192MHz bus speed allows four PCM data streams to share a common bus. The 16.384MHz bus speed allows eight PCM data streams to share a common bus. See Figure 21-1 for an example of four transceivers sharing a common 8.192MHz PCM bus. The receive elastic stores of each transceiver must be enabled. Via the IBO register the user can configure each transceiver for a specific bus speed and position. For all IBO bus configurations each transceiver is assigned an exclusive position in the high speed PCM bus. When the device is configured for IBO operation, the TSYNCx pin should be configured as an output or as an input connected to ground. The user cannot supply a TSYNCx signal in this mode.

Register Name: **IBO**
Register Description: **INTERLEAVE BUS OPERATION REGISTER**
Register Address: **1C Hex**

Bit #	7	6	5	4	3	2	1	0
SYM	-	IBOTCS	SCS1	SCS0	IBOEN	DA2	DA1	DA0

SYMBOL	BIT	NAME AND DESCRIPTION
-	7	**Not Assigned.** Should be set to 0.
IBOTCS	6	**IBO Transmit Clock Source.** 0 = TCLK pin will be source of transmit clock 1 = Transmit clock will internally derived from the clock at the SYSCLK pin
SCS1	5	**System Clock Select Bit 1.** See Table 21-2.
SCS0	4	**System Clock Select Bit 0.** See Table 21-2.
IBOEN	3	**Interleave Bus Operation Enable** 0 = Interleave Bus Operation disabled. 1 = Interleave Bus Operation enabled.
DA2	2	**Device Assignment Bit 3.** See Table 21-1.
DA1	1	**Device Assignment Bit 2.** See Table 21-1.
DA0	0	**Device Assignment Bit 1.** See Table 21-1.

IBO DEVICE ASSIGNMENT Table 21-1

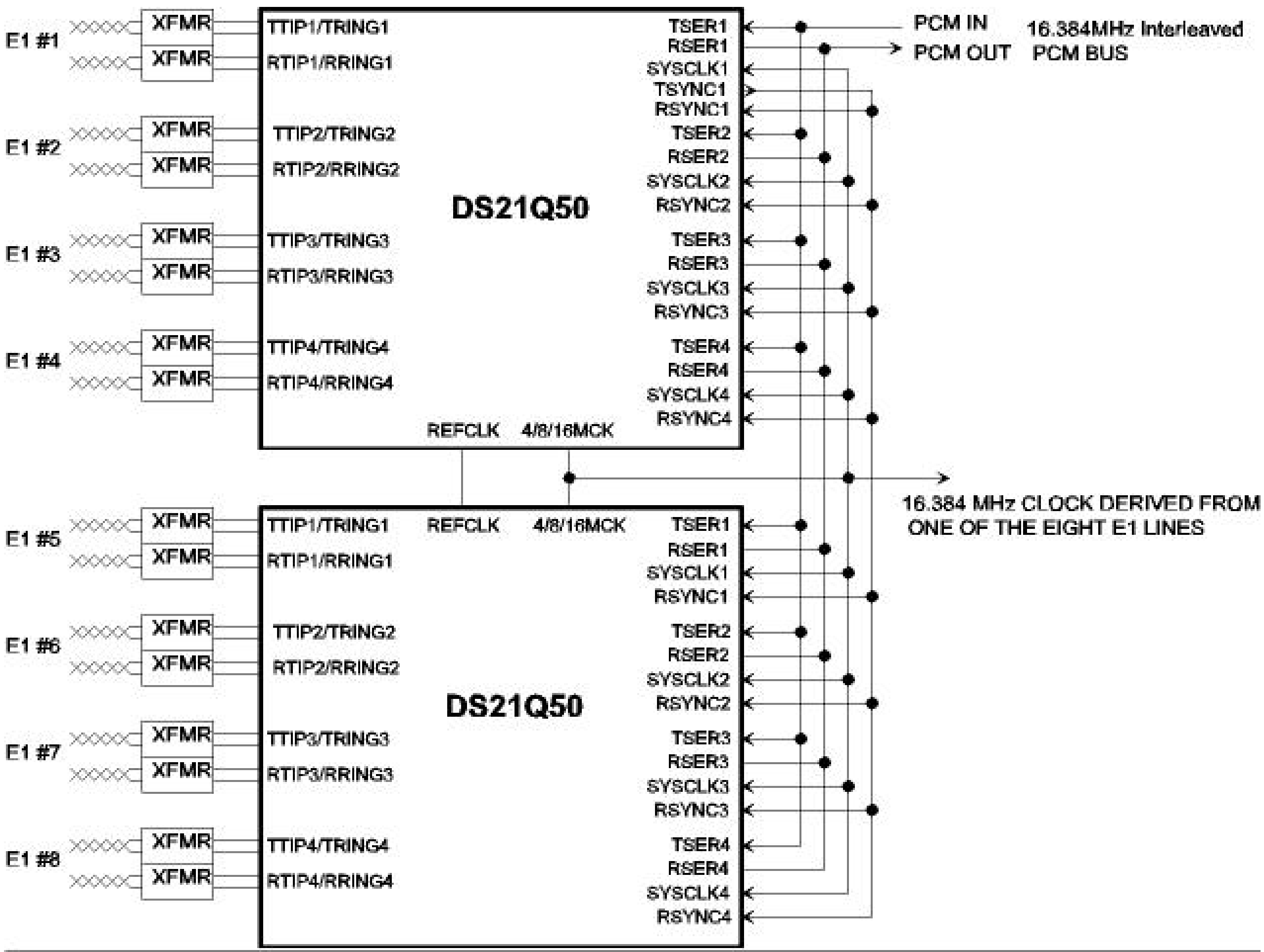
DA2	DA1	DA0	FUNCTION
0	0	0	1st Device on bus
0	0	1	2nd Device on bus
0	1	0	3rd Device on bus
0	1	1	4th Device on bus
1	0	0	5th Device on bus
1	0	1	6th Device on bus
1	1	0	7th Device on bus
1	1	1	8th Device on bus

IBO SYSTEM CLOCK SELECT Table 21-2

SCS1	SCS0	FUNCTION
0	0	2.048MHz, Single device on bus
0	1	4.096MHz, Two devices on bus
1	0	8.192MHz, Four devices on bus
1	1	16.384MHz, Eight devices on bus

IBO CONFIGURATION USING 2 DS21Q50 TRANSCEIVERS (8 E1 Lines)

Figure 21-1



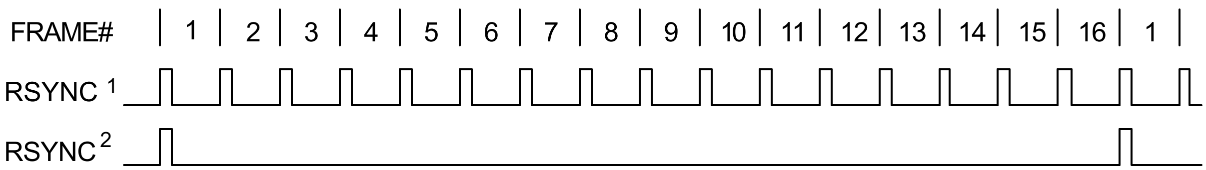
NOTE:

1) See Section 19 for details on Line Interface circuit.

22. FUNCTIONAL TIMING DIAGRAMS

22.1 Receive

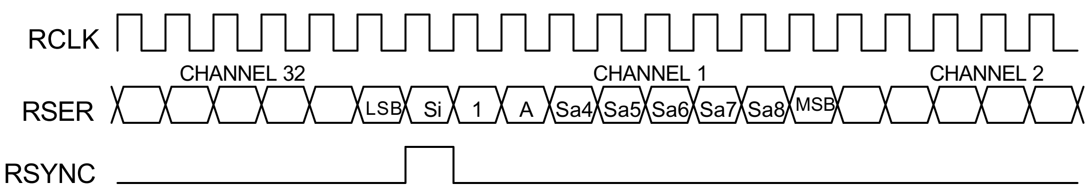
RECEIVE FRAME AND MULTIFRAME TIMING Figure 22-1



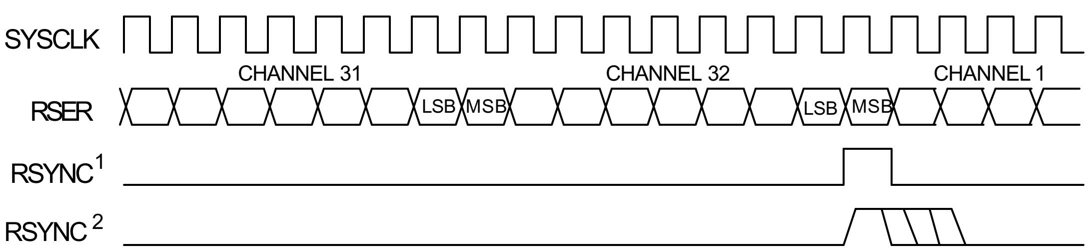
NOTES:

1) RSYNC in frame/output mode (RCR.6 = 0).
2) RSYNC in multiframe/output mode (RCR.6 = 1).
3) This diagram assumes the CAS MF begins in the RAF frame.

RECEIVE BOUNDARY TIMING (With Elastic Store Disabled) Figure 22-2



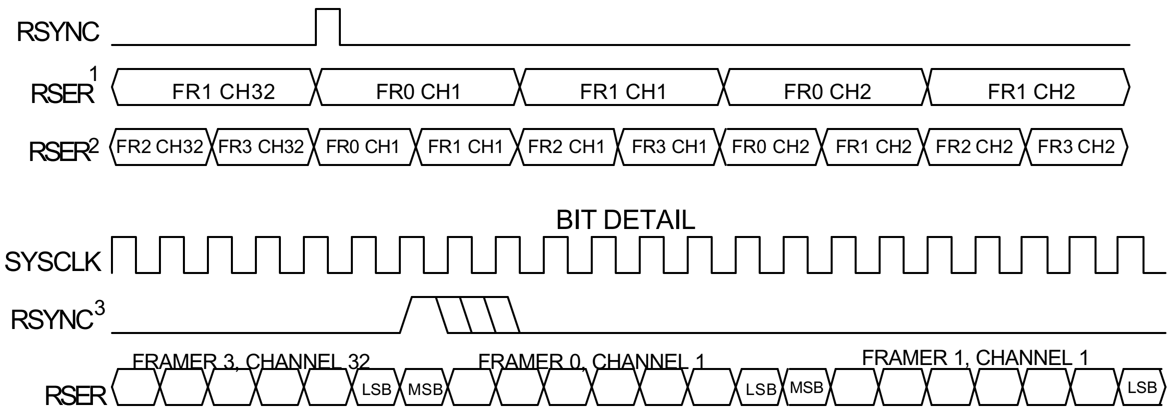
RECEIVE BOUNDARY TIMING (With Elastic Store Enabled) Figure 22-3



NOTES:

1) RSYNC is in the output mode (RCR.5 = 0).
2) RSYNC is in the input mode (RCR.5 = 1).

RECEIVE INTERLEAVE BUS OPERATION Figure 22-4

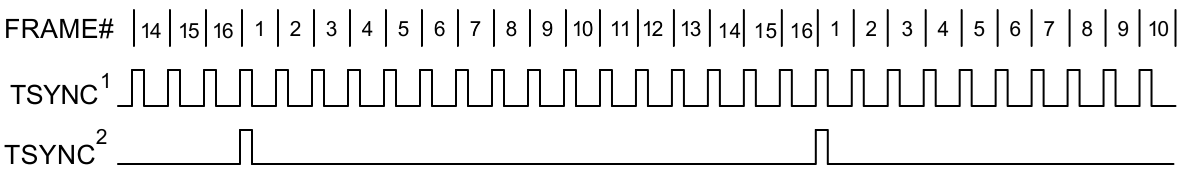


NOTES:

1) 4.096MHz bus configuration.
2) 8.192MHz bus configuration.
3) RSYNC is in the input mode (RCR.5 = 0).

22.2 Transmit

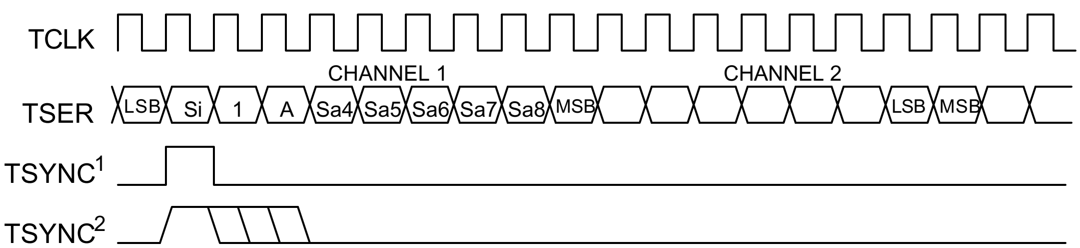
TRANSMIT FRAME AND MULTIFRAME TIMING Figure 22-5



NOTES:

1) TSYNC in frame mode (TCR.1 = 0).
2) TSYNC in multiframe mode (TCR.1 = 1).

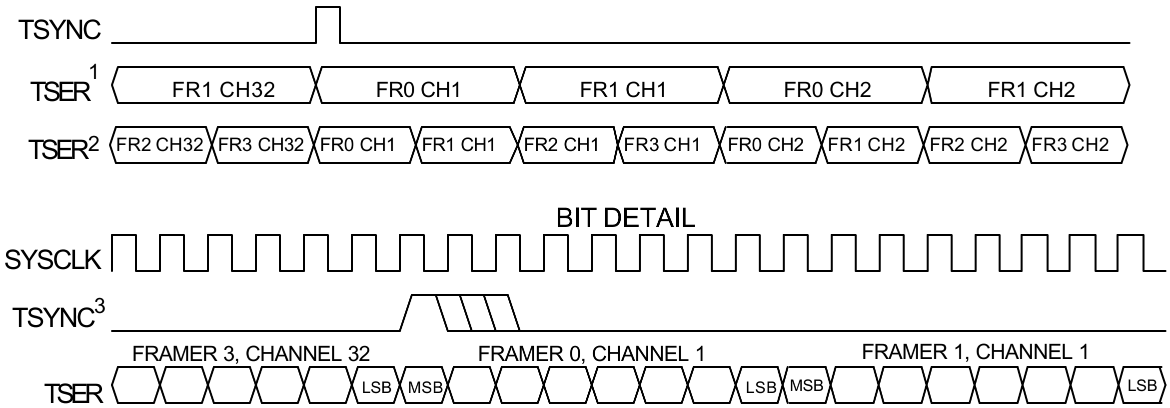
TRANSMIT BOUNDARY TIMING Figure 22-6



NOTES:

1) TSYNC is in the output mode (TCR.0 = 1).
2) TSYNC is in the input mode (TCR.0 = 0).

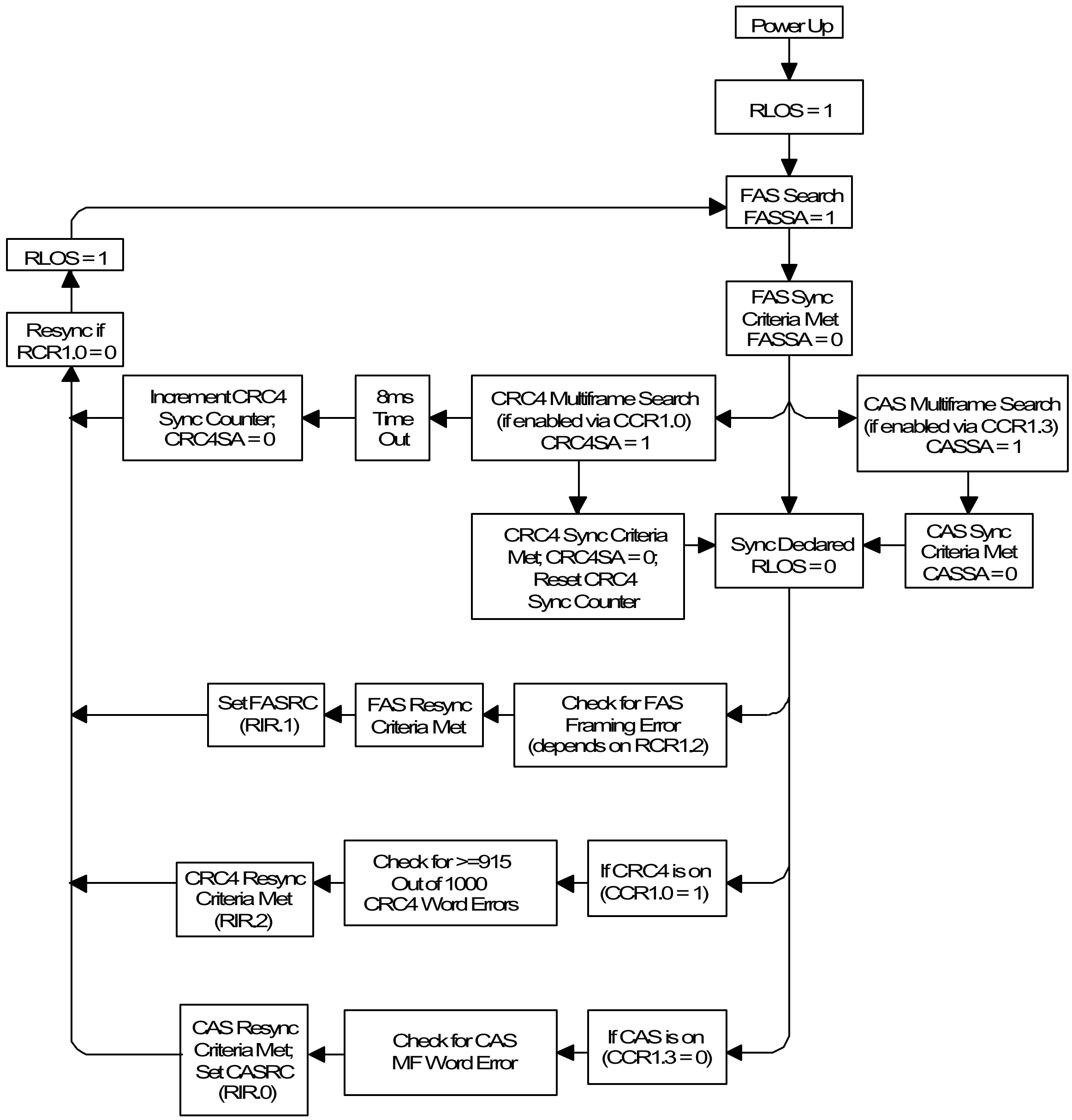
TRANSMIT INTERLEAVE BUS OPERATION Figure 22-7



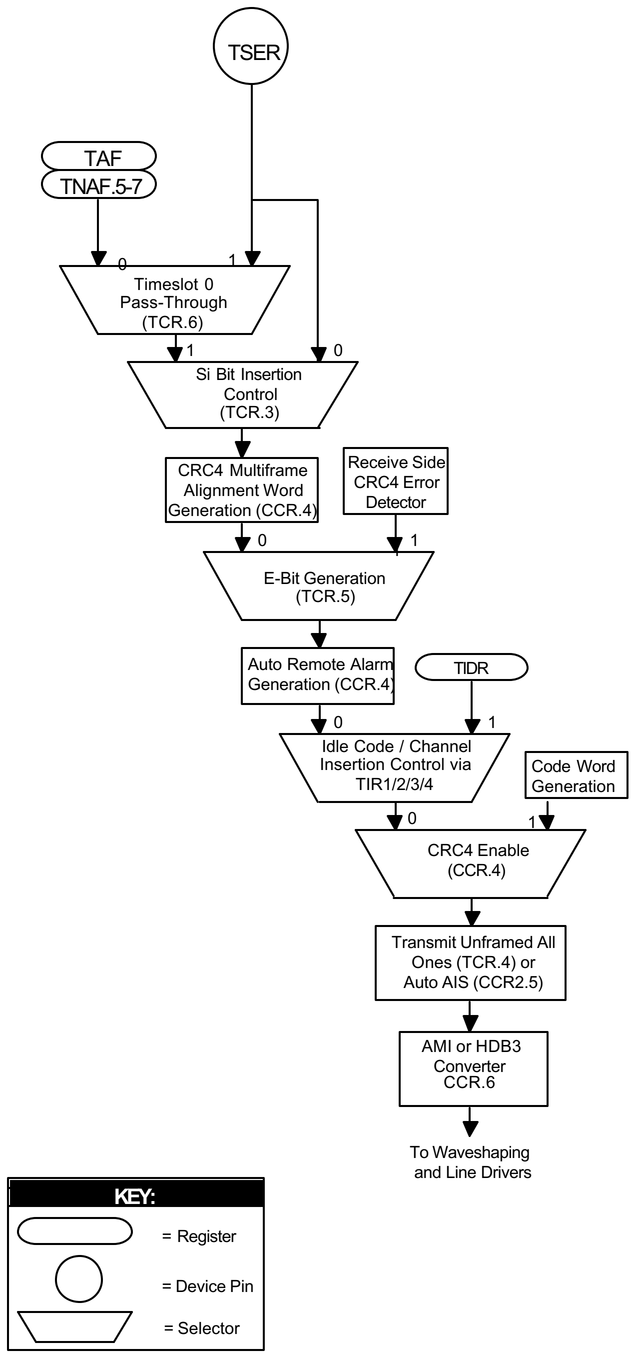
NOTES:

1) 4.096MHz bus configuration.
2) 8.192MHz bus configuration.
3) TSYNC is in the input mode (TCR.0 = 0).

DS21Q50 FRAMER SYNCHRONIZATION FLOWCHART Figure 22-8



DS21Q50 TRANSMIT DATA FLOW Figure 22-9



NOTES:
1. Auto Remote Alarm if enabled will only overwrite bit 3 of timeslot 0 in the Not Align Frames if the alarm needs to be sent.

23. OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS*

Voltage Range on Any Pin Relative to Ground	-1.0V to +6.0V
Operating Temperature Range for DS21Q50L	0°C to +70°C
Operating Temperature Range for DS21Q50LN	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature Range	See J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to +70°C for DS21Q50L; -40°C to +85°C for DS21Q50LN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		5.5	V	
Logic 0	V_{IL}	–0.3		+0.8	V	
Supply	V_{DD}	3.135	3.3	3.465	V	1

CAPACITANCE

(T_A =+25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS

(0°C to +70°C; V_{DD} = 3.3.0V ± 5% for DS21Q50L; -40°C to +85°C; V_{DD} = 3.3.0V ± 5% for DS21Q50LN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 3.3V	I_{DD}		230		mA	2
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
Output Leakage	I_{LO}			1.0	µA	4
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1) Applies to RVDD, TVDD, and DVDD.
2) TCLKs = SYSCLKs = MCLK = 2.048MHz; outputs open circuited; TTIPs and TRINGs driving 30? ; QRSS data pattern. 0.0V < V_{IN} < V_{DD}.
3) Applied to INT* when 3-stated.
4) Applies to output pins in 3-state condition.

24. AC TIMING PARAMETERS AND DIAGRAMS

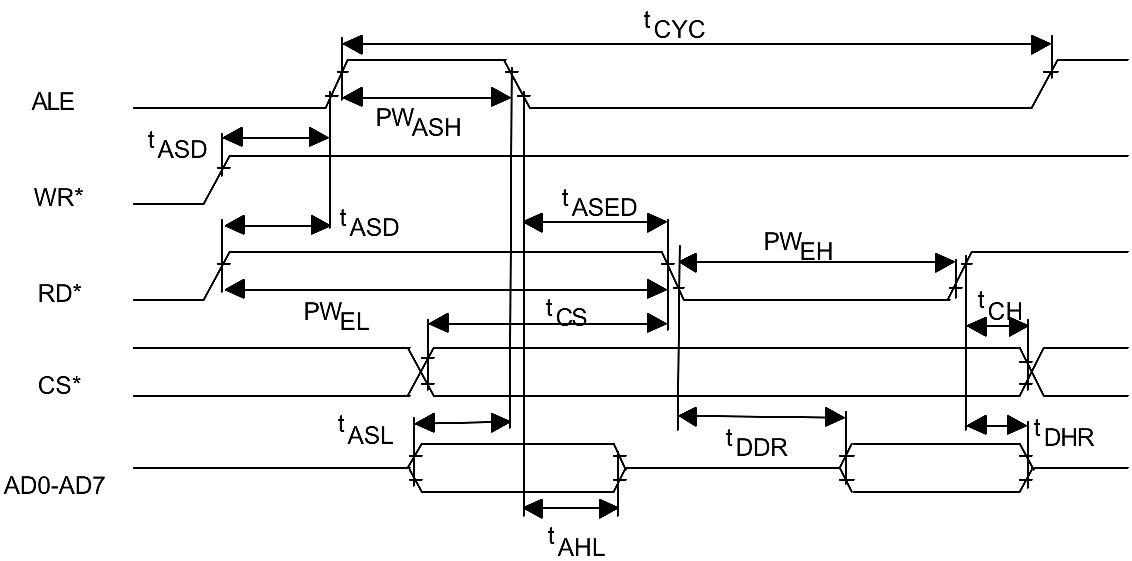
24.1 Multiplexed Bus AC Characteristics

AC CHARACTERISTICS– MULTIPLEXED PARALLEL PORT
[See Figure 24-1 to Figure 24-3]

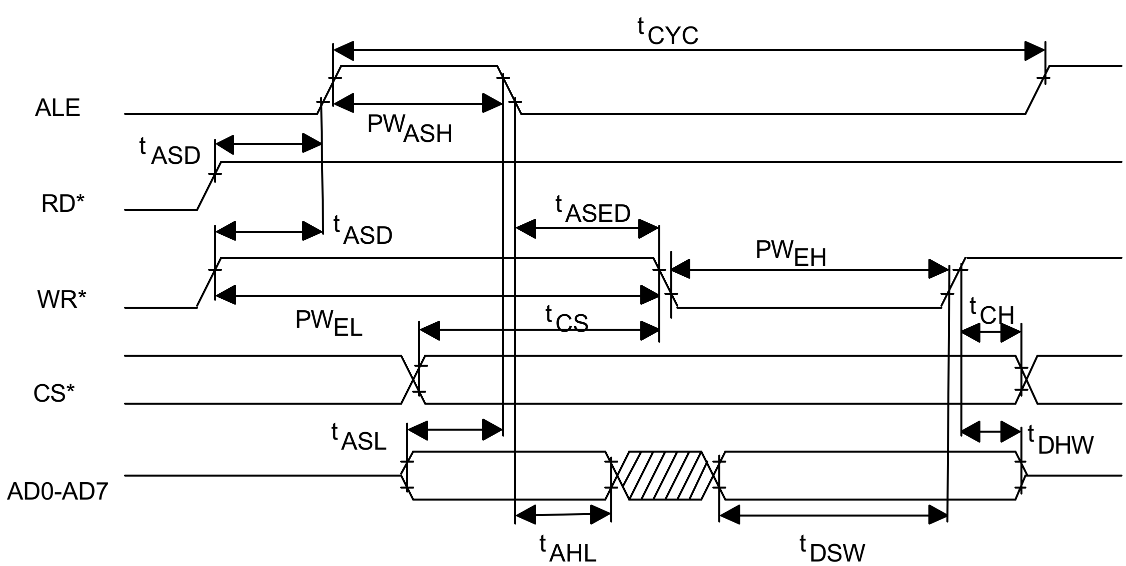
(0°C to +70°C; V_{DD} = 3.3.0V ± 5% for DS21Q50L; -40°C to +85°C; V_{DD} = 3.3.0V ± 5% for DS21Q50LN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	200			ns	
Pulse Width, DS Low or RD* High	PW_{EL}	100			ns	
Pulse Width, DS High or RD* Low	PW_{EH}	100			ns	
Input Rise/Fall times	t_R, t_F			20	ns	
R/W* Hold Time	t_{RWH}	10			ns	
R/W* Setup Time before DS High	t_{RWS}	50			ns	
CS* Setup Time before DS, WR*, or RD* Active	t_{CS}	20			ns	
CS* Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid to AS or ALE Fall	t_{ASL}	15			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay time DS, WR* or RD* to AS or ALE Rise	t_{ASD}	20			ns	
Pulse Width AS or ALE High	PW_{ASH}	30			ns	
Delay Time, AS or ALE to DS, WR* or RD*	t_{ASED}	10			ns	
Output Data Delay Time from DS or RD*	t_{DDR}	20		140	ns	
Data Setup time	t_{DSW}	50			ns	

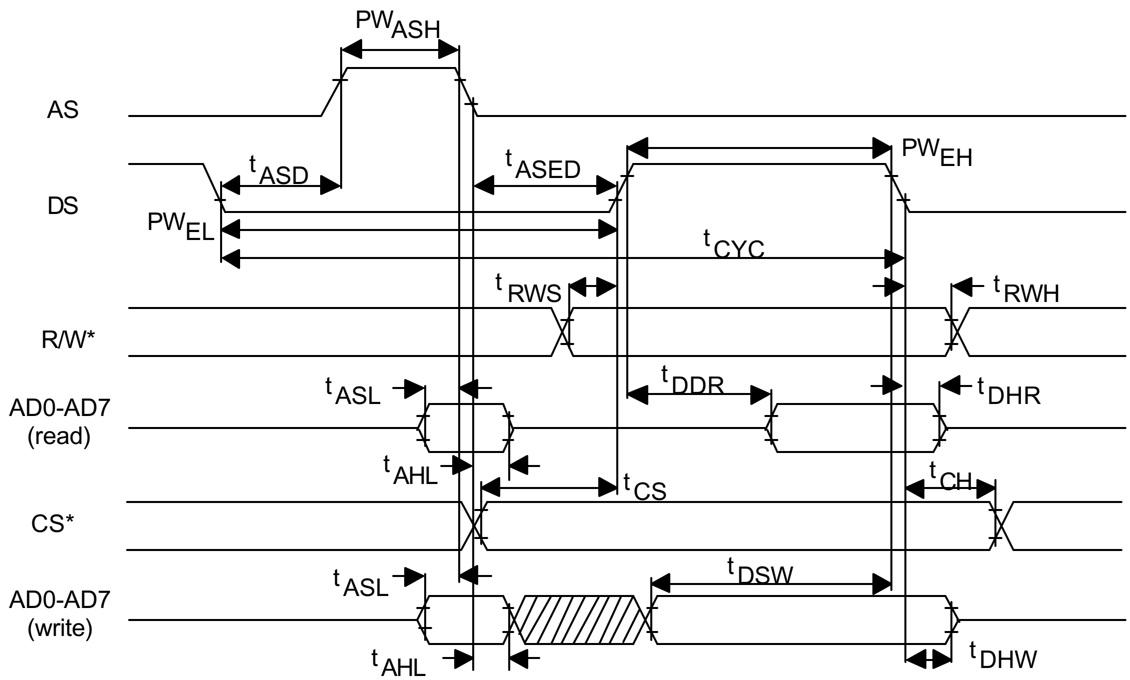
INTEL BUS READ AC TIMING (PBTS = 0) Figure 24-1



INTEL BUS WRITE TIMING (PBTS = 0) Figure 24-2



MOTOROLA BUS AC TIMING (PBTS = 1) Figure 24-3



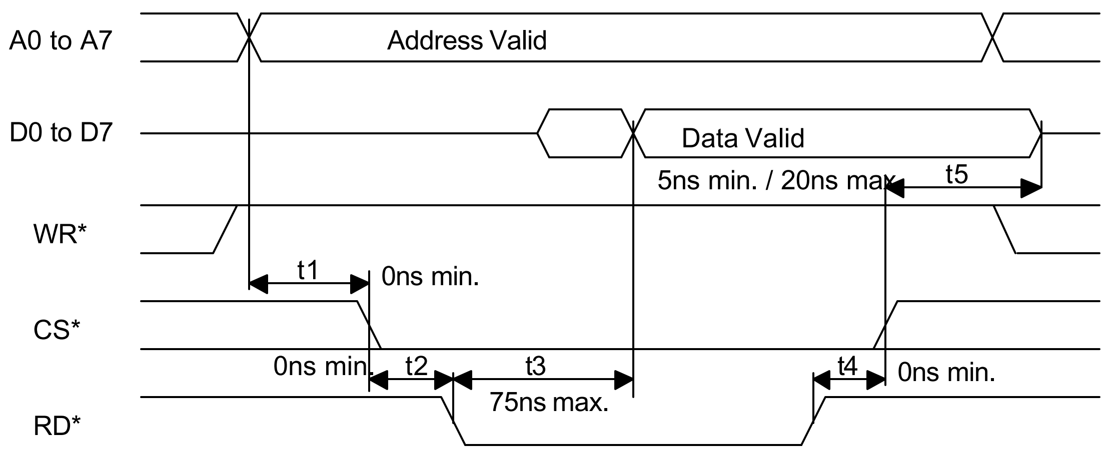
24.2 Nonmultiplexed Bus AC Characteristics

AC CHARACTERISTICS– NONMULTIPLEXED PARALLEL PORT
[See Figure 24-4 to Figure 24-7]

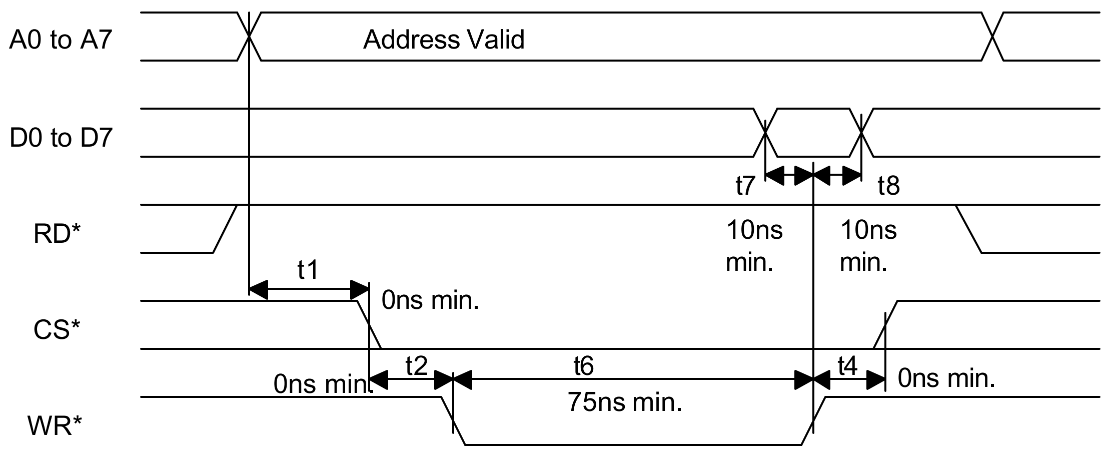
(0°C to +70°C; V_{DD} = 3.3V ± 5% for DS21Q50L; -40°C to +85°C; V_{DD} = 3.3V ± 5% for DS21Q50N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Setup Time for A0 to A7, Valid to CS* Active	t1	0			ns	
Setup Time for CS* Active to Either RD*, WR*, or DS* Active	t2	0			ns	
Delay Time from Either RD* or DS* Active to Data Valid	t3			140	ns	
Hold Time from Either RD*, WR*, or DS* Inactive to CS* Inactive	t4	0			ns	
Hold Time from CS* Inactive to Data Bus 3-State	t5	5		20	ns	
Wait Time from Either WR* or DS* Active to Latch Data	t6	75			ns	
Data Setup Time to Either WR* or DS* Inactive	t7	10			ns	
Data Hold Time from Either WR* or DS* Inactive	t8	10			ns	
Address Hold from Either WR* or DS* Inactive	t9	10			ns	

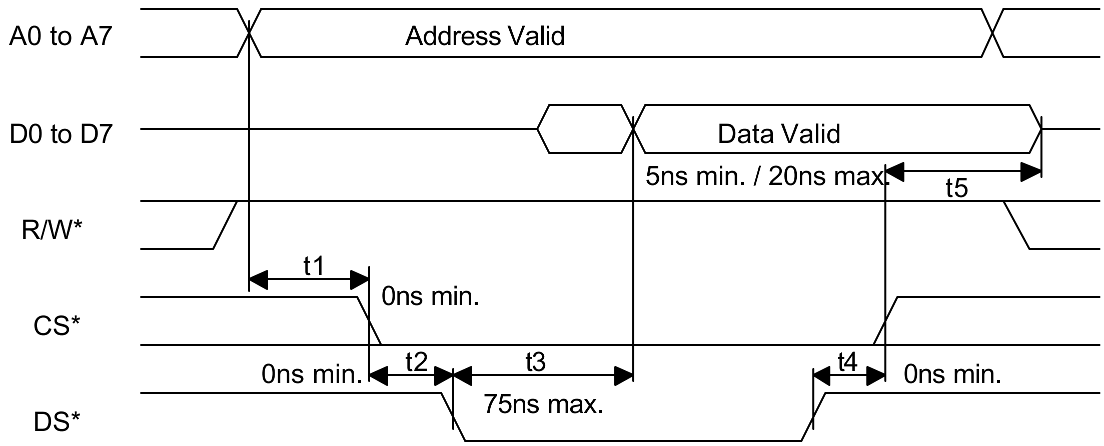
INTEL BUS READ TIMING (PBTS = 0) Figure 24-4



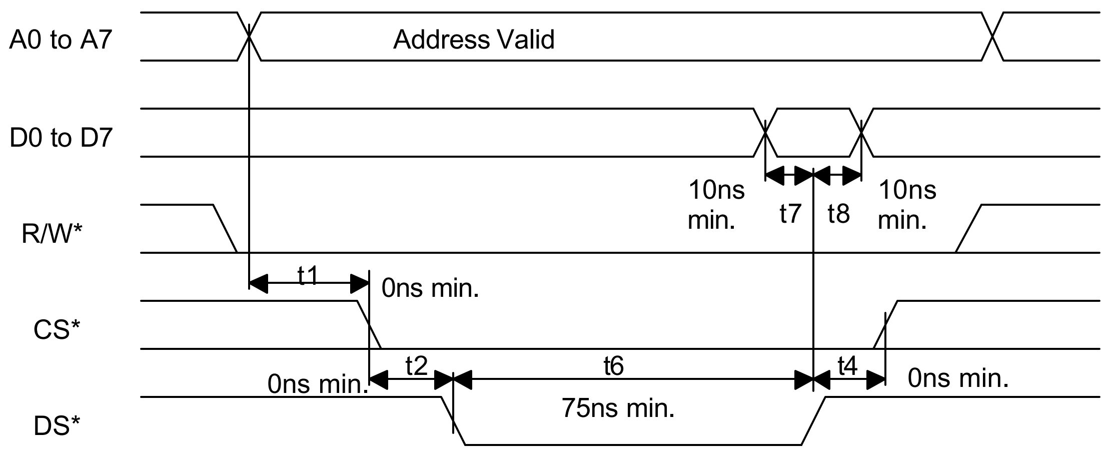
INTEL BUS WRITE TIMING (PBTS = 0) Figure 24-5



MOTOROLA BUS READ TIMING (PBTS = 1) Figure 24-6



MOTOROLA BUS WRITE TIMING (PBTS = 1) Figure 24-7



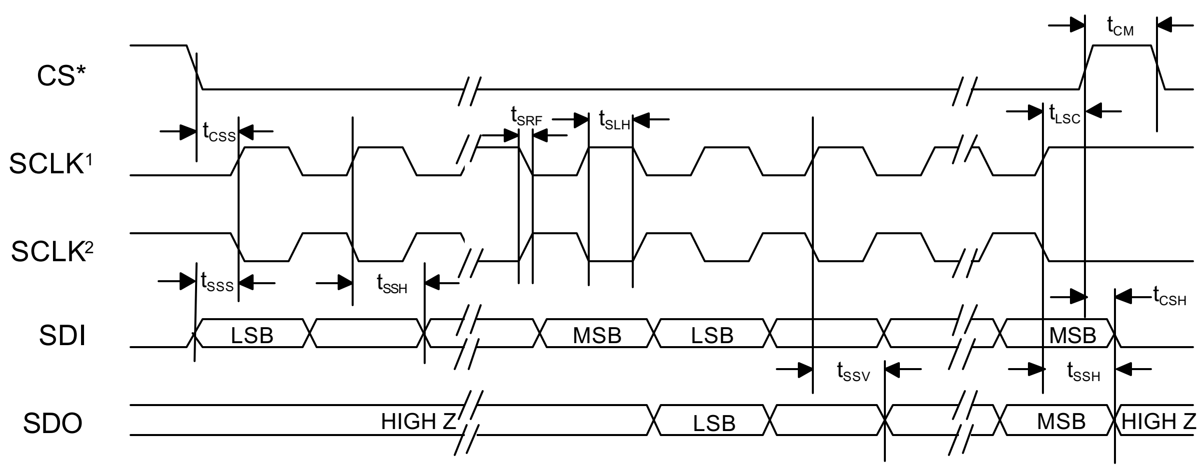
24.3 Serial Port

AC CHARACTERISTICS – SERIAL PORT
(BTS1 = 1, BTS0 = 0) [See Figure 24-8]

(0°C to +70°C; V_{DD} = 3.3V ± 5% for DS21Q50L; -40°C to +85°C; V_{DD} = 3.3V ± 5% for DS21Q50N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Set Up Time CS* to SCLK	t_{CSS}	50			ns	
Set Up Time SDI to SCLK	t_{SSS}	50			ns	
Hold Time SCLK to SDI	t_{SSH}	50			ns	
SCLK High/Low Time	t_{SLH}	200			ns	
SCLK Rise/Fall Time	t_{SRF}			50	ns	
SCLK to CS* Inactive	t_{LSC}	50			ns	
CS* Inactive Time	t_{CM}	250			ns	
SCLK to SDO Valid	t_{SSV}			50	ns	
SCLK to SDO 3-State	t_{SSH}		100		ns	
CS* Inactive to SDO 3-State	t_{CSH}		100		ns	

SERIAL BUS TIMING (BTS1 = 1, BTS0 = 0) Figure 24-8



NOTES:
1) OCES =1 and ICES = 0.
2) OCES = 0 and ICES = 1.

24.4 Receive AC Characteristics

AC CHARACTERISTICS– RECEIVER
[See Figure 24-9 to Figure 24-10]

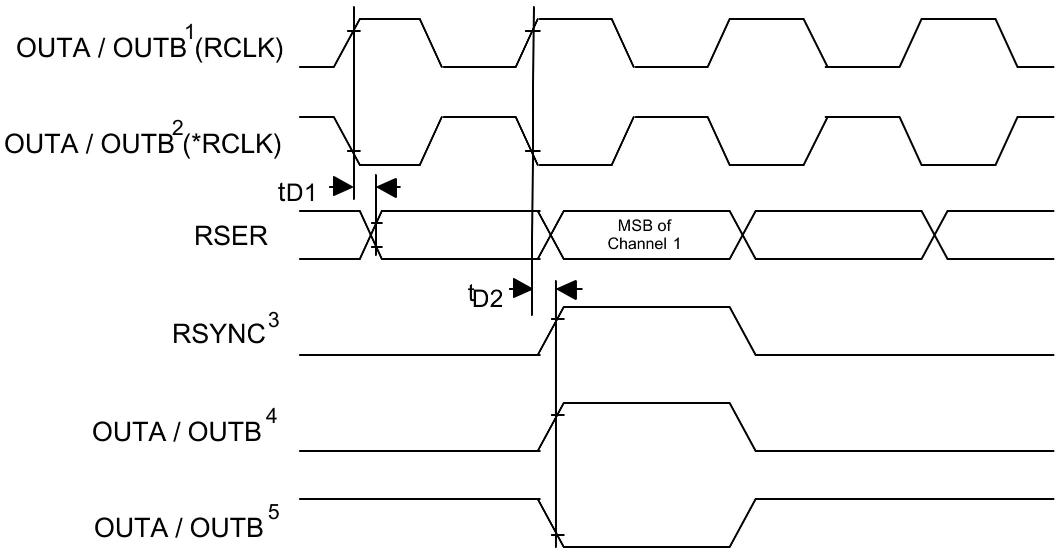
(0°C to +70°C; V_{DD} = 3.3.0V ± 5% for DS21Q50L;
--40°C to +85°C; V_{DD} = 3.3.0V ± 5% for DS21Q50LN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SYSCLK Period	t_{SP}	122	488		ns	1
SYSCLK Pulse Width	t_{SH} t_{SL}	50 50			ns ns	
RSYNC Setup to SYSCLK Falling	t_{SU}	20		t_{SH} - 5	ns	
RSYNC Pulse Width	t_{PW}	50			ns	
Delay RCLK to RSER Valid	t_{D1}			50	ns	
Delay RCLK to RSYNC, OUTA, OUTB	t_{D2}			50	ns	
Delay SYSCLK to RSER Valid	t_{D3}			50	ns	
Delay SYSCLK to RSYNC, OUTA, OUTB	t_{D4}			50	ns	

NOTE:

1) SYSCLK = 2.048MHz.

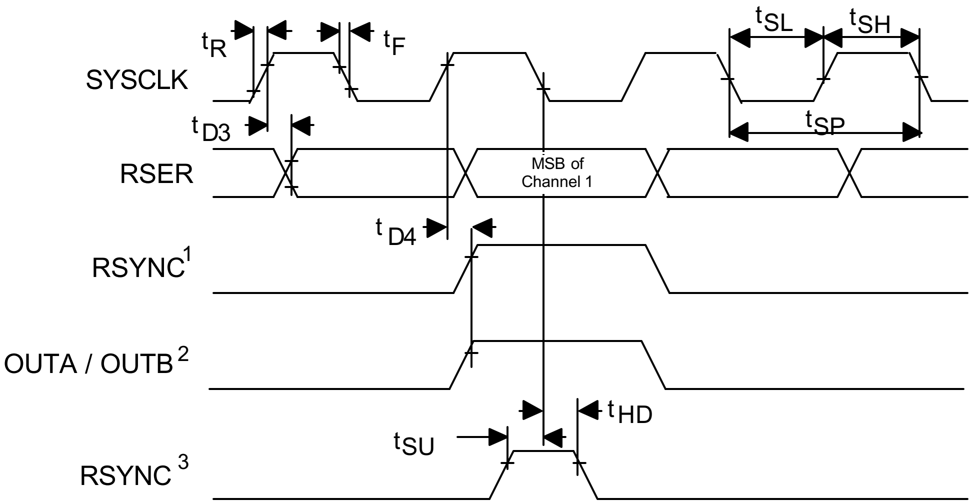
RECEIVE AC TIMING (Receive Elastic Store Disabled) Figure 24-9



NOTES:

1) OUTA or OUTB configured to output RCLK (noninverted).
2) OUTA or OUTB configured to output *RCLK (inverted).
3) RSYNC is in the output mode (RCR1.5 = 0).
4) OUTA or OUTB configured to output RFSYNC, CRC4 MF sync, or CAS MF sync (noninverted).
5) OUTA or OUTB configured to output RFSYNC, CRC4 MF sync, or CAS MF sync (inverted).

RECEIVE AC TIMING (Receive Elastic Store Enabled) Figure 24-10



NOTES:

1) RSYNC is in the output mode (RCR.5 = 0).
2) OUTA or OUTB configured as CRCR MF sync or CAS MF sync.
3) RSYNC is in the output mode (RCR.5 = 1).

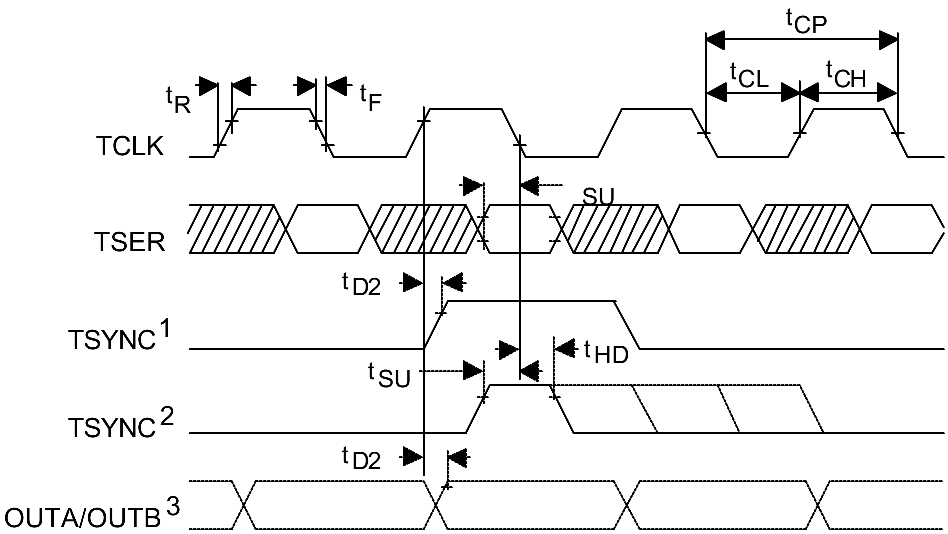
24.5 Transmit AC Characteristics

AC CHARACTERISTICS– TRANSMIT
[See Figure 24-11 to Figure 24-12]

(0°C to +70°C; V_{DD} = 3.3.0V ± 5% for DS21Q50L;
-40°C to +85°C; V_{DD} = 3.3.0V ± 5% for DS21Q50LN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_{CP}		488		ns	
TCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
TSYNC Setup to TCLK	t_{SU}	20		t_{CH} - 5 or t_{SH} - 5	ns	
TSYNC Pulse Width	t_{PW}	50			ns	
TSER Setup to TCLK Falling	t_{SU}	20			ns	
TSER Hold from TCLK Falling	t_{HD}	20			ns	
TCLK Rise and Fall Times	t_R , t_F			25	ns	

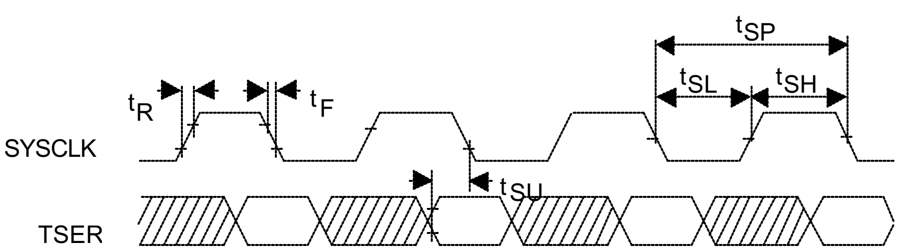
TRANSMIT AC TIMING (IBO Disabled) Figure 24-11



NOTES:

1) TSYNC is in the output mode (TCR.0 = 1)
2) TSYNC is in the input mode (TCR.0 = 0)
3) Applies to OUTA and OUTB when configures for TPOS and TNEG outputs.

TRANSMIT AC TIMING (IBO Enabled) Figure 24-12



NOTE:

1) TSER is only sampled on the falling edge of SYSCLK when the IBO mode is enabled.

24.6 Special Modes AC Characteristics

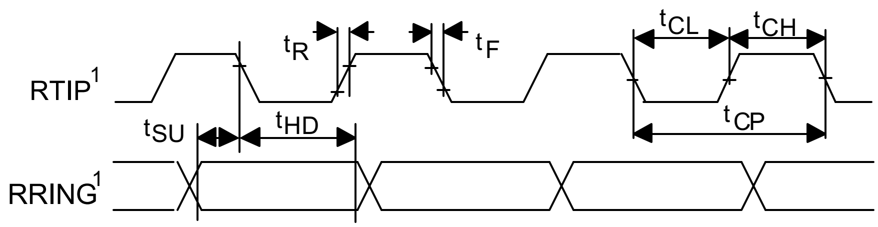
AC CHARACTERISTICS– Special Modes
[See Figure 24-13]

(0°C to +70°C; V_{DD} = 3.3.0V ± 5% for DS21Q50L; -40°C to +85°C; V_{DD} = 3.3.0V ± 5% for DS21Q50LN)

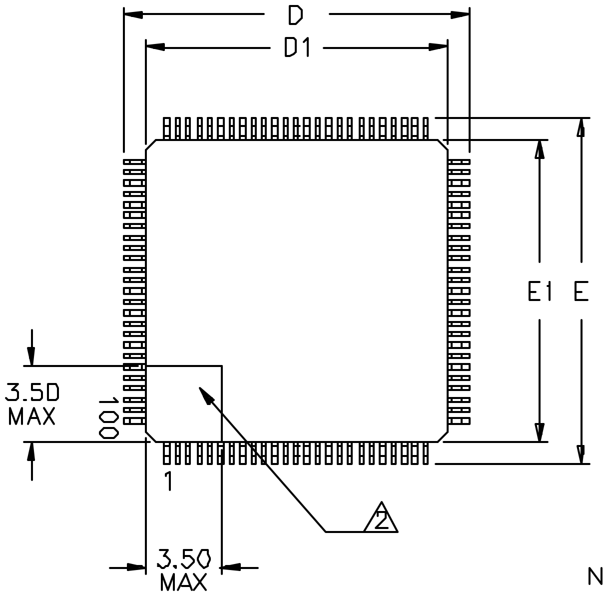
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RTIP Period	t_{CP}		488		ns	
RTIP Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
RTIP Setup to RRING Falling	t_{SU}	20			ns	
TSER Hold from TCLK Falling	t_{HD}	20			ns	
RTIP, RRING Rise and Fall Times	t_R , t_F			25	ns	

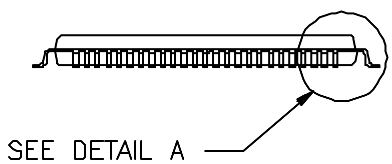
Special Mode: OUTBC.7 = 1
RTIP and RRING become NRZ data and clock inputs.

NRZ INPUT AC TIMING Figure 24-13



25. MECHANICAL DESCRIPTION–100-PIN LQFP

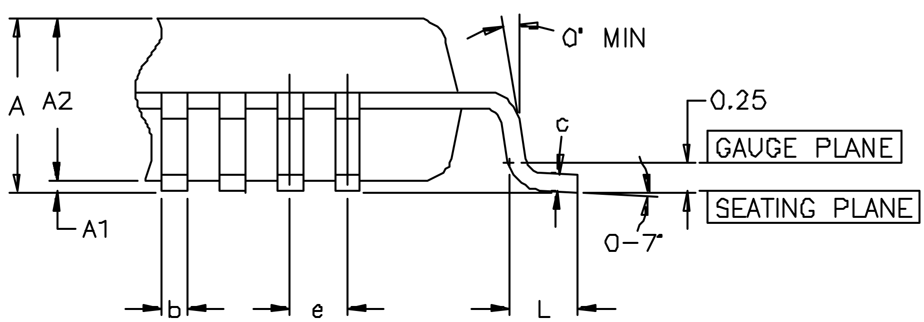




NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. (△) DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION; PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.
4. ALL DIMENSIONS ARE IN MILLIMETERS.

DIM	MIN	MAX
A	–	1.60
A1	0.05	–
A2	1.35	1.45
b	0.17	0.27
c	0.09	0.20
D	15.80	16.20
D1	14.00 BSC	
E	15.80	16.20
E1	14.00 BSC	
e	0.50 BSC	
L	0.45	0.75



DETAIL A