

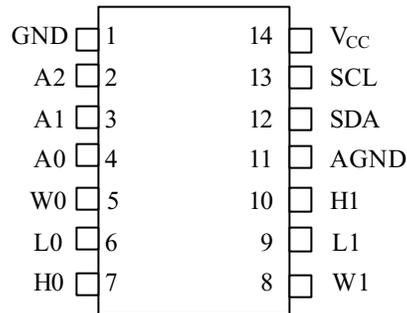
### FEATURES

- Operates from 3V or 5V Power Supplies
- Ultra-low power consumption
- Two digitally controlled, 65-position potentiometers
- Logarithmic resistor characteristics (1 dB per step)
- Zero-crossing detection eliminates noise caused by discrete wiper changes
- Addressable using 3-Chip Select Inputs
- Serial/Synchronous Bus Inputs
- Operating Temperature Range:
  - Industrial: -40°C to +85°C
- Standard Resistance Value: 45 kΩ

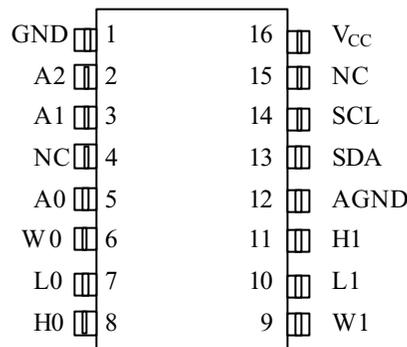
### PIN DESCRIPTION

- |                 |   |                            |
|-----------------|---|----------------------------|
| L0, L1          | - | Low End of Resistor        |
| H0, H1          | - | High End of Resistor       |
| W0, W1          | - | Wiper Terminal of Resistor |
| V <sub>CC</sub> | - | 3V/5V Power Supply Input   |
| A0..A2          | - | Chip Select Inputs         |
| SDA             | - | Serial Data I/O            |
| SCL             | - | Serial Clock Input         |
| GND             | - | Ground                     |
| AGND            | - | Analog Ground              |
| NC              | - | No connection              |

### PIN ASSIGNMENT



DS1807 14-Pin DIP (300-mil)  
DS1807E 14-Pin TSSOP (173-mil)



DS1807S 16-Pin SOIC (300-mil)  
See mech. Drawings Section

### DESCRIPTION

The DS1807 Addressable Dual Audio Taper Potentiometer is a dual audio taper potentiometer having a logarithmic resistive characteristic. Each potentiometer has a total of 65 wiper positions including the mute position. Adjacent wiper positions are separated by 1 dB giving a total attenuation range of 64 dB. When the wipers are in the mute position, attenuation in excess of 90 dB is achieved. The DS1807 also provides a zero-crossing detection capability. This capability eliminates noise caused by discrete wiper position changes. The DS1807 is controlled via a two-input, serial synchronous interface that provides the capability of addressing up to eight different DS1807s. Addressability is obtained via communication protocol and three (3) address select inputs A0, A1, and A2. Communication protocol allows for the exact positioning of the DS1807 wiper's position. Additionally, communication protocol allows for independent or simultaneous setting of the two potentiometers' wipers. Wiper positions can also be read via the 2-wire serial interface.

The DS1807 is available in 14-pin DIP, SOIC, and TSSOP packages. The DS1807 is offered in industrial temperature grades. The standard resistance of the DS1807 is 45 k $\Omega$ .

## DEVICE OPERATION

The DS1807 is an addressable, digitally controlled device that has two 65-position potentiometers. The DS1807 potentiometers are logarithmic tapers providing a resolution or step size of 1 dB per step from positions 0 through 63. The 64<sup>th</sup> position is the mute position and provides attenuation in excess of 90 dB. Moving the potentiometer's wiper from position 63 (or 63 dB of attenuation) to position 64 will provide a step size in excess of 30 dB. A functional block diagram of the part is shown in Figure 1.

As stated, each potentiometer is composed of a 65 position resistor array. Two 8-bit registers, each assigned to a respective potentiometer, are used to set wiper position on the resistor array. The wiper terminal is multiplexed to one of 65 positions on the resistor array based on its corresponding 8-bit register value.

Because the DS1807 has 65 positions, only seven bits of data are needed to set a wiper's position. Bits 0 through 5 of the register are used to set the position on the resistor array. Bit 6 is used to set the wiper position to the mute position and bit 7 is a don't care. *If the value of bit 6 is set equal to 1, regardless of all other bit values, the wiper position of the respective potentiometer will be set to the mute position.* An example diagram of the wiper register and associated bit function is provided in Figure 2.

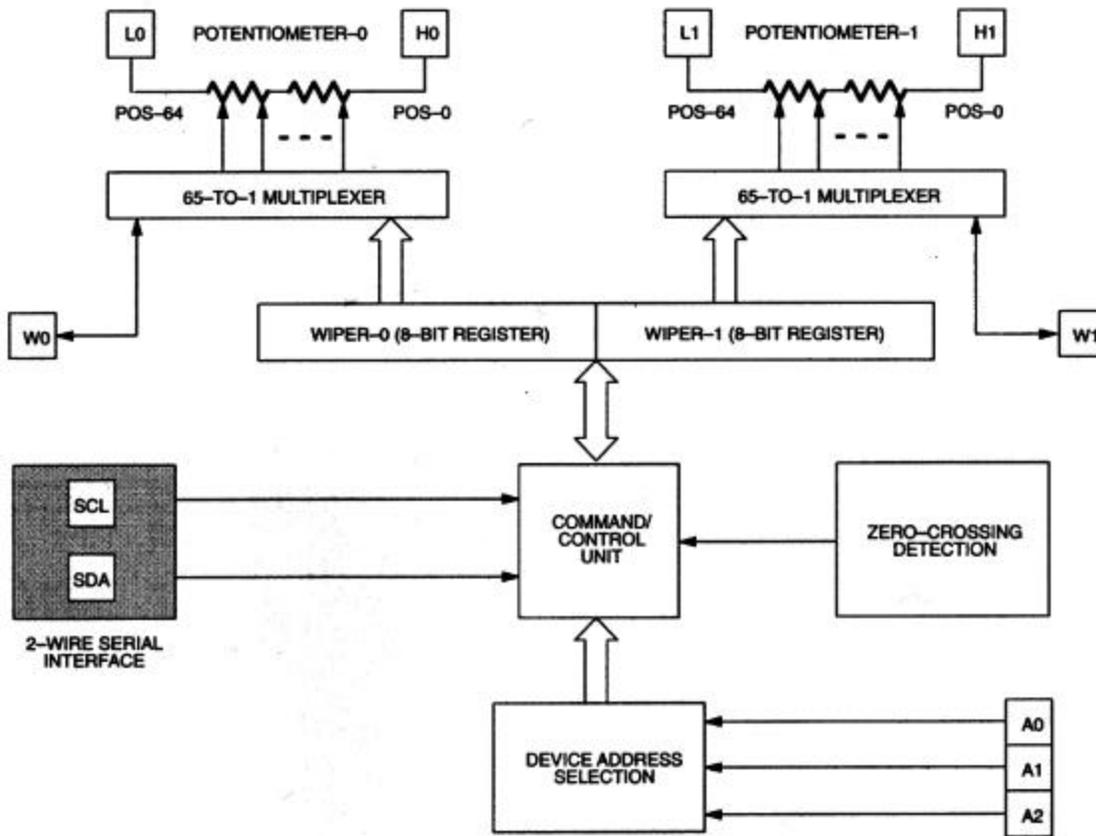
The DS1807 is designed to operate as an attenuator. (see Figure 3) As such, wiper position values are set with respect to the amount of attenuation desired. For example, if the user wishes to attenuate an incoming signal by 6 dB, the wiper position register value(s) should be set to binary (0000 0110).

The H0 and H1 terminals of the DS1807 have wiper position values (binary) 0000 0000. These terminals provide 0 dB of attenuation for the input signal. The L0 and L1 terminals provide the greatest attenuation of the input signal. They represent the mute positions for the DS1807 and have wiper position values (binary) 0100 0000 or greater.

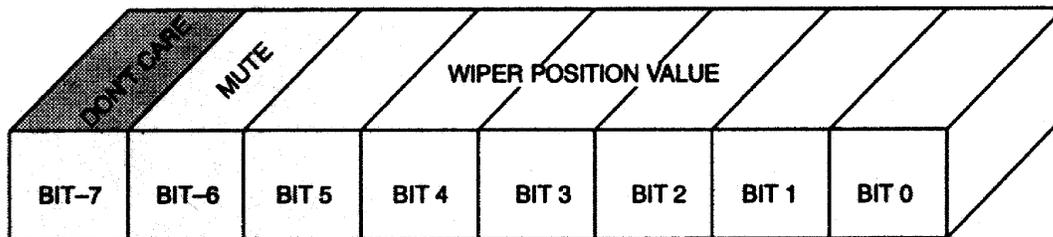
On power-up, the serial port is stable and active within 10 microseconds. Additionally, DS1807 wiper positions will be set to position 63 or (binary) 0011 1111, one position above mute. The user may then set the wiper register to a desired value.

Communication with the DS1807 takes place over the 2-wire serial interface consisting of the bi-directional data terminal, SDA, and the serial clock input, SCL. The 2-wire serial interface and chip select inputs A0, A1, and A2 allow operation of up to eight devices in a bus topology; with A0, A1, and A2 being the physical address of the device. Complete details of the 2-Wire interface are discussed in the section entitled "2-Wire Serial Data Bus."

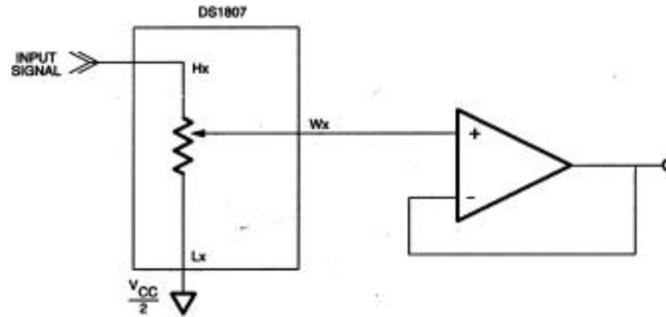
**DS1807 BLOCK DIAGRAM** Figure 1



**WIPER REGISTER CONFIGURATION** Figure 2



## DS1807 ATTENUATOR CONFIGURATION Figure 3



### ZERO-CROSSING DETECTION

The DS1807 provides many features for digitally controlled audio applications. Zero-crossing detection is useful in eliminating “zipper noise,” which is commonly associated with digital potentiometers. Zipper noise (because it sounds like a zipper) is caused by discrete wiper position changes on the resistor array. These changes cause discontinuities in the audio output signal which are manifested as audible pops heard at the output of the audio chain. If subsequent amplification follows the digital potentiometer, this audible noise can be quite disturbing. The DS1807 minimizes zipper noise by allowing wiper position changes only during zero-crossings of the input signal.

The zero-crossing detection feature can be enabled or disabled via software. The complete software command for enabling or disabling zero-crossing is discussed in the section, “2-wire serial data bus.”

When enabled, the zero-crossing detection feature allows *independent* wiper changes within a 50 millisecond time window when the Hx and Lx (where x = 0 or 1) terminals have equal potentials. The 50 millisecond time window begins once the DS1807 has responded with an ACKNOWLEDGE after a “write potentiometer “ command. The STOP condition is discussed in the following section.

If at 50 milliseconds the DS1807 has not detected a zero-crossing ( $Hx - Lx = 0$ ), the wiper position of the potentiometer(s) will change regardless of the state of the input signal.

When the zero-crossing detection feature is not activated, the DS1807 will allow movement to the new wiper position as soon as the ACKNOWLEDGE condition has been issued by the master controlling device.

The DS1807 is designed to provide the zero-crossing detection feature when initially powered. If this feature is not to be used, it must be deactivated once the device has reached a fully powered condition.

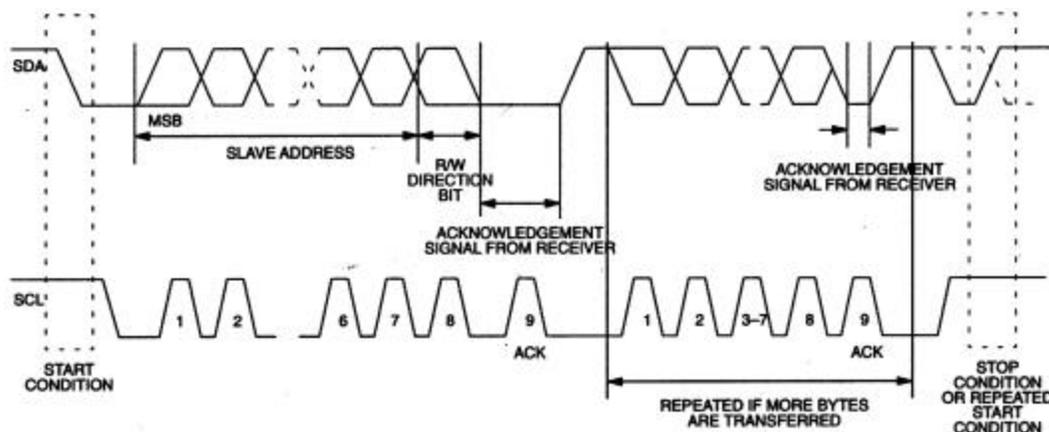
### 2-WIRE SERIAL DATA BUS

The DS1807 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a “master.” The devices that are controlled by the master are “slaves.” The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1807 operates as a slave on the 2-wire bus. Connections to the bus are made via the open-drain I/O line, SDA, and the serial clock line, SCL.

The following bus protocol has been defined (See Figure 4).

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

## 2-WIRE DATA TRANSFER OVERVIEW Figure 4



Accordingly, the following bus conditions have been defined:

**Bus not busy:** Both data and clock lines remain HIGH.

**Start data transfer:** A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

**Stop data transfer:** A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

**Data valid:** The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Figure 4 details how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible:

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a 9th bit.

Within the bus specifications a regular mode (100 kHz clock rate) and a fast mode (400 kHz clock rate) are defined. The DS1807 works in both modes.

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the control byte (or slave address). Next follows a number of data bytes. The slave returns an acknowledge bit after each received. byte.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit . Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a ‘not acknowledge’ is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1807 may operate in the following two modes:

1. **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2. **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1807 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

## SLAVE ADDRESS

A control byte is the first byte received following the START condition from the master device. The control byte consists of a 4-bit control code. For the DS1807, this is set as 0101 binary for read/write operations. The next 3 bits of the control byte are the device select bits (A2, A1, and A0). They are used by the master device to select which of eight devices are to be accessed. The select bits are in effect the three least significant bits of the slave address. The last bit of the control byte (R/W) defines the operation to be performed. When set to a 1 a read operation is selected, and when set to a 0 a write operation is selected. Figure 5 shows the control byte structure for the DS1807.

Following the START condition, the DS1807 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 0101 address code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line.

## COMMAND AND PROTOCOL

The command and protocol structure of the DS1807 allows the user to read or write the potentiometer(s). The command structures for the part are presented in Figures 6 and 7. Potentiometer data values and control and command values are always transmitted most significant bit (MSB) first. During communications, the receiving unit always generates the acknowledgement.

## READING THE DS1807

As shown in Figure 6, the DS1807 provides one read command operation. This operation allows the user to read both potentiometers. Specifically, the R/W bit of the control byte is set equal to a 1 for a read operation. Communication to read the DS1807 begins with a START condition which is issued by the master device. The control byte from the master device will follow the START condition. Once the control byte has been received by the DS1807, the part will respond with an ACKNOWLEDGE. The read/write bit of the control byte as stated should be set equal to 1 for reading the DS1807.

When the master has received the ACKNOWLEDGE from the DS1807, the master can then begin to receive potentiometer wiper data. The value of the potentiometer-0 wiper position will be the first returned from the DS1807. Once the 8 bits of the potentiometer-0 wiper position have been transmitted, the master will need to issue an ACKNOWLEDGE, unless it is the only byte to be read, in which case the master issues a NOT ACKNOWLEDGE. If desired the master may stop the communication transfer at this point by issuing the STOP condition. However, if the value of the potentiometer-1 wiper position value is needed communication transfer can continue by clocking the remaining eight bits of the potentiometer-1 value, followed by a NOT ACKNOWLEDGE. Final communication transfer is terminated by issuing the STOP command. Again the flow of the read operation is presented in Figure 6.

## WRITING THE DS1807

A data flow diagram for writing the DS1807 is shown in Figure 7. The DS1807 has three commands which are used to change the position(s) of the wiper. These include write pot-0, write pot-1, and write pot-0/1. The write pot-0 command allows the user to write the value of potentiometer-0 and as an option the value of potentiometer-1. The write-1 command allows the user to write the value of potentiometer-1 only. The last write command, write-0/1, allows the user to write both potentiometers to the same value with one command and one data value being issued.

All the write operations begin with a START condition. Following the START condition, the master device will issue the control byte. The read/write bit of the control byte will be set to 0 for writing the DS1807. Once the control byte has been issued and the master receives the acknowledgment from the DS1807, the command byte is transmitted to the DS1807. As mentioned above, there exist three write operations that can be used with the DS1807. The binary value of each write command is shown in Figure 7 and also in Table 1.

### 2-WIRE WRITE COMMAND WORDS Table 1

| COMMAND               | COMMAND VALUE |
|-----------------------|---------------|
| Write Potentiometer-0 | 101010 01     |
| Write Potentiometer-1 | 101010 10     |
| Write Both Pots       | 101011 11     |

Once the DS1807 has received the command byte, it will respond with an ACKNOWLEDGE. The master can then write the corresponding data-byte associated with the command byte. When the DS1807 has received the data byte(s), it will respond with an acknowledgement. At this point the master device should respond with the STOP condition.

## ZERO-CROSSING DETECTION COMMAND WORD

Zero-crossing detection was described under the operation section of this document. As stated earlier, zero-crossing detection must be deactivated or activated under software control. The command words used to activate or deactivate the zero-crossing detection feature is shown in Table 2.

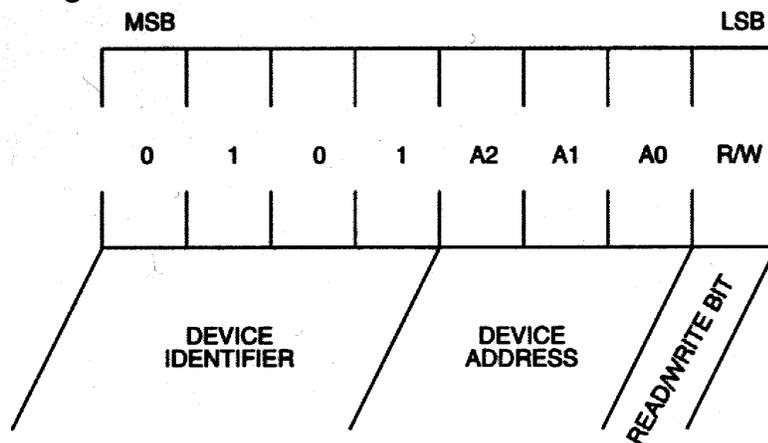
### ZERO-CROSSING DETECTION COMMAND WORDS Table 2

| COMMAND                  | COMMAND VALUE |
|--------------------------|---------------|
| Activate Zero-Crossing   | 101111 01     |
| Deactivate Zero-Crossing | 101111 10     |

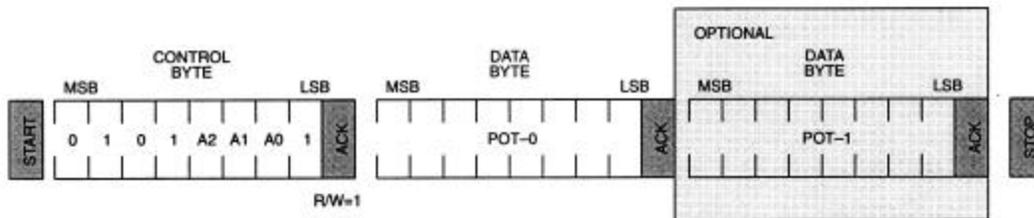
Communication to activate or deactivate zero-crossing detection begins with a START condition which is issued by the master device. The control byte from the master device will follow the START condition. Once the control byte has been received by the DS1807, the part will respond with an ACKNOWLEDGE. The read/write bit of the control byte, as stated, should be set equal to 0 for writing the DS1807.

When the master has received the ACKNOWLEDGE from the DS1807, the master can then begin to transmit the desired zero-crossing detection mode. Once the DS1807 has received the command byte, it will respond with an ACKNOWLEDGE. At this point, the master device should respond with the STOP condition.

### CONTROL BYTE Figure 5

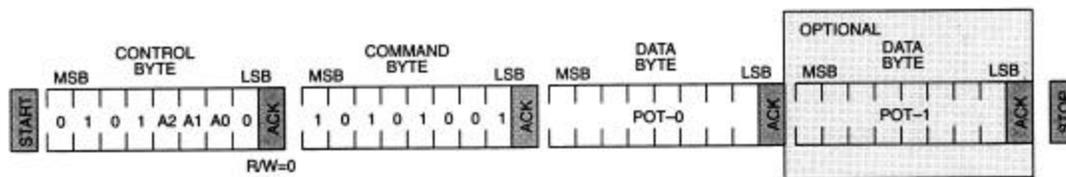


## 2-WIRE READ PROTOCOL Figure 6

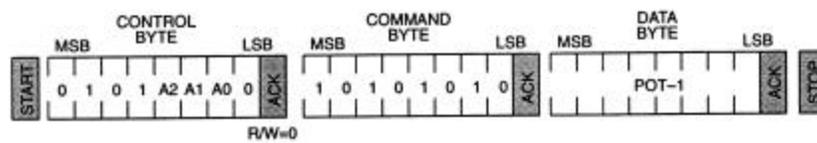


## 2-READ READ PROTOCOL Figure 7

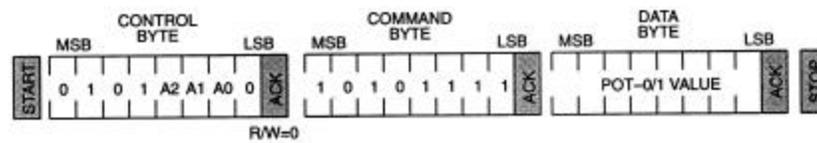
### Write Pot-0



### Write Pot-1



### Write Pot-0/1 (same value)



**ABSOLUTE MAXIMUM RATINGS\***

|                                       |                      |
|---------------------------------------|----------------------|
| Voltage on Any Pin Relative to Ground | -1.0V to +7.0V       |
| Operating Temperature                 | -40° to +85°C        |
| Storage Temperature                   | -55°C to +125°C      |
| Soldering Temperature                 | 260°C for 10 seconds |

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS** (-40°C to +85°C)

| PARAMETER        | SYMBOL   | MIN     | TYP | MAX          | UNITS | NOTES |
|------------------|----------|---------|-----|--------------|-------|-------|
| Supply Voltage   | $V_{CC}$ | +2.7    |     | 5.5          | V     | 1     |
| Resistors Inputs | L,H,W    | GND-0.5 |     | $V_{CC}+0.5$ | V     | 1     |
| Ground           | GND      | GND     |     | GND          | V     | 1,16  |
| Analog Ground    | AGND     | GND-0.7 |     | $GND+0.7$    | V     | 1,16  |

**DC ELECTRICAL CHARACTERISTICS** (-40°C to +85°C;  $V_{CC}=2.7V$  to 5.5V)

| PARAMETER  | SYMBOL     | CONDITION                      | MIN                    | TYP      | MAX                         | UNITS    | NOTES |
|--|------------|--------------------------------|------------------------|----------|-----------------------------|----------|-------|
| Supply Current Active  | $I_{CC}$   |                                |                        |          | 2000                        | $\mu A$  | 3     |
| Input Leakage  | $I_{LI}$   |                                | -1                     |          | +1                          | $\mu A$  |       |
| Wiper Resistance   | $R_W$      |                                |                        | 400      | 1000                        | $\Omega$ |       |
| Wiper Current  | $I_W$      |                                |                        |          | 1                           | mA       |       |
| Input Logic 1  | $V_{IH}$   |                                | $0.7V_{CC}$            |          | $V_{CC}+0.5$                | V        | 1,2   |
| Input Logic 0  | $V_{IL}$   |                                | GND-0.5                |          | $0.3V_{CC}$                 | V        | 1,2   |
| Input Logic Levels A0, A1, A2                                      |            | Input Logic 1<br>Input Logic 0 | $0.7V_{CC}$<br>GND-0.5 |          | $V_{CC}+0.5$<br>$0.3V_{CC}$ | V        | 13    |
| Input Current each I/O Pin   |            | $0.4 < V_{I/O} < 0.9V_{DD}$    | -10                    |          | +10                         | $\mu A$  |       |
| Standby Current<br>3V<br>5V  | $I_{STBY}$ |                                |                        | 12<br>20 | 40                          | $\mu A$  | 4     |
| Low Level Output Voltage   | $V_{OL1}$  | 3 mA sink current              | 0.0                    |          | 0.4                         | V        |       |
|  | $V_{OL2}$  | 6 mA sink current              | 0.0                    |          | 0.6                         | V        |       |
| I/O Capacitance  | $C_{I/O}$  |                                |                        |          | 10                          | pF       |       |
| Pulse Width of Spikes which must be suppressed by the input filter | $t_{SP}$   | Fast Mode                      | 0                      |          | 50                          | ns       |       |

**ANALOG RESISTOR CHARACTERISTICS** (-40°C to +85°C;  $V_{CC}=2.7V$  to 5.5V)

| PARAMETER   | SYMBOL       | MIN   | TYP   | MAX   | UNITS         | NOTES |
|---|--------------|-------|-------|-------|---------------|-------|
| End to End Resistor Tolerance   |              | -20   |       | +20   | %             | 17    |
| Absolute Tolerance  |              | -1    |       | +1    | dB            | 10    |
| Interchannel Matching   |              | -0.5  |       | +0.5  | dB            | 15    |
| Tap-to-Tap  |              | -0.25 |       | +0.25 | dB            | 11    |
| -3 dB Cutoff Frequency  | $f_{cutoff}$ | 700   |       |       | kHz           | 14    |
| Temperature Coefficient   |              |       | 750   |       | ppm/°C        |       |
| Total Harmonic Distortion<br>( $V_{IN}=1$ V RMS , 1 kHz, Tap = -6 dB) | THD          |       | 0.002 |       | %             | 14    |
| Output Noise (20 Hz to 20 kHz,<br>Grounded Input, Tap = -6 dB)        |              |       | 2.2   |       | $\mu V_{RMS}$ | 14    |
| Digital Feedthrough<br>(20 Hz to 20 kHz, Tap = -6 dB)                 |              |       | -90   |       | dB            | 14    |
| Interchannel Isolation<br>(1 kHz, Tap = -6 dB)                        |              |       | -100  |       | dB            | 14    |
| Mute Control Active   |              |       | -100  |       | dB            |       |

**AC ELECTRICAL CHARACTERISTICS** (-40°C to +85°C;  $V_{CC}=2.7V$  to 5.5V)

| PARAMETER   | SYMBOL       | MIN         | TYP | MAX         | UNITS   | NOTES   |
|---|--------------|-------------|-----|-------------|---------|---------|
| SCL Clock Frequency                               | $f_{SCL}$    | 0<br>0      |     | 400<br>100  | kHz     | *<br>** |
| Bus Free Time Between STOP and<br>START Condition | $t_{BUF}$    | 1.3<br>4.7  |     |             | $\mu s$ | *<br>** |
| Hold Time (Repeated) START<br>Condition           | $t_{HD:STA}$ | 0.6<br>4.0  |     |             | $\mu s$ | 5       |
| Low Period of SCL Clock                           | $t_{LOW}$    | 1.3<br>4.7  |     |             | $\mu s$ |         |
| High Period of SCL Clock                          | $t_{HIGH}$   | 0.6<br>4.0  |     |             | $\mu s$ |         |
| Data Hold Time                                    | $t_{HD:DAT}$ | 0<br>0      |     | 0.9         | $\mu s$ | 6,7     |
| Data Set-Up Time                                  | $t_{SU:DAT}$ | 100<br>250  |     |             | ns      | 8       |
| Rise Time of both SDA and SCL<br>Signals          | $t_R$        | $20+0.1C_R$ |     | 300<br>1000 | ns      | 9       |
| Fall Time of both SDA and SCL<br>Signals          | $t_F$        | $20+0.1C_R$ |     | 300<br>300  | ns      | 9       |
| Set-Up Time for STOP Condition                    | $t_{SU:STO}$ | 0.6<br>4.0  |     |             | $\mu s$ |         |
| Capacitive Load for each Bus Line                 | $C_R$        |             |     | 400         | pF      |         |

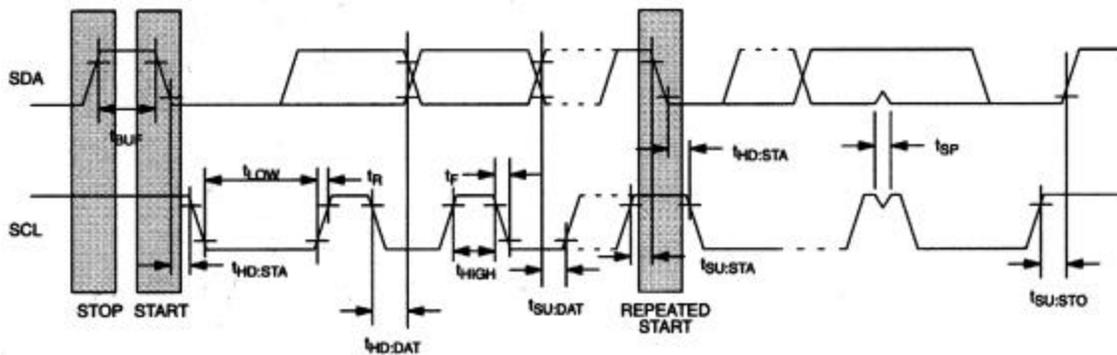
\*fast mode

\*\*standard mode

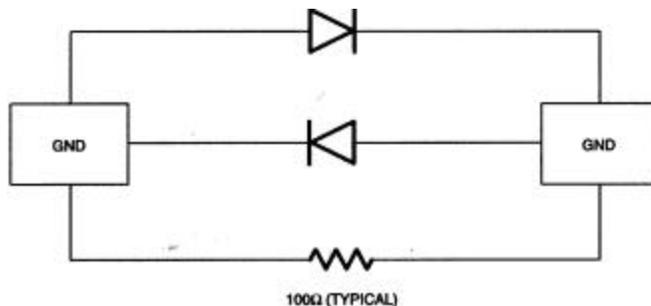
**NOTES:**

1. All voltages are referenced to ground.
2. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if  $V_{DD}$  is switched off.
3.  $I_{CC}$  specified with zero-crossing detection active and operating device serial port in fast mode.
4.  $I_{STBY}$  specified with for  $V_{CC}$  equal 3.0V and 5.0V and SDA and SCL are driven to the appropriate logic levels.  $I_{STBY}$  is specified as the current consumption of the device when SDA and SCL are in the inactive (high) states.
5. After this period, the first clock pulse is generated.
6. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the  $V_{IHMIN}$  of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7. The maximum  $t_{HD:DAT}$  has only to be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal.
8. A fast mode device can be used in a standard mode system, but the requirement  $t_{SU:DAT} > 250$  ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{RMAX} + t_{SU:DAT} = 1000 + 250 = 1250$  ns before the SCL line is released.
9.  $C_B$ - total capacitance of one bus line in picofarads, timing referenced to  $(0.9(V_{CC}))$  and  $(0.1)(V_{CC})$ .
10. Absolute tolerance is used to determine measured wiper voltage versus expected wiper voltage as determined by wiper position.
11. Tap-to-tap tolerance is used to determine the change in voltage between successive tap positions. The DS1807 is specified for a  $\pm 0.25$  dB tap-to-tap tolerance.
12. Typical values are for  $t_A = 25^\circ\text{C}$  and nominal supply voltage.
13. Address inputs, A0, A1, and A2, should be tied to either  $V_{CC}$  or GND depending on the desired address selections.
14. These parameters are characterized and not 100% tested.
15. Interchannel matching is used to determine the relative difference in dB between the same position on each potentiometer. The DS1807 is specified for  $\pm 0.5$  dB Interchannel matching
16. See Figure 9.
17. Valid at  $25^\circ\text{C}$  only.

**TIMING DIAGRAM Figure 8**



**INTERNAL GROUND CONNECTIONS Figure 9**



**NOTE:** GND and AGND must be tied to the same voltage level.

**DS1807 ORDERING INFORMATION**

| ORDERING NUMBER | PACKAGE             | OPERATING TEMPERATURE | VERSION |
|-----------------|---------------------|-----------------------|---------|
| DS1807          | 14L DIP             | -40°C TO +85°C        | 45KΩ    |
| DS1807E         | 14L TSSOP (173-MIL) | -40°C TO +85°C        | 45KΩ    |
| DS1807S         | 16L SOIC (300-MIL)  | -40°C TO +85°C        | 45KΩ    |