

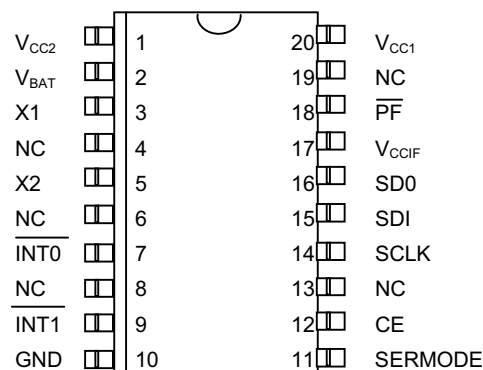
### FEATURES

- Real-time clock (RTC) counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap-year compensation valid up to 2100
- 96-byte, battery-backed, nonvolatile (NV) RAM for data storage
- Two time-of-day alarms—programmable on combination of seconds, minutes, hours, and day of the week
- Serial interface supports Motorola Serial Peripheral Interface (SPI) serial data ports or standard 3-wire interface
- Burst mode for reading/writing successive addresses in clock/RAM
- Dual-power supply pins for primary and backup power supplies
- Optional trickle charge output to backup supply
- 2.0V to 5.5V operation
- Optional industrial temperature range: -40°C to +85°C
- Available in space-efficient, 20-pin TSSOP package
- Underwriters Laboratory (UL) recognized

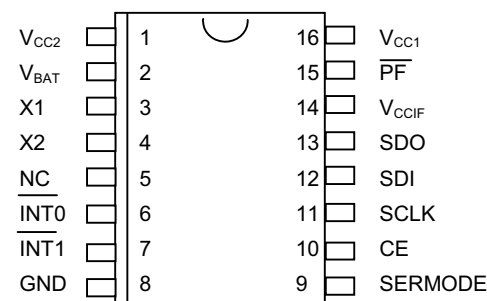
### ORDERING INFORMATION

DS1305	16-Pin DIP (300mil)
DS1305N	16-Pin DIP (Industrial)
DS1305E	20-Pin TSSOP (173mil)
DS1305EN	20-Pin TSSOP (Industrial)

### PIN ASSIGNMENT

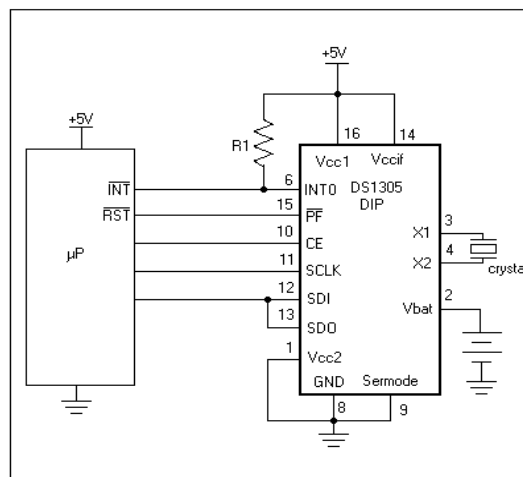


DS1305 20-Pin TSSOP (173mil)



DS1305 16-Pin DIP (300mil)

### TYPICAL OPERATING CIRCUIT



## PIN DESCRIPTION

$V_{CC1}$	- Primary Power Supply
$V_{CC2}$	- Backup Power Supply
$V_{BAT}$	- +3V Battery Input
$V_{CCIF}$	- Interface Logic Power Supply Input
GND	- Ground
X1, X2	- 32,768kHz Crystal Connection
$\overline{INT0}$	- Interrupt 0 Output
$\overline{INT1}$	- Interrupt 1 Output
SDI	- Serial Data In
SDO	- Serial Data Out
CE	- Chip Enable
SCLK	- Serial Clock
SERMODE	- Serial Interface Mode
$\overline{PF}$	- Power-Fail Output

## DESCRIPTION

The DS1305 Serial Alarm Real-Time Clock provides a full binary-coded decimal (BCD) clock calendar that is accessed via a simple serial interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. In addition, 96 bytes of nonvolatile RAM are provided for data storage.

An interface logic power supply input pin ( $V_{CCIF}$ ) allows the DS1305 to drive SDO and  $\overline{PF}$  pins to a level that is compatible with the interface logic. This allows an easy interface to 3V logic in mixed supply systems.

The DS1305 offers dual-power supplies as well as a battery input pin. The dual power supplies support a programmable trickle charge circuit that allows a rechargeable energy source (such as a super cap or rechargeable battery) to be used for a backup supply. The  $V_{BAT}$  pin allows the device to be backed up by a non-rechargeable battery. The DS1305 is fully operational from 2.0V to 5.5V.

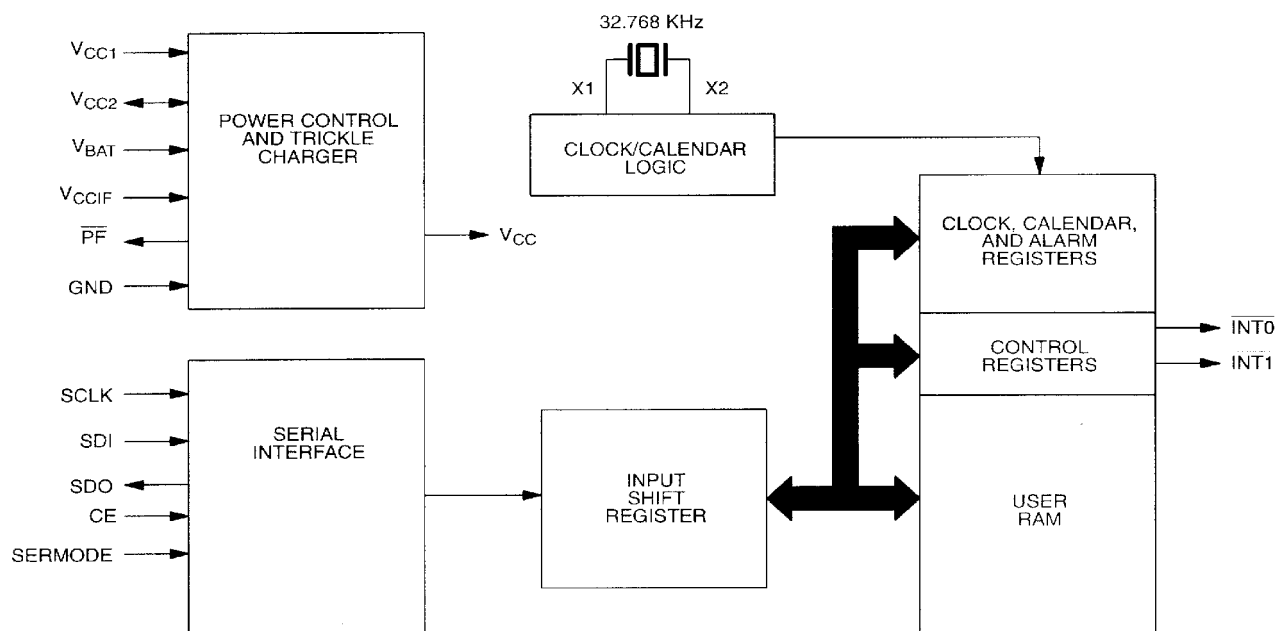
Two programmable time-of-day alarms are provided by the DS1305. Each alarm can generate an interrupt on a programmable combination of seconds, minutes, hours, and day. “Don’t care” states can be inserted into one or more fields if it is desired for them to be ignored for the alarm condition. The time-of-day alarms can be programmed to assert two different interrupt outputs or to assert one common interrupt output. Both interrupt outputs operate when the device is powered by  $V_{CC1}$ ,  $V_{CC2}$ , or  $V_{BAT}$ .

The DS1305 supports a direct interface to Motorola SPI serial data ports or standard 3-wire interface. A straightforward address and data format is implemented in which data transfers can occur 1 byte at a time or in multiple-byte burst mode.

## OPERATION

The block diagram in Figure 1 shows the main elements of the serial alarm RTC. The following paragraphs describe the function of each pin.

### DS1305 BLOCK DIAGRAM Figure 1



## SIGNAL DESCRIPTIONS

**V<sub>CC1</sub>** – DC power is provided to the device on this pin. V<sub>CC1</sub> is the primary power supply.

**V<sub>CC2</sub>** – This is the secondary power supply pin. In systems using the trickle charger, the rechargeable energy source is connected to this pin.

**V<sub>BAT</sub>** – Battery input for any standard 3V lithium cell or other energy source. UL recognized to ensure against reverse charging current when used in conjunction with a lithium battery.

See “Conditions of Acceptability” at <http://www.maxim-ic.com/TechSupport/QA/ntrl.htm>.

**V<sub>CCIF</sub> (Interface Logic Power Supply Input)** – The V<sub>CCIF</sub> pin allows the DS1305 to drive SDO and  $\overline{\text{PF}}$  output pins to a level that is compatible with the interface logic, thus allowing an easy interface to 3V logic in mixed supply systems. This pin is physically connected to the source connection of the p-channel transistors in the output buffers of the SDO and  $\overline{\text{PF}}$  pins.

**SERMODE (Serial Interface Mode Input)** – The SERMODE pin offers the flexibility to choose between two serial interface modes. When connected to GND, standard 3-wire communication is selected. When connected to V<sub>CC</sub>, Motorola SPI communication is selected.

**SCLK (Serial Clock Input)** – SCLK is used to synchronize data movement on the serial interface for either the SPI or 3-wire interface.

**SDI (Serial Data Input)** – When SPI communication is selected, the SDI pin is the serial data input for the SPI bus. When 3-wire communication is selected, this pin must be tied to the SDO pin (the SDI and SDO pins function as a single I/O pin when tied together).

**SDO (Serial Data Output)** – When SPI communication is selected, the SDO pin is the serial data output for the SPI bus. When 3-wire communication is selected, this pin must be tied to the SDI pin (the SDI and SDO pins function as a single I/O pin when tied together).

**CE (Chip Enable)** – The chip enable signal must be asserted high during a read or a write for both 3-wire and SPI communication. This pin has an internal 55k pull-down resistor (typical).

**$\overline{\text{INT0}}$  (Interrupt 0 Output)** – The  $\overline{\text{INT0}}$  pin is an active low output of the DS1305 that can be used as an interrupt input to a processor. The  $\overline{\text{INT0}}$  pin can be programmed to be asserted by only Alarm 0 or can be programmed to be asserted by either Alarm 0 or Alarm 1. The  $\overline{\text{INT0}}$  pin remains low as long as the status bit causing the interrupt is present and the corresponding interrupt enable bit is set. The  $\overline{\text{INT0}}$  pin operates when the DS1305 is powered by  $V_{CC1}$ ,  $V_{CC2}$ , or  $V_{BAT}$ . The  $\overline{\text{INT0}}$  pin is an open drain output and requires an external pull-up resistor.

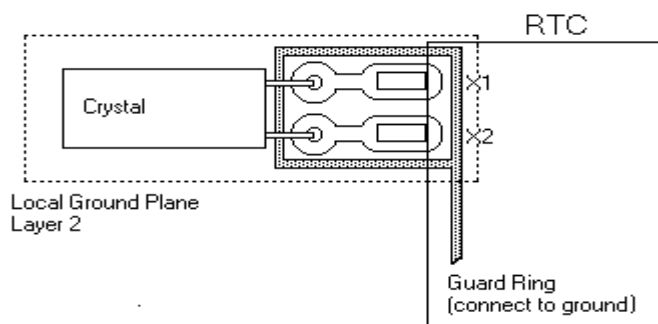
**$\overline{\text{INT1}}$  (Interrupt 1 Output)** – The  $\overline{\text{INT1}}$  pin is an active low output of the DS1305 that can be used as an interrupt input to a processor. The  $\overline{\text{INT1}}$  pin can be programmed to be asserted by Alarm 1 only. The  $\overline{\text{INT1}}$  pin remains low as long as the status bit causing the interrupt is present and the corresponding interrupt enable bit is set. The  $\overline{\text{INT1}}$  pin operates when the DS1305 is powered by  $V_{CC1}$ ,  $V_{CC2}$ , or  $V_{BAT}$ . The  $\overline{\text{INT1}}$  pin is an open drain output and requires an external pull-up resistor.

Both  $\overline{\text{INT0}}$  and  $\overline{\text{INT1}}$  are open drain outputs. The two interrupts and the internal clock continue to run regardless of the level of  $V_{CC}$  (as long as a power source is present).

**$\overline{\text{PF}}$  (Power Fail Output)** – The  $\overline{\text{PF}}$  pin is used to indicate loss of the primary power supply ( $V_{CC1}$ ). When  $V_{CC1}$  is less than  $V_{CC2}$  or is less than  $V_{BAT}$ , the  $\overline{\text{PF}}$  pin will be driven low.

**X1, X2** – Connections for a standard 32.768kHz quartz crystal. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6pF. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, “Crystal Considerations with Dallas Real-Time Clocks.” The DS1305 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

## RECOMMENDED LAYOUT FOR CRYSTAL



## CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error will be added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. See Application Note 58, “Crystal Considerations with Dallas Real-Time Clocks” for detailed information.

## CLOCK, CALENDAR, AND ALARM

The time and calendar information is obtained by reading the appropriate register bytes. The RTC registers and user RAM are illustrated in Figure 2. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. Note that some bits are set to zero. These bits will always read 0 regardless of how they are written. Also note that registers 12h to 1Fh (read) and registers 92h to 9Fh are reserved. These registers will always read 0 regardless of how they are written. The contents of the time, calendar, and alarm registers are in the BCD format.

Except where otherwise noted, the initial power on state of all registers is not defined. Therefore, it is important to enable the oscillator (EOSC = 0) and disable write protect (WP = 0) during initial configuration.

**RTC REGISTERS AND ADDRESS MAP Figure 2**

HEX ADDRESS READ    WRITE		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	RANGE	
00H	80H	0	10 SEC			SEC				00-99	
01H	81H	0	10 MIN			MIN				00-59	
02H	82H	0	12	P	10 HR	HOURS				01-12 + P/A	
				A						00-23	
			24	10							
03H	83H	0	0	0	0	DAY				1-7	
04H	84H	0	0	10 DATE		DATE				1-31	
05H	85H	0	0	10 MONTH		MONTH				01-12	
06H	86H	10 YEAR				YEAR				00-99	
		Alarm 0									
07H	87H	M	10 SEC ALARM			SEC ALARM				00-59	
08H	88H	M	10 MIN ALARM			MIN ALARM				00-59	
09H	89H	M	12	P	10 HR	HOUR ALARM				01-12 + P/A	
				A						00-23	
			24	10							
0AH	8AH	M	0	0	0	DAY ALARM				01-07	
		Alarm 1									
0BH	8BH	M	10 SEC ALARM			SEC ALARM				00-59	
0CH	8CH	M	10 MIN ALARM			MIN ALARM				00-59	
0DH	8DH	M	12	P	10 HR	HOUR ALARM				01-12 + P/A	
				A						00-23	
			24	10							
0EH	8EH	M	0	0	0	DAY ALARM				01-07	
0FH	8FH	CONTROL REGISTER									
10H	90H	STATUS REGISTER									
11H	91H	TRICKLE CHARGER REGISTER									
12-1FH	92-9FH	RESERVED									
20-7FH	A0-FFH	96 BYTES USER RAM									00-FF

**Note:** Range for alarm registers does not include mask'm' bits.

The DS1305 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours).

The DS1305 contains two time-of-day alarms. Time-of-day alarm 0 can be set by writing to registers 87h to 8Ah. Time-of-day alarm 1 can be set by writing to registers 8Bh to 8Eh. The alarms can be programmed (by the INTCN bit of the control register) to operate in two different modes; each alarm can drive its own separate interrupt output or both alarms can drive a common interrupt output. Bit 7 of each of the time-of-day alarm registers are mask bits (Table 1). When all of the mask bits are logic 0, a time-of-day alarm will only occur once per week when the values stored in timekeeping registers 00h to 03h match the values stored in the time-of-day alarm registers. An alarm will be generated every day when bit 7 of the day alarm register is set to a logic 1. An alarm will be generated every hour when bit 7 of the day and hour alarm registers is set to a logic 1. Similarly, an alarm will be generated every minute when bit 7 of the day, hour, and minute alarm registers is set to a logic 1. When bit 7 of the day, hour, minute, and seconds alarm registers is set to a logic 1, alarm will occur every second.

**TIME-OF-DAY ALARM MASK BITS Table 1**

ALARM REGISTER MASK BITS (BIT 7)				
SECONDS	MINUTES	HOURS	DAYS	
1	1	1	1	Alarm once per second
0	1	1	1	Alarm when seconds match
0	0	1	1	Alarm when minutes and seconds match
0	0	0	1	Alarm hours, minutes and seconds match
0	0	0	0	Alarm day, hours, minutes and seconds match

**SPECIAL PURPOSE REGISTERS**

The DS1305 has three additional registers (control register, status register, and trickle charger register) that control the real-time clock, interrupts, and trickle charger.

**CONTROL REGISTER (READ 0FH, WRITE 8FH)**

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
$\overline{\text{EOSC}}$	WP	0	0	0	INTCN	AIE1	AIE0

**$\overline{\text{EOSC}}$  (Enable Oscillator)** – This bit when set to logic 0 will start the oscillator. When this bit is set to a logic 1, the oscillator is stopped and the DS1305 is placed into a low-power standby mode with a current drain of less than 100 nanoamps when power is supplied by  $V_{\text{BAT}}$  or  $V_{\text{CC2}}$ . The initial power on state is not defined.

**WP (Write Protect)** – Before any write operation to the clock or RAM, this bit must be logic 0. When high, the write protect bit prevents a write operation to any register, including bits 0, 1, 2, and 7 of the control register. Upon initial power-up, the state of the WP bit is undefined. Therefore, the WP bit should be cleared before attempting to write to the device.

**INTCN (Interrupt Control)** – This bit controls the relationship between the two time-of-day alarms and the interrupt output pins. When the INTCN bit is set to a logic 1, a match between the timekeeping registers and the alarm 0 registers will activate the  $\overline{\text{INT0}}$  pin (provided that the alarm is enabled) and a match between the timekeeping registers and the alarm 1 registers will activate the  $\overline{\text{INT1}}$  pin (provided that the alarm is enabled). When the INTCN bit is set to a logic 0, a match between the timekeeping registers and either alarm 0 or alarm 1 will activate the  $\overline{\text{INT0}}$  pin (provided that the alarms are enabled).  $\overline{\text{INT1}}$  has no function when INTCN is set to a logic 0.

**AIE0 (Alarm Interrupt Enable 0)** – When set to a logic 1, this bit permits the interrupt 0 request flag (IRQF0) bit in the status register to assert  $\overline{\text{INT0}}$ . When the AIE0 bit is set to logic 0, the IRQF0 bit does not initiate the  $\overline{\text{INT0}}$  signal.

**AIE1 (Alarm Interrupt Enable 1)** – When set to a logic 1, this bit permits the interrupt 1 request flag (IRQF1) bit in the status register to assert  $\overline{\text{INT1}}$  (when INTCN = 1) or to assert  $\overline{\text{INT0}}$  (when INTCN = 0). When the AIE1 bit is set to logic 0, the IRQF1 bit does not initiate an interrupt signal.

**STATUS REGISTER (READ 10H)**

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	0	0	0	0	0	IRQF1	IRQF0

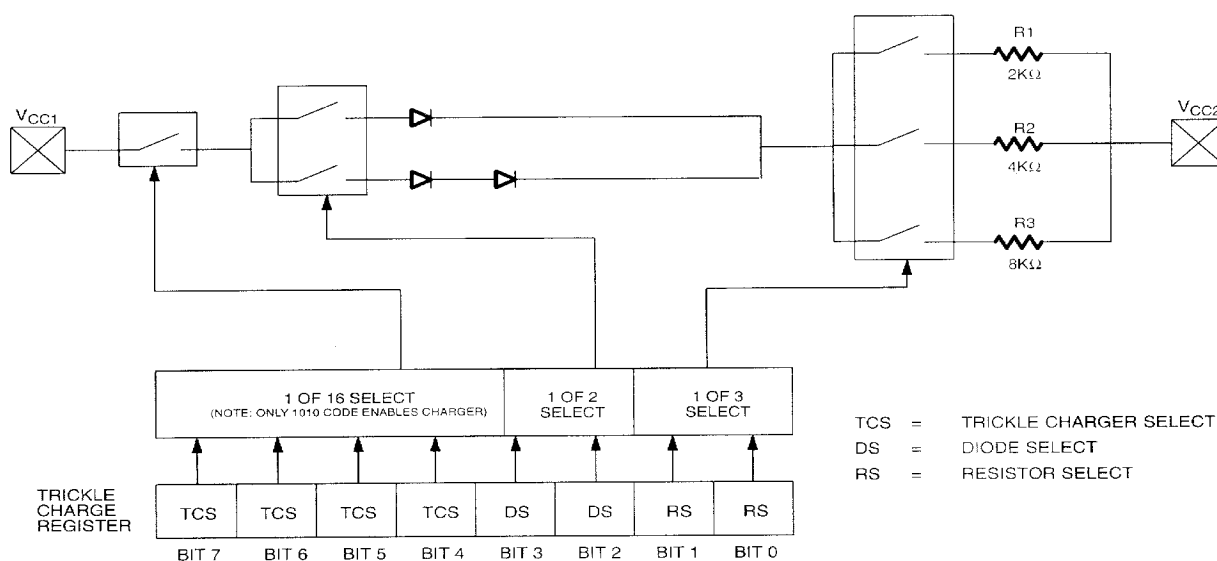
**IRQF0 (Interrupt 0 Request Flag)** – A logic 1 in the interrupt request flag bit indicates that the current time has matched the alarm 0 registers. If the AIE0 bit is also a logic 1, the  $\overline{\text{INT0}}$  pin will go low. IRQF0 is cleared when the address pointer goes to any of the alarm 0 registers during a read or write.

**IRQF1 (Interrupt 1 Request Flag)** – A logic 1 in the interrupt request flag bit indicates that the current time has matched the alarm 1 registers. This flag can be used to generate an interrupt on either  $\overline{\text{INT0}}$  or  $\overline{\text{INT1}}$  depending on the status of the INTCN bit in the control Register. If the INTCN bit is set to a logic 1 and IRQF1 is at a logic 1 (and AIE1 bit is also a logic 1), the  $\overline{\text{INT1}}$  pin will go low. If the INTCN bit is set to a logic 0 and IRQF1 is at a logic 1 (and AIE1 bit is also a logic 1), the  $\overline{\text{INT0}}$  pin will go low. IRQF1 is cleared when the address pointer goes to any of the alarm 1 registers during a read or write.

## TRICKLE CHARGE REGISTER (READ 11H, WRITE 91H)

This register controls the trickle charge characteristics of the DS1305. The simplified schematic of Figure 3 shows the basic components of the trickle charger. The trickle charge select (TCS) bits (bits 4-7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern of 1010 will enable the trickle charger. All other patterns will disable the trickle charger. On the initial application of power, the DS1305 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2-3) select whether one diode or two diodes are connected between  $V_{CC1}$  and  $V_{CC2}$ . The resistor select (RS) bits select the resistor that is connected between  $V_{CC1}$  and  $V_{CC2}$ . The resistor and diodes are selected by the RS and DS bits as shown in Table 2.

## PROGRAMMABLE TRICKLE CHARGER Figure 3





**TRICKLE CHARGER RESISTOR & DIODE SELECT Table 2**

TCS Bit 7	TCS Bit 6	TCS Bit 5	TCS Bit 4	DS Bit 3	DS Bit 2	RS Bit 1	RS Bit 0	FUNCTION
X	X	X	X	X	X	0	0	Disabled
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
1	0	1	0	0	1	0	1	1 Diode, 2k $\Omega$
1	0	1	0	0	1	1	0	1 Diode, 4k $\Omega$
1	0	1	0	0	1	1	1	1 Diode, 8k $\Omega$
1	0	1	0	1	0	0	1	2 Diodes, 2k $\Omega$
1	0	1	0	1	0	1	0	2 Diodes, 4k $\Omega$
1	0	1	0	1	0	1	1	2 Diodes, 8k $\Omega$

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5V is applied to  $V_{CC1}$  and a super cap is connected to  $V_{CC2}$ . Also assume that the trickle charger has been enabled with 1 diode and resistor R1 between  $V_{CC1}$  and  $V_{CC2}$ . The maximum current  $I_{MAX}$  would, therefore, be calculated as follows:

$$I_{MAX} = (5.0V - \text{diode drop}) / R1 \approx (5.0V - 0.7V) / 2k\Omega \approx 2.2mA$$

As the super cap charges, the voltage drop between  $V_{CC1}$  and  $V_{CC2}$  will decrease and, therefore, the charge current will decrease.

## POWER CONTROL

Power is provided through the  $V_{CC1}$ ,  $V_{CC2}$ , and  $V_{BAT}$  pins. Three different power supply configurations are illustrated in Figure 4. Configuration 1 shows the DS1305 being backed up by a non-rechargeable energy source such as a lithium battery. In this configuration, the system power supply is connected to  $V_{CC1}$  and  $V_{CC2}$  is grounded. The DS1305 will be write protected if  $V_{CC1}$  is less than  $V_{BAT}$ . The DS1305 will be fully accessible when  $V_{CC1}$  is greater than  $V_{BAT} + 0.2V$ .

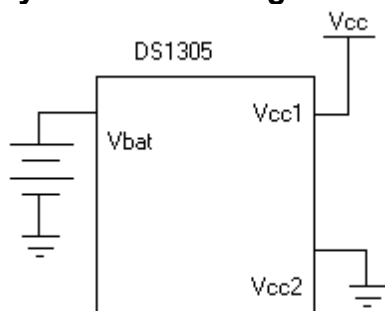
Configuration 2 illustrates the DS1305 being backed up by a rechargeable energy source. In this case, the  $V_{BAT}$  pin is grounded,  $V_{CC1}$  is connected to the primary power supply, and  $V_{CC2}$  is connected to the secondary supply (the rechargeable energy source). The DS1305 will operate from the larger of  $V_{CC1}$  or  $V_{CC2}$ . When  $V_{CC1}$  is greater than  $V_{CC2} + 0.2V$  (typical),  $V_{CC1}$  will power the DS1305. When  $V_{CC1}$  is less than  $V_{CC2}$ ,  $V_{CC2}$  will power the DS1305. The DS1305 does not write protect itself in this configuration.

Configuration 3 shows the DS1305 in battery operate mode where the device is powered only by a single battery. In this case, the  $V_{CC1}$  and  $V_{BAT}$  pins are grounded and the battery is connected to the  $V_{CC2}$  pin.

Only these three configurations are allowed. Unused supply pins must be grounded.

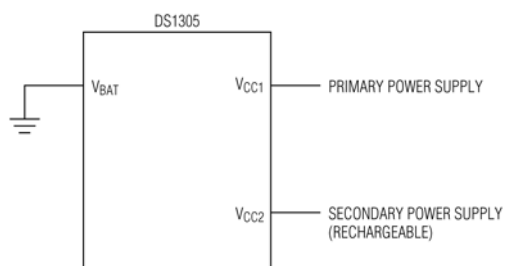
## POWER SUPPLY CONFIGURATIONS FOR THE DS1305 Figure 4

### Configuration 1: Backup Supply is a Nonrechargeable Lithium Battery



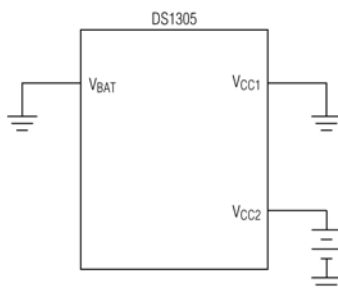
Note: Device is write protected if  $V_{CC} < V_{CCTP}$

### Configuration 2: Backup Supply is a Rechargeable Battery or Super Capacitor



**Note:** Device does not provide automatic write protection.

### Configuration 3: Battery Operate Mode



## SERIAL INTERFACE

The DS1305 offers the flexibility to choose between two serial interface modes. The DS1305 can communicate with the SPI interface or with a standard 3-wire interface. The interface method used is determined by the SERMODE pin. When this pin is connected to  $V_{CC}$ , SPI communication is selected. When this pin is connected to ground, standard 3-wire communication is selected.

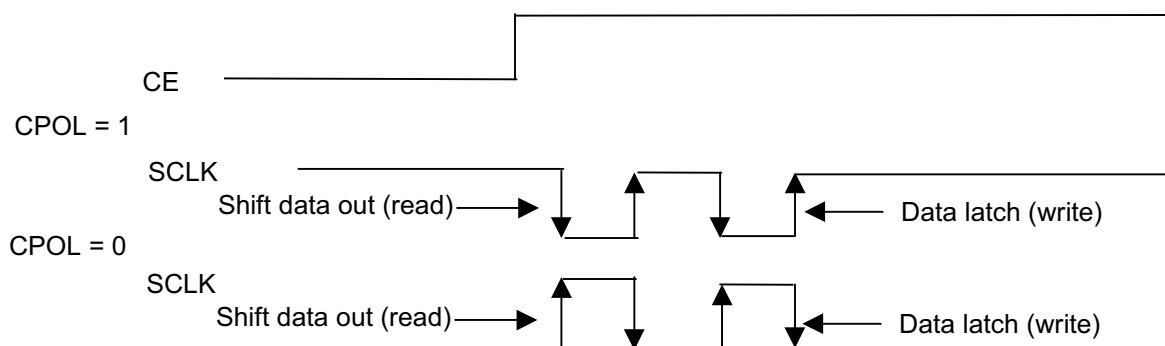
## SERIAL PERIPHERAL INTERFACE (SPI)

The serial peripheral interface (SPI) is a synchronous bus for address and data transfer, and is used when interfacing with the SPI bus on specific Motorola microcontrollers such as the 68HC05C4 and the 68HC11A8. The SPI mode of serial communication is selected by tying the SERMODE pin to  $V_{CC}$ . Four pins are used for the SPI. The four pins are the SDO (Serial Data Out), SDI (Serial Data In), CE (Chip Enable), and SCLK (Serial Clock). The DS1305 is the slave device in an SPI application, with the microcontroller being the master.

The SDI and SDO pins are the serial data input and output pins for the DS1305, respectively. The CE input is used to initiate and terminate a data transfer. The SCLK pin is used to synchronize data movement between the master (microcontroller) and the slave (DS1305) devices.

The shift clock (SCLK), which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus. The inactive clock polarity is programmable in some microcontrollers. The DS1305 determines the clock polarity by sampling SCLK when CE becomes active. Therefore, either SCLK polarity can be accommodated. Input data (SDI) is latched on the internal strobe edge and output data (SDO) is shifted out on the shift edge (Figure 5). There is one clock for each bit transferred. Address and data bits are transferred in groups of eight.

## SERIAL CLOCK AS A FUNCTION OF MICROCONTROLLER CLOCK POLARITY (CPOL) Figure 5



CPHA bit polarity (if applicable) may need to be set accordingly.

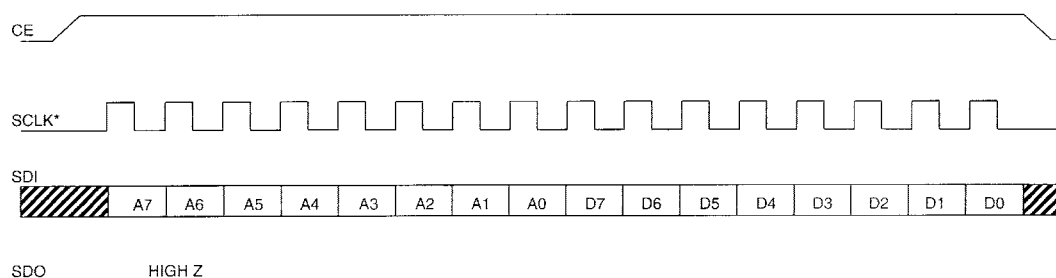
CPOL is a bit that is set in the microcontroller's control register.

SDO remains at High-Z until 8 bits of data are ready to be shifted out during a read.

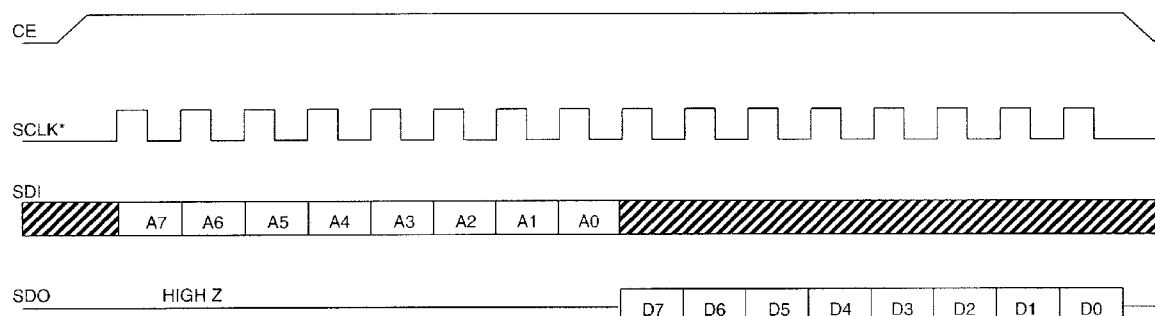
## ADDRESS AND DATA BYTES

Address and data bytes are shifted MSB first into the serial data input (SDI) and out of the serial data output (SDO). Any transfer requires the address of the byte to specify a write or read to either a RTC or RAM location, followed by one or more bytes of data. Data is transferred out of the SDO for a read operation and into the SDI for a write operation (see Figure 6 and 7).

## SPI SINGLE-BYTE WRITE Figure 6



## SPI SINGLE-BYTE READ Figure 7

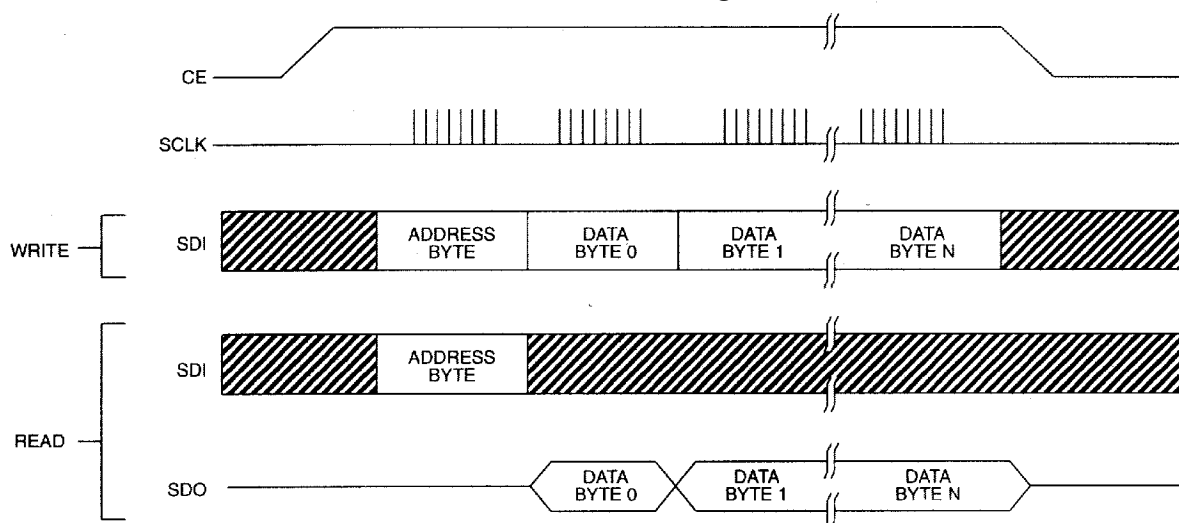


\*SCLK can be either polarity.

The address byte is always the first byte entered after CE is driven high. The most significant bit (A7) of this byte determines if a read or write will take place. If A7 is 0, one or more read cycles will occur. If A7 is 1, one or more write cycles will occur.

Data transfers can occur 1 byte at a time or in multiple-byte burst mode. After CE is driven high an address is written to the DS1305. After the address, one or more data bytes can be written or read. For a single-byte transfer 1 byte is read or written and then CE is driven low. For a multiple-byte transfer, however, multiple bytes can be read or written to the DS1305 after the address has been written. Each read or write cycle causes the RTC register or RAM address to automatically increment. Incrementing continues until the device is disabled. When the RTC is selected, the address wraps to 00h after incrementing to 1Fh (during a read) and wraps to 80h after incrementing to 9Fh (during a write). When the RAM is selected, the address wraps to 20h after incrementing to 7Fh (during a read) and wraps to A0h after incrementing to FFh (during a write).

## SPI MULTIPLE-BYTE BURST TRANSFER Figure 8



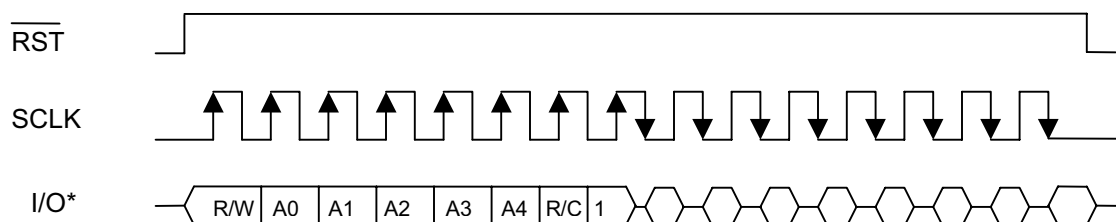
## 3-WIRE INTERFACE

The 3-wire interface mode operates similarly to the SPI mode. However, in 3-wire mode there is one I/O instead of separate data in and data out signals. The 3-wire interface consists of the I/O (SDI and SDO pins tied together), CE, and SCLK pins. In 3-wire mode, each byte is shifted in LSB first unlike SPI mode where each byte is shifted in MSB first.

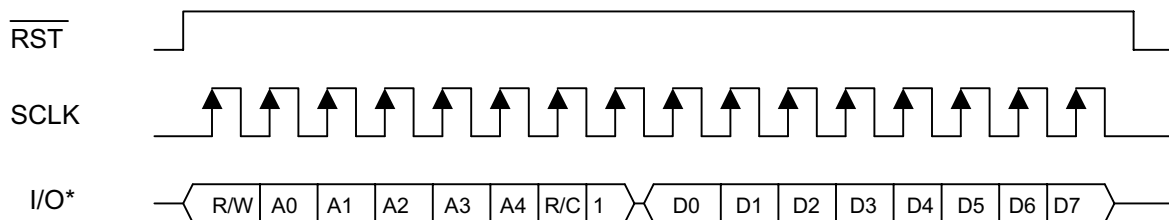
As is the case with the SPI mode, an address byte is written to the device followed by a single data byte or multiple data bytes. Figure 9 illustrates a read and write cycle. In 3-wire mode, data is input on the rising edge of SCLK and output on the falling edge of SCLK.

### 3-WIRE SINGLE-BYTE TRANSFER Figure 9

#### SINGLE BYTE READ



#### SINGLE BYTE WRITE



In burst mode,  $\overline{\text{RST}}$  is kept high and additional SCLK cycles are sent until the end of the burst.

\*I/O is SDI and SDO tied together.

**ABSOLUTE MAXIMUM RATINGS\***

Voltage Range on Any Pin Relative to Ground	-0.5V to +7.0V
Storage Temperature Range	-55°C to +125°C
Soldering Temperature range	260°C for 10 seconds

\*This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

**OPERATING RANGE**

RANGE	TEMP RANGE (°C)	V <sub>CC</sub> (V)
Commercial	0 to +70	2.0 to 5.5 V <sub>CC1</sub> or V <sub>CC2</sub>
Industrial	-40 to +85	2.0 to 5.5 V <sub>CC1</sub> or V <sub>CC2</sub>

**RECOMMENDED DC OPERATING CONDITIONS** Over the operating range\*

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Supply Voltage V <sub>CC1</sub> , V <sub>CC2</sub>	V <sub>CC1</sub> , V <sub>CC2</sub>		2.0		5.5	V	7
Logic 1 Input	V <sub>IH</sub>		2.0		V <sub>CC</sub> + 0.3	V	
Logic 0 Input	V <sub>IL</sub>	V <sub>CC</sub> = 2.0V	-0.3		+0.3	V	
		V <sub>CC</sub> = 5V	-0.3		+0.8		
V <sub>BAT</sub> Battery Voltage	V <sub>BAT</sub>		2.0		5.5	V	
V <sub>CCIF</sub> Supply Voltage	V <sub>CCIF</sub>		2.0		5.5	V	11

\*Unless otherwise specified.

**DC ELECTRICAL CHARACTERISTICS**

Over the operating range\*

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Input Leakage	$I_{LI}$		-100		+500	$\mu A$	
Output Leakage	$I_{LO}$		-1		1	$\mu A$	
Logic 0 Output $I_{OL} = 1.5mA$ $I_{OL} = 4.0mA$	$V_{OL}$	$V_{CC} = 2.0V$			0.4	V	
		$V_{CC} = 5V$			0.4		
Logic 1 Output $I_{OH} = -0.4mA$ $I_{OH} = -1.0mA$	$V_{OH}$	$V_{CCIF} = 2.0V$	1.6			V	
		$V_{CCIF} = 5V$	2.4				
$V_{CC1}$ Active Supply Current	$I_{CC1A}$	$V_{CC1} = 2.0V$			0.425	mA	2, 8
		$V_{CC1} = 5V$			1.28		
$V_{CC1}$ Timekeeping Current (Osc on)	$I_{CC1T}$	$V_{CC1} = 2.0V$			25.3	$\mu A$	1, 8, 12
		$V_{CC1} = 5V$			81		
$V_{CC1}$ Standby Current (Osc off)	$I_{CC1S}$	$V_{CC1} = 2.0V$			25	$\mu A$	6, 8, 12
		$V_{CC1} = 5V$			80		
$V_{CC2}$ Active Supply Current	$I_{CC2A}$	$V_{CC2} = 2.0V$			0.4	mA	2, 9
		$V_{CC2} = 5V$			1.2		
$V_{CC2}$ Timekeeping Current (Osc on)	$I_{CC2T}$	$V_{CC2} = 2.0V$			0.3	$\mu A$	1, 9, 12
		$V_{CC2} = 5V$			1		
$V_{CC2}$ Standby Current (Osc off)	$I_{CC2S}$	$V_{CC2} = 2.0V$			200	nA	6, 9, 12
		$V_{CC2} = 5V$			200		
Battery Timekeeping Current	$I_{BAT}$	$V_{BAT} = 3V$			400	nA	10, 12
Battery Standby Current	$I_{BATS}$	$V_{BAT} = 3V$			200	nA	10, 12
$V_{CC}$ Trip Point	$V_{CCTP}$		$V_{BAT} - 50$		$V_{BAT} + 200$	mV	
Trickle Charge Resistors	R1			2		k $\Omega$	
	R2			4		k $\Omega$	
	R3			8		k $\Omega$	
Trickle Charge Diode Voltage Drop	$V_{TD}$			0.7		V	

\*Unless otherwise specified.

**CAPACITANCE**(T<sub>A</sub> = +25°C)

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_I$		10		pF	
Output Capacitance	$C_O$		15		pF	
Crystal Capacitance	$C_X$		6		pF	

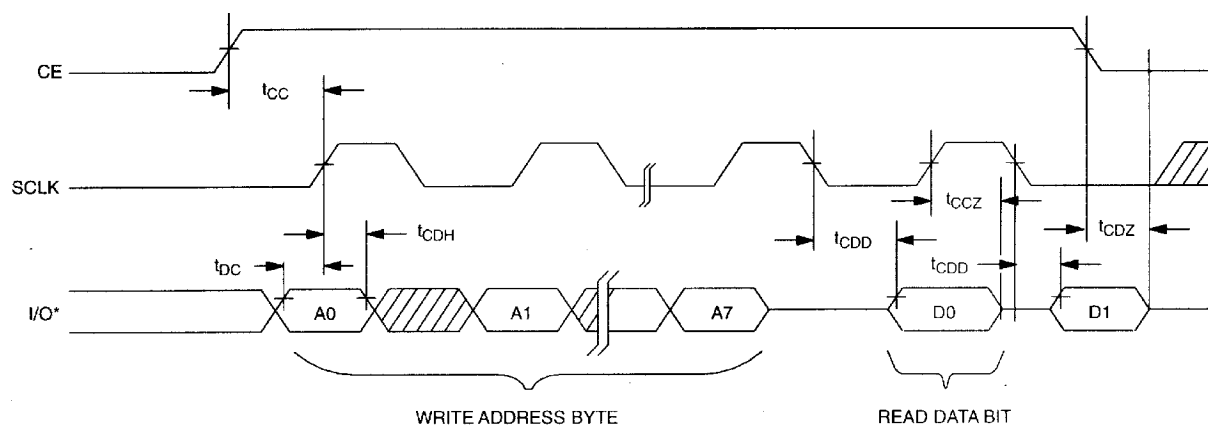


**3-WIRE AC ELECTRICAL CHARACTERISTICS**

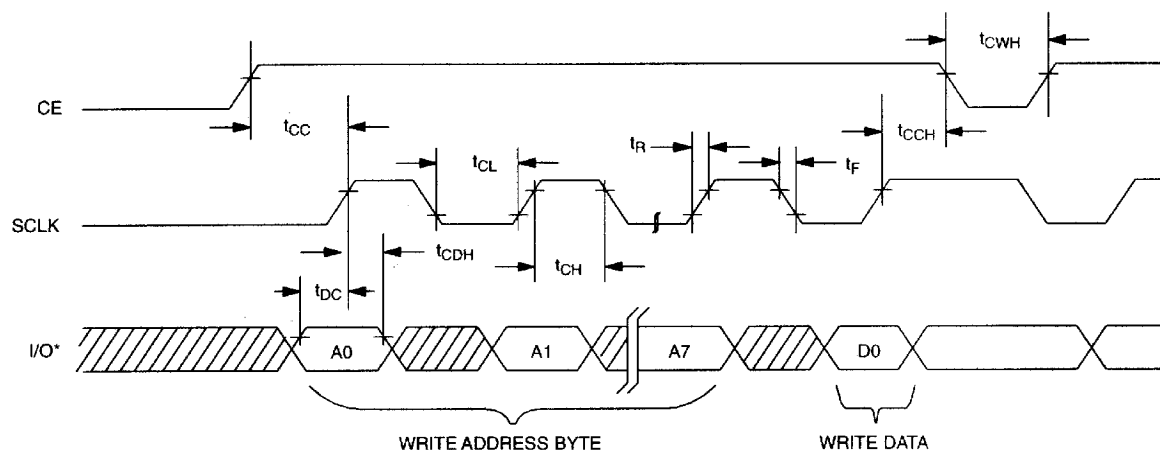
Over the operating range\*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	$t_{DC}$	$V_{CC} = 2.0V$	200		ns	3,4
		$V_{CC} = 5V$	50			
CLK to Data Hold	$t_{CDH}$	$V_{CC} = 2.0V$	280		ns	3,4
		$V_{CC} = 5V$	70			
CLK to Data Delay	$t_{CDD}$	$V_{CC} = 2.0V$		800	ns	3,4,5
		$V_{CC} = 5V$		200		
CLK Low Time	$t_{CL}$	$V_{CC} = 2.0V$	1000		ns	4
		$V_{CC} = 5V$	250			
CLK High Time	$t_{CH}$	$V_{CC} = 2.0V$	1000		ns	4
		$V_{CC} = 5V$	250			
CLK Frequency	$t_{CLK}$	$V_{CC} = 2.0V$		0.6	MHz	4
		$V_{CC} = 5V$	DC	2.0		
CLK Rise and Fall	$t_R, t_F$	$V_{CC} = 2.0V$		2000	ns	
		$V_{CC} = 5V$		500		
CE to CLK Setup	$t_{CC}$	$V_{CC} = 2.0V$	4		$\mu s$	4
		$V_{CC} = 5V$	1			
CLK to CE Hold	$t_{CCH}$	$V_{CC} = 2.0V$	240		ns	4
		$V_{CC} = 5V$	60			
CE Inactive Time	$t_{CWH}$	$V_{CC} = 2.0V$	4		$\mu s$	4
		$V_{CC} = 5V$	1			
CE to Output High Z	$t_{CDZ}$	$V_{CC} = 2.0V$		280	ns	3,4
		$V_{CC} = 5V$		70		
SCLK to Output High Z	$t_{CCZ}$	$V_{CC} = 2.0V$		280	ns	3,4
		$V_{CC} = 5V$		70		

\*Unless otherwise specified.

**TIMING DIAGRAM: 3-WIRE READ DATA TRANSFER** Figure 10

# TIMING DIAGRAM: 3-WIRE WRITE DATA TRANSFER Figure 11



\* I/O is SDI and SDO tied together.

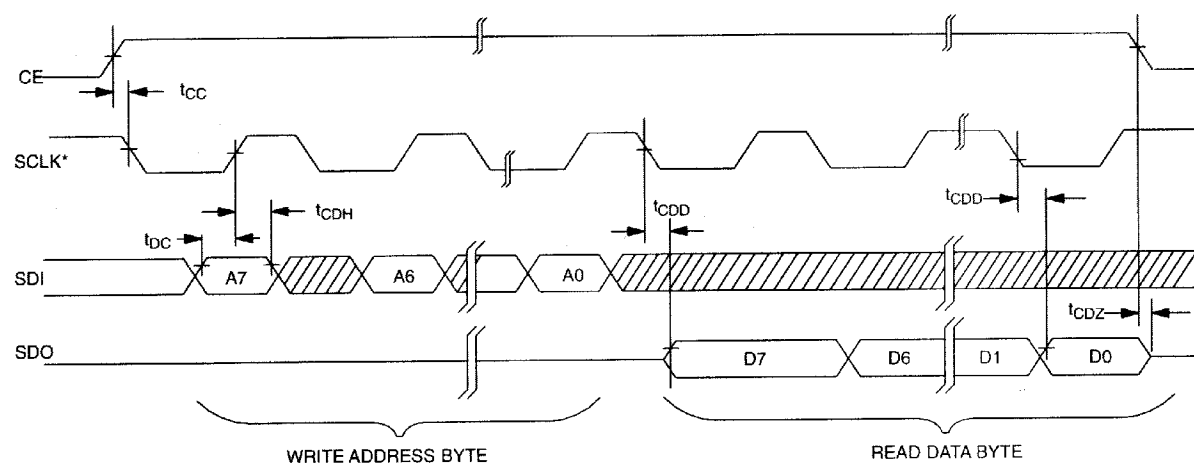
## SPI AC ELECTRICAL CHARACTERISTICS

Over the operating range\*

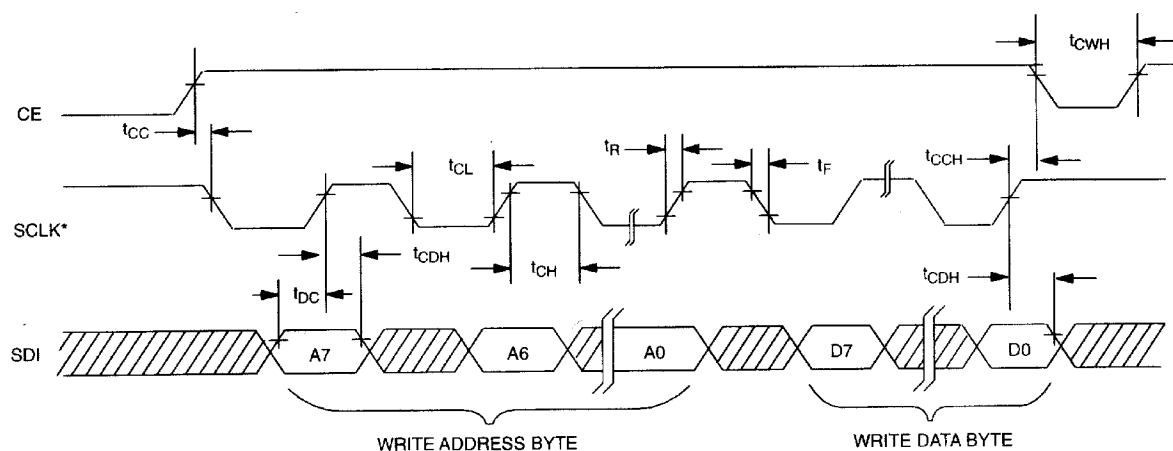
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	$t_{DC}$	$V_{CC} = 2.0V$	200		ns	5,6
		$V_{CC} = 5V$	50			
CLK to Data Hold	$t_{CDH}$	$V_{CC} = 2.0V$	280		ns	5,6
		$V_{CC} = 5V$	70			
CLK to Data Delay	$t_{CDD}$	$V_{CC} = 2.0V$		800	ns	5,6,7
		$V_{CC} = 5V$		200		
CLK Low Time	$t_{CL}$	$V_{CC} = 2.0V$	1000		ns	6
		$V_{CC} = 5V$	250			
CLK High Time	$t_{CH}$	$V_{CC} = 2.0V$	1000		ns	6
		$V_{CC} = 5V$	250			
CLK Frequency	$t_{CLK}$	$V_{CC} = 2.0V$		0.6	MHz	6
		$V_{CC} = 5V$	DC	2.0		
CLK Rise and Fall	$t_R, t_F$	$V_{CC} = 2.0V$		2000	ns	
		$V_{CC} = 5V$		500		
CE to CLK Setup	$t_{CC}$	$V_{CC} = 2.0V$	4		$\mu s$	6
		$V_{CC} = 5V$	1			
CLK to CE Hold	$t_{CCH}$	$V_{CC} = 2.0V$	240		ns	6
		$V_{CC} = 5V$	60			
CE Inactive Time	$t_{CWH}$	$V_{CC} = 2.0V$	4		$\mu s$	6
		$V_{CC} = 5V$	1			
CE to Output High-Z	$t_{CDZ}$	$V_{CC} = 2.0V$		280	ns	5,6
		$V_{CC} = 5V$		70		

\*Unless otherwise specified.

# TIMING DIAGRAM: SPI READ DATA TRANSFER Figure 12



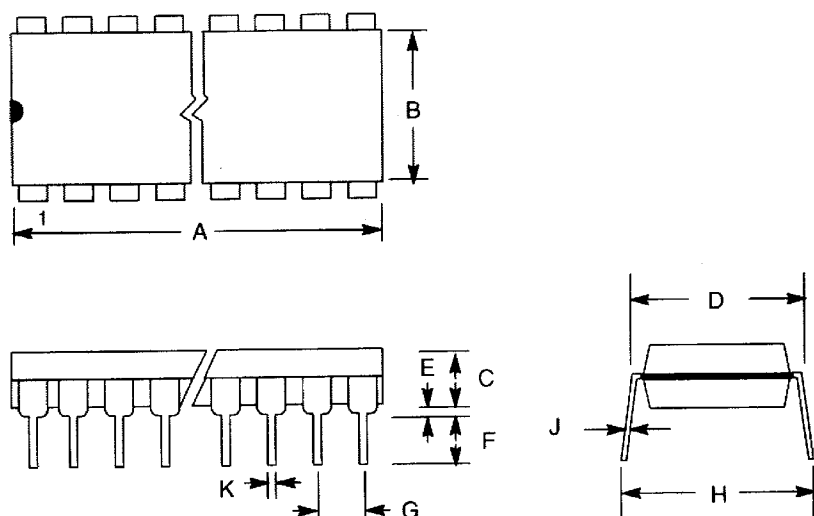
# TIMING DIAGRAM: SPI WRITE DATA TRANSFER Figure 13



\* SCLK can be either polarity, timing shown for CPOL = 1.

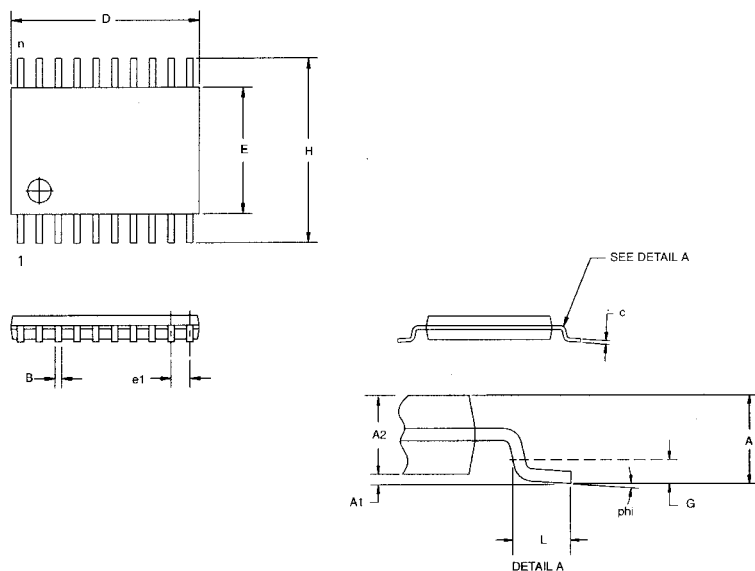
**NOTES:**

1.  $I_{CC1T}$  and  $I_{CC2T}$  are specified with CE set to a logic 0 and  $\overline{EOSC}$  bit = 0 (oscillator enabled).
2.  $I_{CC1A}$  and  $I_{CC2A}$  are specified with  $CE = V_{CC}$ ,  $SCLK = 2MHz$  at  $V_{CC} = 5V$ ;  $SCLK = 500kHz$  at  $V_{CC} = 2.0V$ ,  $V_{IL} = 0V$ ,  $V_{IH} = V_{CC}$ , and  $\overline{EOSC}$  bit = 0 (oscillator enabled).
3. Measured at  $V_{IH} = 2.0V$  or  $V_{IL} = 0.8V$  and 10ms maximum rise and fall time.
4. Measured with 50pF load.
5. Measured at  $V_{OH} = 2.4V$  or  $V_{OL} = 0.4V$ .
6.  $I_{CC1S}$  and  $I_{CC2S}$  are specified with CE set to a logic 0. The  $\overline{EOSC}$  bit must be set to logic 1 (oscillator disabled).
7.  $V_{CC} = V_{CC1}$ , when  $V_{CC1} > V_{CC2} + 0.2V$  (typical);  $V_{CC} = V_{CC2}$ , when  $V_{CC2} > V_{CC1}$ .
8.  $V_{CC2} = 0V$ .
9.  $V_{CC1} = 0V$ .
10.  $V_{CC1} < V_{BAT}$ .
11.  $V_{CCIF}$  must be less than or equal to the largest of  $V_{CC1}$ ,  $V_{CC2}$ , and  $V_{BAT}$ .
12. Using a crystal on X1 and X2, rated for 6pF load.

**DS1305 16-PIN DIP (300MIL)**

PKG	16-PIN	
DIM	MIN	MAX
A IN	0.740	0.780
MM	18.80	19.81
B IN	0.240	0.260
MM	6.10	6.60
C IN	0.120	0.140
MM	3.05	3.56
D IN	0.300	0.325
MM	7.62	8.26
E IN	0.015	0.040
MM	0.38	1.02
F IN	0.120	0.140
MM	3.05	3.56
G IN	0.090	0.110
MM	2.29	2.79
H IN	0.320	0.370
MM	8.13	9.40
J IN	0.008	0.012
MM	0.20	0.30
K IN	0.015	0.021
MM	0.38	0.53

# DS1305 20-PIN TSSOP



PKG	20-PIN	
DIM	MIN	MAX
A MM	-	1.10
A1 MM	0.05	-
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°