

### FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818B and DS1287A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap-year compensation valid up to 2100
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general-purpose RAM
- Programmable square-wave output signal
- Bus-compatible interrupt signals ( $\overline{\text{IRQ}}$ )
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 $\mu$ s to 500ms
  - End-of-clock update cycle

### PIN ASSIGNMENT

MOT	1	24	$V_{CC}$
NC	2	23	$\overline{\text{SQW}}$
NC	3	22	NC
AD0	4	21	$\overline{\text{RCLR}}$
AD1	5	20	NC
AD2	6	19	$\overline{\text{IRQ}}$
AD3	7	18	$\overline{\text{RESET}}$
AD4	8	17	DS
AD5	9	16	NC
AD6	10	15	$\overline{\text{R/W}}$
AD7	11	14	AS
GND	12	13	$\overline{\text{CS}}$

DS12887A  
24-Pin Encapsulated Package

### PIN DESCRIPTION

AD0–AD7	- Multiplexed Address/Data Bus
NC	- No Connection
MOT	- Bus Type Selection
$\overline{\text{CS}}$	- Chip Select
AS	- Address Strobe
$\overline{\text{R/W}}$	- Read/Write Input
DS	- Data Strobe
$\overline{\text{RESET}}$	- Reset Input
$\overline{\text{IRQ}}$	- Interrupt Request Output
$\overline{\text{SQW}}$	- Square-Wave Output
$V_{CC}$	- +5V Supply
$\overline{\text{RCLR}}$	- RAM Clear
GND	- Ground

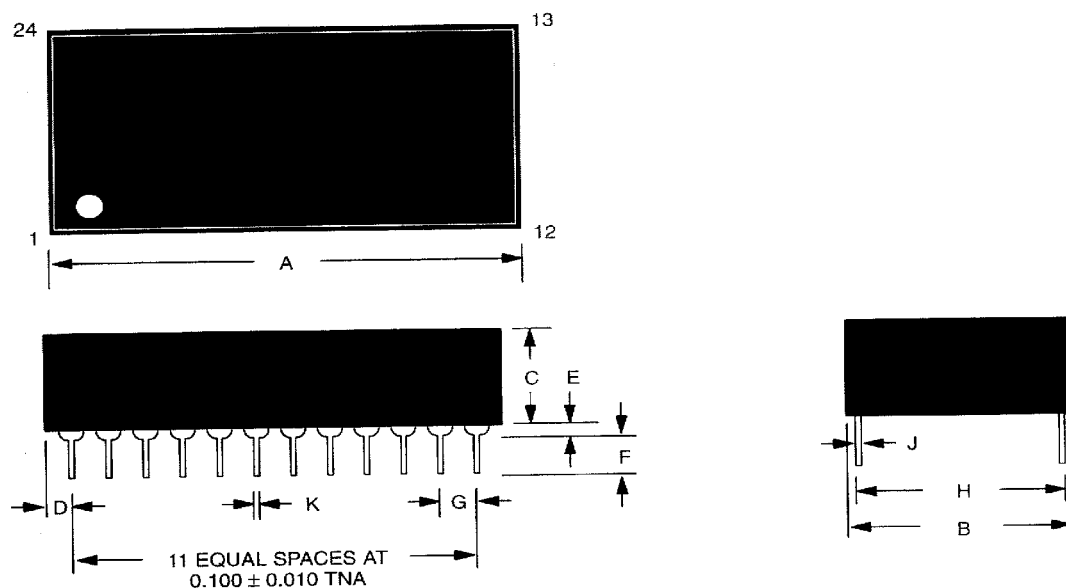
### DESCRIPTION

The DS12887A real-time clock plus RAM is designed to be a direct replacement for the DS1287A. The DS12887A is identical in form, fit, and function to the DS1287A, and includes additional 64 bytes of general-purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. The  $\overline{\text{RCLR}}$  pin is used to clear (set to logic 1) all 114 bytes of general purpose RAM but does not affect the RAM associated with the real-time clock. In order to clear the RAM,  $\overline{\text{RCLR}}$  must be forced to an input logic 0 (-0.3V to +0.8V) during battery-backup mode

when  $V_{CC}$  is not applied. The  $\overline{RCLR}$  function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers.

For a complete description of operating conditions, electrical characteristics, bus timing and pin descriptions other than  $\overline{RCLR}$ , see the DS12887 data sheet.

## DS12887A REAL-TIME CLOCK PLUS RAM



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.320	1.335
MM	33.53	33.91
B IN.	0.675	0.700
MM	17.15	17.78
C IN.	0.345	0.370
MM	8.76	9.40
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

**Note:** Pins 2, 3, 16, 20, and 22 are missing by design. This device cannot be stored or shipped in conductive material that will give a continuity path between the RAM clear pin and ground.