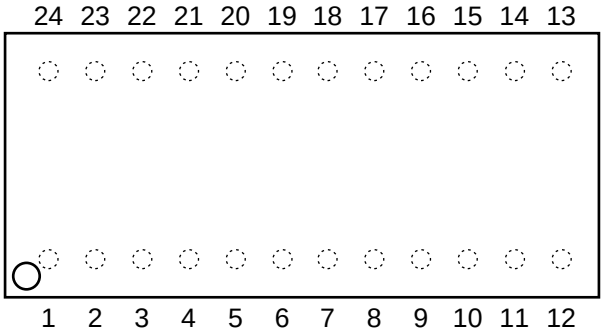
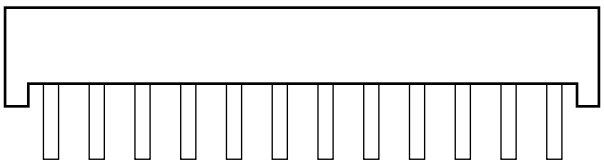
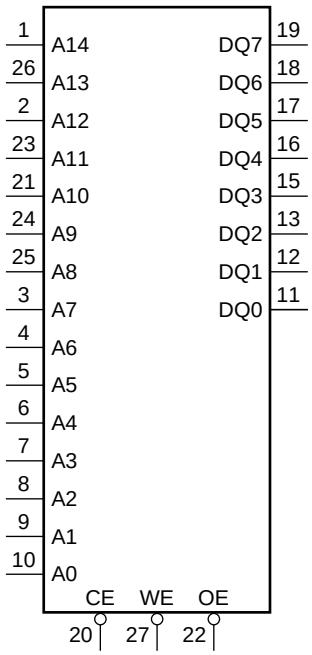
# C-MOS 256 K (32,768 × 8)-BIT NONVOLATILE STATIC RAM

—TOP/SIDE VIEW—






| PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL |
|---|---|---|---|---|---|
| 1 | I | A14 | 15 | I/O | DQ3 |
| 2 | I | A12 | 16 | I/O | DQ4 |
| 3 | I | A7 | 17 | I/O | DQ5 |
| 4 | I | A6 | 18 | I/O | DQ6 |
| 5 | I | A5 | 19 | I/O | DQ7 |
| 6 | I | A4 | 20 | I/O | $\overline{CE}$ |
| 7 | I | A3 | 21 | I | A10 |
| 8 | I | A2 | 22 | I/O | $\overline{OE}$ |
| 9 | I | A1 | 23 | I | A11 |
| 10 | I | A0 | 24 | I | A9 |
| 11 | I/O | DQ0 | 25 | I | A8 |
| 12 | I/O | DQ1 | 26 | I | A13 |
| 13 | I/O | DQ2 | 27 | I/O | $\overline{WE}$ |
| 14 | — | GND | 28 | — | $V_{DD}$ |

**INPUT**

A0 - A14 : ADDRESS

**INPUT/OUTPUT**

$\overline{CE}$ : CHIP ENABLE

DQ0 - DQ7 : DATA

$\overline{OE}$ : OUTPUT ENABLE

$\overline{WE}$ : WRITE ENABLE