SIEMENS

Memory Products

Modular embedded DRAM

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1 Introduction

Modular embedded DRAM is the core of a new service provided by the **SIEMENS** Memory Products group. Custom logic can be combined with the latest **SIEMENS** dynamic memory technology providing application specific embedded DRAM solutions manufactured by **SIEMENS**. Modular embedded DRAM is based on 256 Kbit DRAM building blocks. A library of core modules allows the fast creation of dynamic memory optimized for specific applications. Memory modules of up to 16 Mbit can be customized increment steps of 256 Kbit.

The synchronous interface of Modular embedded DRAM operates at high speed using fast page mode access. Optional multibank operation allows high performance applications. Multiple block configurations enable large data busses with up to 512 bit bus width. The resulting maximum bus throughput rate is 42.4 Gbit/s at a clock frequency of 83 MHz. Programmable pipeline stages of depth one, two or three stages allow to optimize data transmission by trading clock frequency for latency.

Application examples include signal processing or graphics devices which benefit from the large bandwidth of the wide on-chip interface. Dedicated memory architectures with customized memory modules are supported.

This product overview describes features and application of the 256 Kbit DRAM memory block DRM256 for custom memory modules between 256 Kbit and 16 Mbit.

The 256 Kbit DRAM Core is available today in the latest **SIEMENS** 0.35µ 16-MBit trench technology, enhanced with up to four metal layers. It works from a 3.3 Volt supply.

1.1 Features

- 256 Kbit DRAM building block for memories of up to 16Mbit in customized bank configurations
- Wide configurable interface, up to 512 bit
- Optional BIST with on-chip test controller
- LATENCY 1, 2 and 3 modes
- 256 refresh cycles in 64ms refresh interval
- 1024 local sense amps per block
- 2 redundant rows per block
- 1-T trench capacitor DRAM cells
- Chip area < 8.8 mm² for 2 Mbit with customized interface
- Less than 1.5mW/MHz power consumption per active building block
- 0.35µ CMOS process, up to 4 metal layers
- 3.3V operating voltage

1.2 Block Diagram

Modular embedded DRAM includes three main parts: The actual DRAM, an optional test controller, and a power supply unit. The power supply unit includes a stabilized 2.5 Volt supply for the memory core and an n-well voltage generator for the memory cell transistors. The test controller allows different test options from direct access to built-in self test. Only one test controller and one power supply unit are necessary per device, independently from the number of embedded DRAM cores.

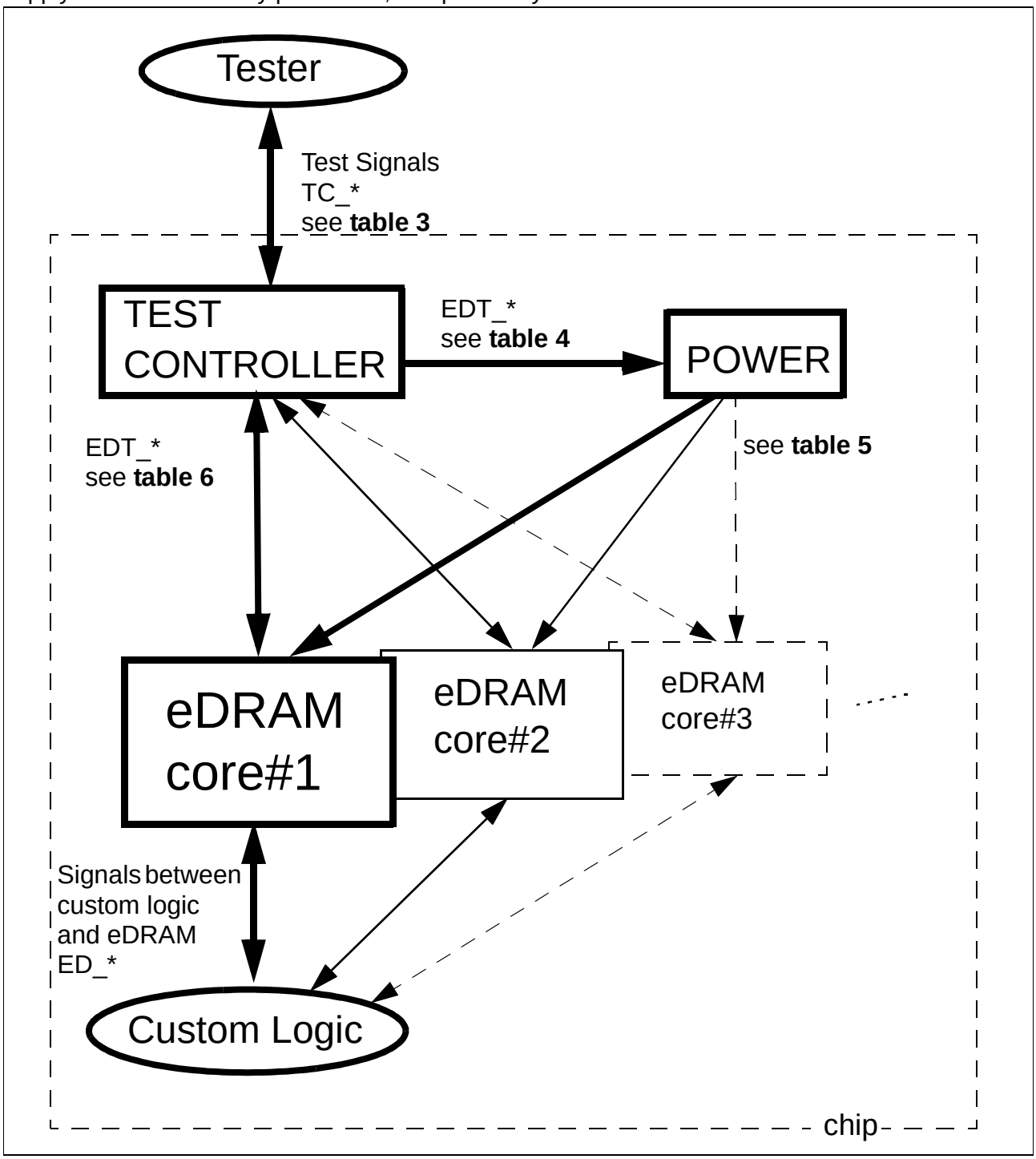

Figure 1
Block Diagram

1.3 Signal Definitions and Functions

The following tables group the signals according to their functions. They include signal name, bus width, direction and a brief description of the function. As depicted in figure 1, signals are grouped into five different clusters as follows:

- “ED_“ signals are connections between the embedded DRAM core and the custom logic part or the power module, see table 2 in section 1.3.1 and table 5 in section 1.3.3, respectively.
- “TC_” signals are connections between the Test Controller and the tester, see table 3 in section 1.3.2.
- “EDT_” signals are connections between Test Controller and either the DRAM core or the power unit, see table 6 in section 1.3.3 and table 4 in section 1.3.3, respectively.

1.3.1 Signals from Custom Logic to DRAM

Table 1
Power Supply Signals

VDD	3.3V +/-10% supply voltage
GND	0V

Table 2
Input Signals from Custom Logic, Output Signals to Custom Logic

Signal Name	Width	Direction at DRAM	Description
ED_CLK	1	I	**CLOCK:** Input to the internal clock buffer of the memory module. CLK can be kept at low for minimum power dissipation.
ED_CKE	1	I	**CLOCK ENABLE:** 1: The internal clock of the memory module is running and the module is ready for operation. 0: The internal clock is stopped and the memory module is in standby. Note that there is no automatic refresh.
ED_RESETN	1	I	**RESET:** Asynchronous input, active low. The memory module is reset while set to „0“. Should be applied together with reset of the entire chip.
ED_CMD[3:0]	4	I	**COMMAND:** Controls the operation of the memory module.The value has to be valid at the rising edge of CLK.
ED_BROW[]	b	I	**BANK ROW:** Selects one bank for a row access. The width of the bus depends on the application configuration of the memory module. The value has to be valid at the rising edge of CLK. Connect o GND, if only one bank is implemented.

ED_AROW[7:0]	8	I	**ADDRESS ROW:** Selects one of the memory modules for a page access. 8 row addresses are available. The value has to be valid at the rising edge of CLK.
ED_BCOL[]	b	I	**BANK COLUMN:** Selects one bank for a column access. The width of the bus depends on the application configuration of the memory module. BROW has the same width as BCOL. The value has to be valid at the rising edge of CLK. Connect o GND, if only one bank is implemented.
ED_ACOL[]	c	I	**ADDRESS COLUMN:** Selects one word of the open page. The width of the bus depends on the application configuration of the memory module, see section 3. The value has to be valid at the rising edge of CLK.
ED_LAT[]	3	I	**LATENCY:** Activates the registers in the data path. Three stages are implemented. Asynchronous signals. Data on this bus must be valid for a complete access. Changes are only allowed while all memory banks of a memory module are in the precharge state.
ED_DI[]	w	I	**DATA INPUT:** Input data bus.The width is application dependent and is the same as DO[].
ED_BWE[]	w/8	I	**Byte Write Enable:** Enables a write operation for 8 bit of the data word if set to 1. Width is equal to wordwidth divided by 8. Set to 1 if not used.
ED_OEN	1	I	**OUTPUT ENABLE:** 0: The tri-state buffers of DO[] are active for data output. 1: The tri-state buffers of DO[] are switched off. Asynchronous signal, active low. Connect to a fixed level if not used.
ED_GROUP	1	I	**GROUP:** This signal is used during the ACTIVATE and PRECHARGE commands. It selects a group of memory blocks.
ED_DO[]	w	O	**DATA OUTPUT:** Data put bus. The width is application dependent and is the same as DI[]. /OE controls the state of the buffers.

Definitions:

w is the word width of the data bus and is currently 16, 32, 64 or 128.

b for b_addrwidth, used to select a bank.

c for col_addrwidth, used to select a column.

1.3.2 Signals to Tester Interface

These signals must be connected to external pads during test. A pad for wafer test and analysis is required; this pad is typically not bonded, as the n-well is driven from the n-well pump.

Table 3
Signals to the Test Controller

Signal Name	Width	Direction at TC	Description
TC_DI[15:0]	16	I	Test Controller Data In
TC_DO[15:0]	16	O	Test Controller Data Out
TC_DDIR	1	I	**I/O Data Pad Direction Select:** Select direction of data at pad. TC_DI and TC_DO are connected to one bidirectional pad. 1:Input 0:Outpout
TC_ADDR [7:0]	8	I	Test Controller Address Bus
TC_CMD [3:0]	4	I	Test Controller Command Bus
TC_FAIL	1	O	Output Fail Indication 1:fail 0:no problems
TC_CLK	1	I	Controller Clock[1)]
TC_RESN	1	I	Test Controller Reset (active low)
TC_BURNIN	1	I	set Burn in mode (active high)
TC_MARCH	1	I	Set March Test Mode (active high)
TC_TEST	1	I	Activate Test Controller (active high)

1) The signal TC_CLK is also used for the DRAM core. Connect to the Test Controller and to the DRAM core via the Clock Select Multiplexer.

1.3.3 Internal Signals

Internal signals are signals that connect the different blocks but are neither connected to the custom logic nor used for test access. These signals have to be connected during the routing of the embedded DRAM product.

Table 4
Signals from Test Controller to Voltage Regulator & Margin Generator:

Signal Name	Width	Direction at TC	Description
EDT_REG_ON	1	O	Voltage regulator on (active high)
EDT_MARGIN[4:0]	5	O	Set Margin Voltage Steps (active high)
EDT_MARG_OFF	1	O	Disable Margin Generator variable margin (active high)

Table 5
Signals from Power Module to DRAM cores

Signal Name	Width	Direction at DRAM	Description
ED_V25	1	I	2,5V for the DRAM core
ED_NWA	1	I	n-Well Voltage
EDT_MARX	1	I	Voltage for margin test

Table 6
Signals from Test Controller to DRAM Cores:

Signal Name	Width	Direction at TC	Description
EDT_BROW [3:0]	4	O	Bank Row and Col are equal and come from Load Bank [3:0]
EDT_BCOL [3:0]	4	O	Bank Row and Col are equal and come from Load Bank [3:0]
EDT_AROW[7:0]	8	O	Test Address Row
EDT_ACOL[6:0]	5	O	Test Address Column
EDT_RESETN	1	O	Test Reset for DRAM core
EDT_CMD[3:0]	4	O	DRAM Command Bus
EDT_DI[3:0]	4	O	DRAM Data Input
EDT_DO[15:0]	16	I	DRAM Data Output
EDT_LAT[2:0]	3	O	latency 1, 2 or 3
EDT_GROUP	1	O	Group: Selection of a group of memory blocks
EDT_CKE[]	m	O	Test Clock Enable;
EDT_OEN[]	m	O	Output Enable
EDT_TEST_MUX[]	m	O	**Test Select (Multiplexer)** 0: Normal mode 1: Test mode
EDT_CLK_MUX[]	m	O	**Clock Select (Multiplexer)** 0: Normal mode 1: Test mode
Test Modi			
EDT_REDTST	1	O	Redundancy Test On
EDT_BOFF	1	O	Bit Redundancy Off
EDT_ROFF	1	O	Row Redundancy Off
EDT_MWLS	1	O	MWL Select test mode enabled
EDT_BOOST_OFF	1	O	Boost Off (cf. Margin control)
EDT_WBI	1	O	Wafer Burn In test mode en.
EDT_COMP	1	O	Compare Output Bits
EDT_SELW	2	O	Output Multiplexer

Definition:

m is the number of memory module connected to one test controller.

2 Device Integration

The integration of Modular embedded DRAM into an application specific circuit is part of the service provided by **SIEMENS**. Given the specific requirements of the DRAM core and the application specific logic, **SIEMENS** provides design integration and manufacturing of the device.The following main steps are applied to create an embedded DRAM product:

- Siemens provides all necessary information for the design of the custom logic part, i.g. design rules, timing parameters etc.
- The DRAM module has to be specified as given in section 3.4. A parameterizable VHDL model is available for device level simulations (see section 3.3). Siemens generates the design and provides all views. An abstract view is provided to be placed in the layout of the product in advance.
- A test concept has to be selected. The test controller is provided in form of a VHDL netlist. It can be synthesized together with the custom logic part. The test concept is described in detail in section 5.
- Test software for the DRAM part can be provided by Siemens, depending on the tester equipment and the selected test concept.
- Mask making and manufacturing are performed by Siemens.
- Testing of the DRAM is done by Siemens, while the custom logic part may be tested by the customer himself. Intellectual property residing in the custom logic completely remains with the customer.

This document describes architecture, test concept, and electrical parameters of Modular embedded DRAM. Note that this document focusses on Modular embedded DRAM, while standard DRAM cores with customized interface are available as well.

The design flow may start at different entry points, depending on the extent of the cooperation. See figure 2 for an overview of the design flow.

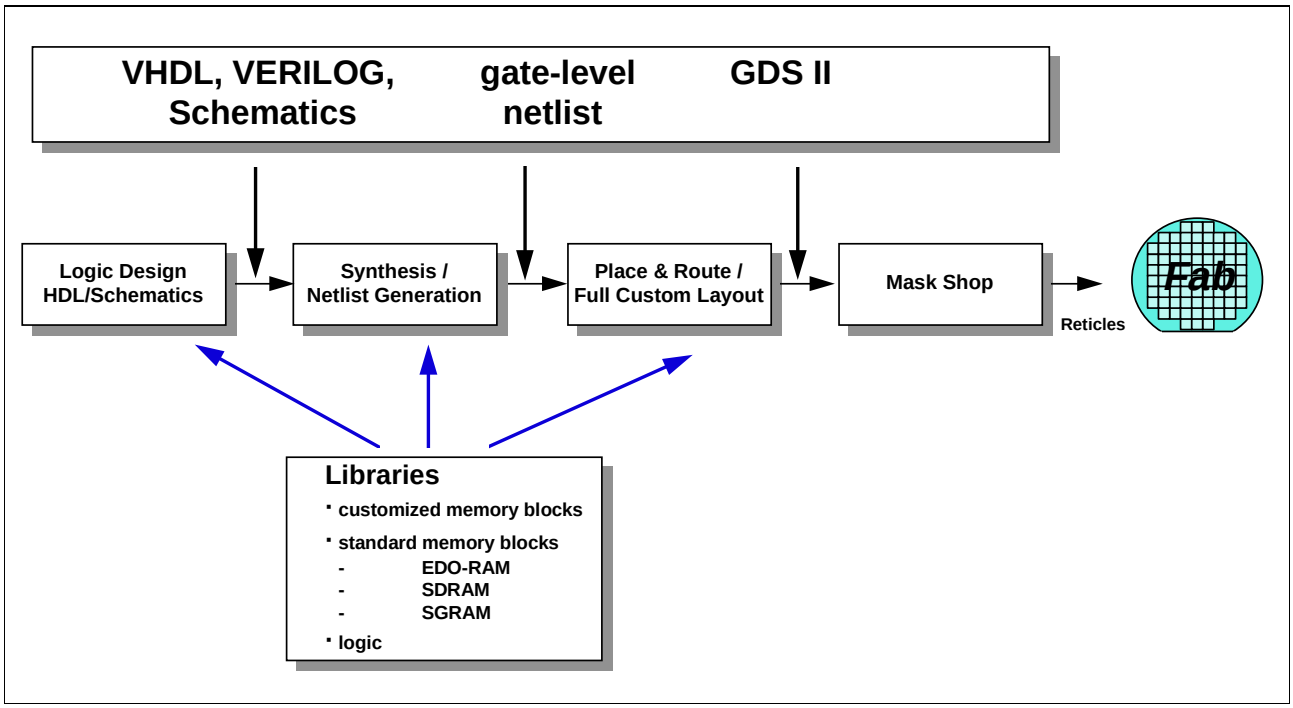

Figure 2
Design Flow

Manufacturing may include packaging, or end at wafer level. See figure 3 for an overview of the backend flow. Depending on the customer's needs, tested wafers, mounted devices or tested devices may be provided.

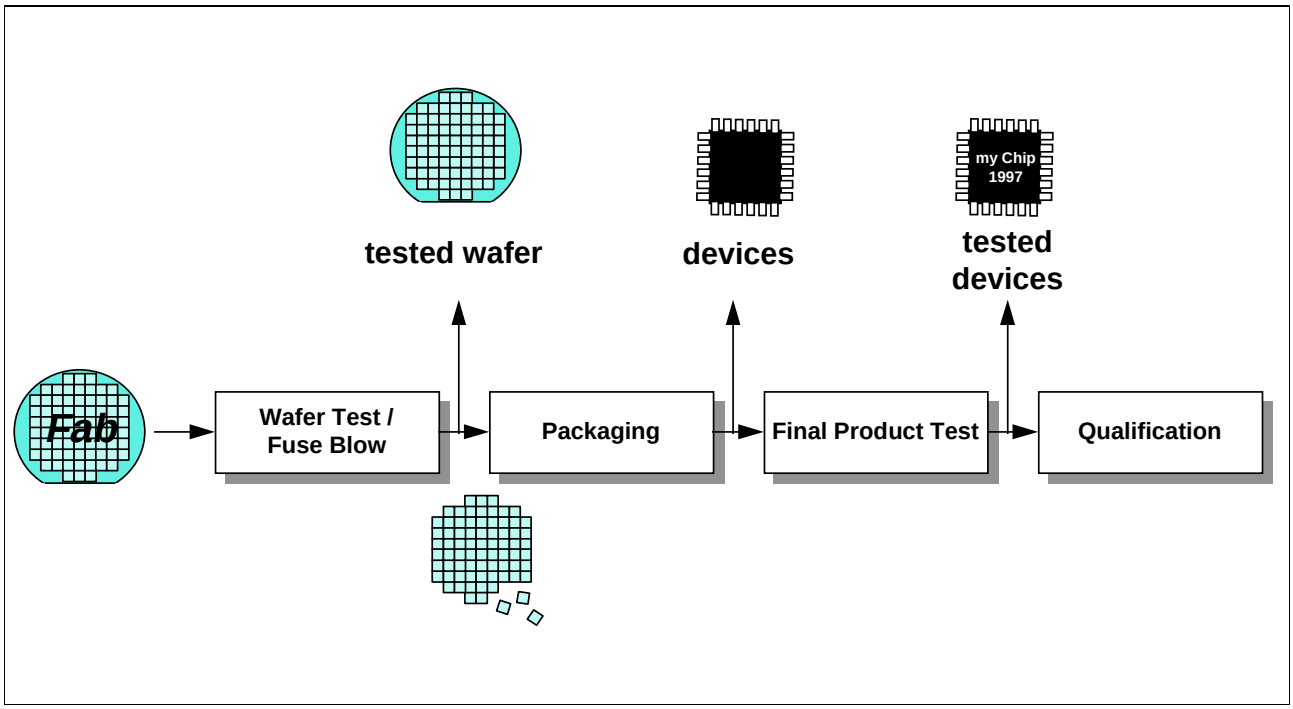

Figure 3
Backend Manufacturing

3 Technical Description

Siemens provides a library of DRAM modules for the fast creation of customized dynamic memory. One memory block contains 256 Kbit, organized in 1024 columns and 256 rows. This way 1024 sense amplifiers build one of 256 available pages. The data is accessible via a 64 bit wide bus. Adding blocks vertically, horizontally or both ways affects bus width and the amount of interface logic needed. The page length can be set separately by providing an appropriate decoder. This decoder is part of the DRAM core and is provided by Siemens to the request of the design. Thus, the architecture can be optimized for the given application.

3.1 Architecture of a Memory Module

The following definitions are used throughout this document:

Memory stripe: all memory blocks with common global bit lines together with the bus interface (see figure 4).

Memory segment: all memory stripes that share same lines of the external data bus (see figure 5).

Memory module: all memory segments sharing one control bridge.

It is possible that one stripe is a segment and that this segment is the whole module. Figures 4 to 6 show different examples for a memory module.

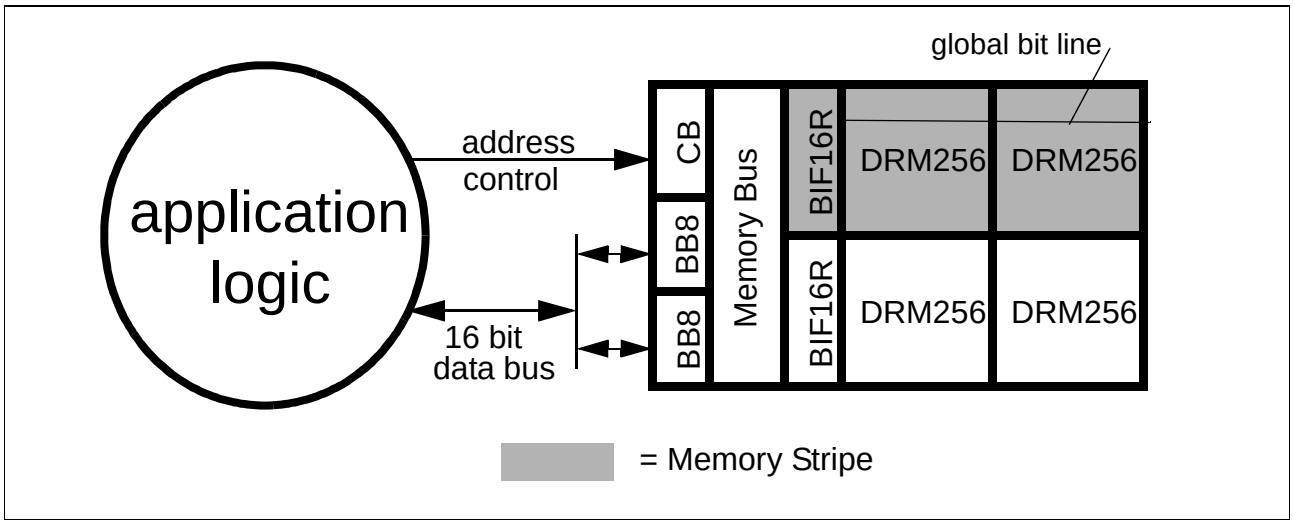

Figure 4
Memory Stripe in a Memory Module with 1 Mbit and 16 Bit Data Bus

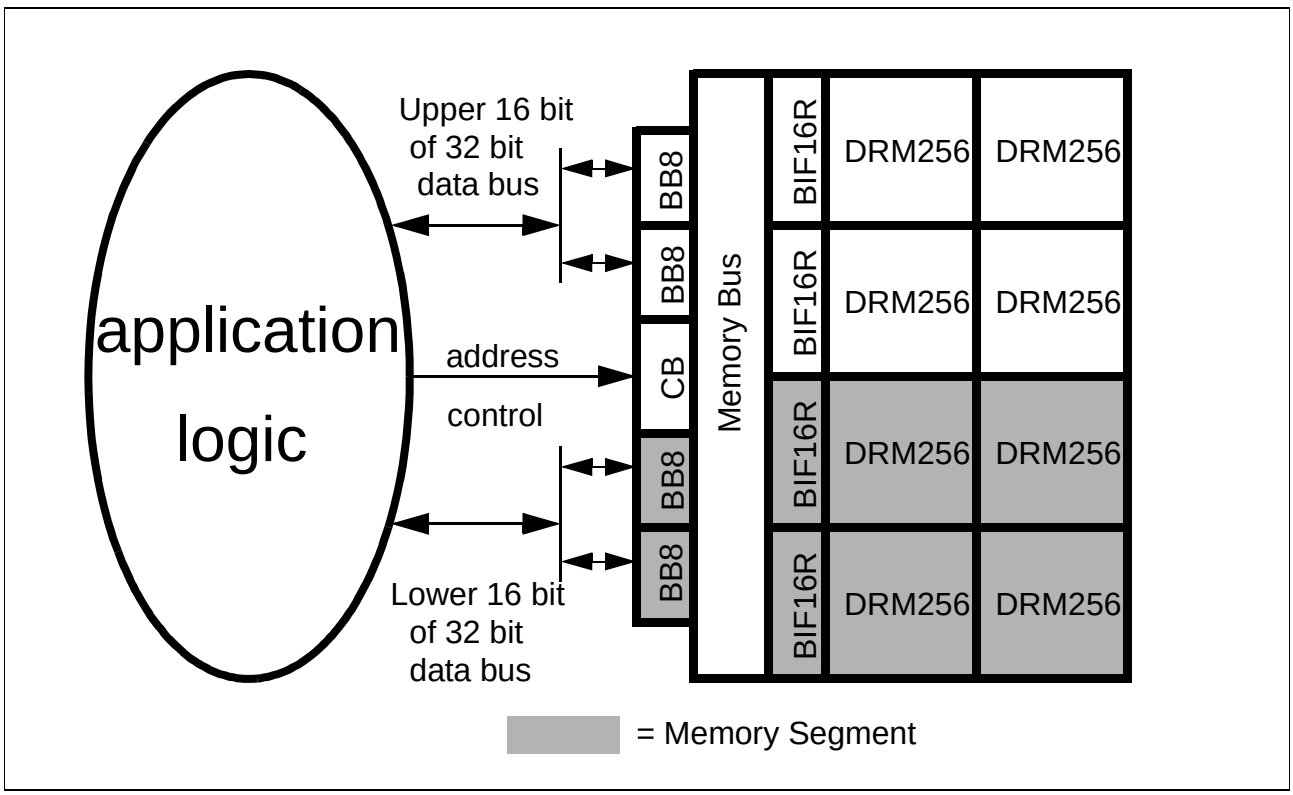

Figure 5
Example for a Memory Module with 2 Mbit and 32 Bit Data Bus

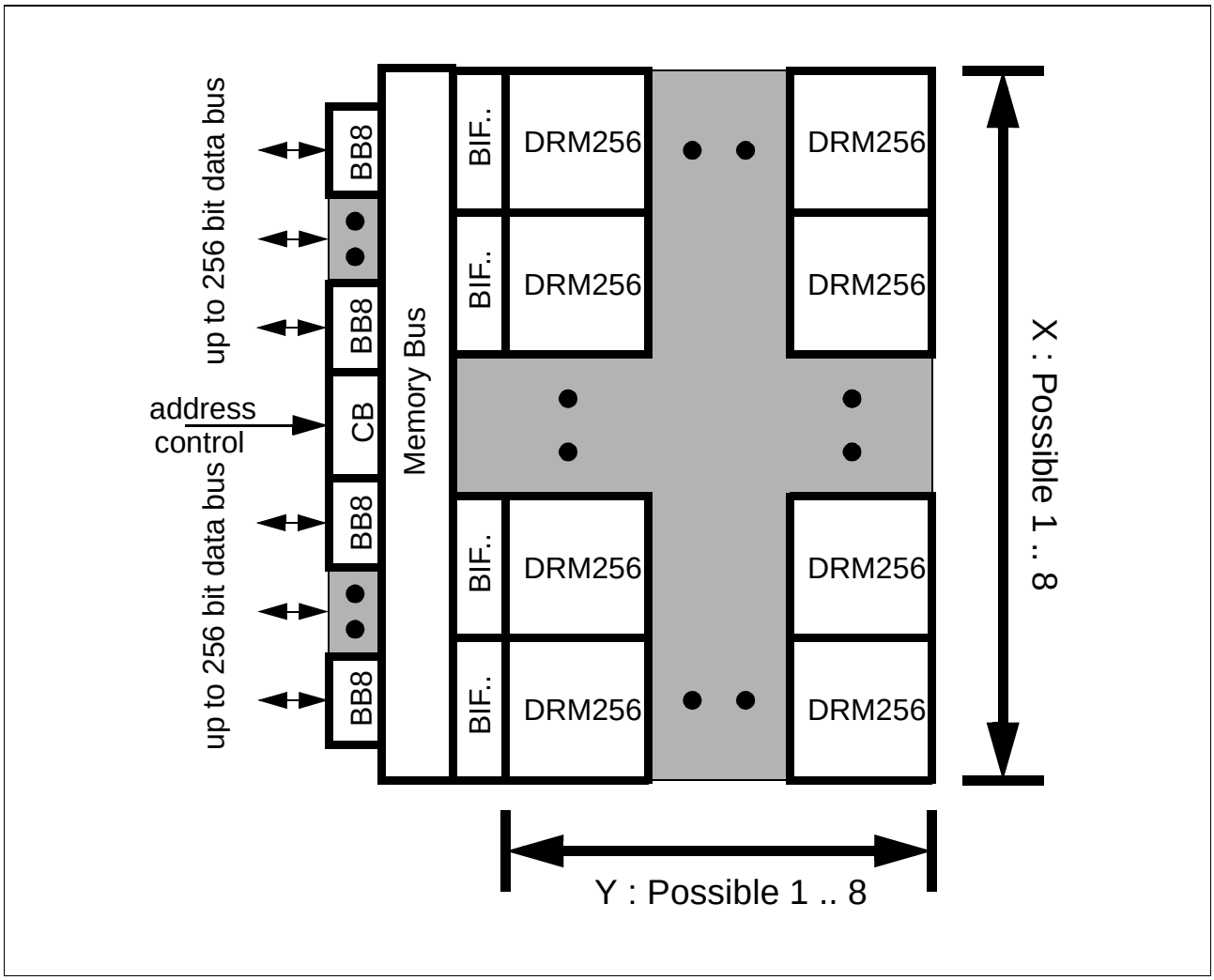

Figure 6
Maximum Configuration of a Memory Module

The number of blocks in y direction for one memory module is limited to 8. Otherwise the length of the global bit line exceeds the driver capability of the bus interface and a serious speed degradation occurs. The number of blocks in x direction is limited to 8 because of the implemented bus width for selection. This also limits the total data bus width to 8 * 64 = 512 bits. In total one memory module can have up to 64 memory blocks or 16 MBit of memory.

3.2 Multibank Option

The logical separation of the memory module is the memory bank. One, two, four or eight memory blocks form one memory bank. The advantage of this organization is the increased page length. One memory block has 1024 local sense amplifiers and therefore offers 1024 bits for „fast page mode“ style access. If *n* blocks form one bank the page length of this bank is *n* * 1024 bits. The purpose of using *multiple* banks is to parallelly keep different data segments in different banks. This allows faster page mode accesses to all data segments with hidden precharge as the probability for a pagehit is increased.

The maximum number of banks of a memory module is equal to the number of memory blocks. However, the effort to keep track of all open banks rises significantly with the number of banks. Thus,

the maximum number of banks supported by Modular embedded DRAM is 16. The maximum size of one bank is 2 MBit. This corresponds to a maximum page length of 8 Kbit.

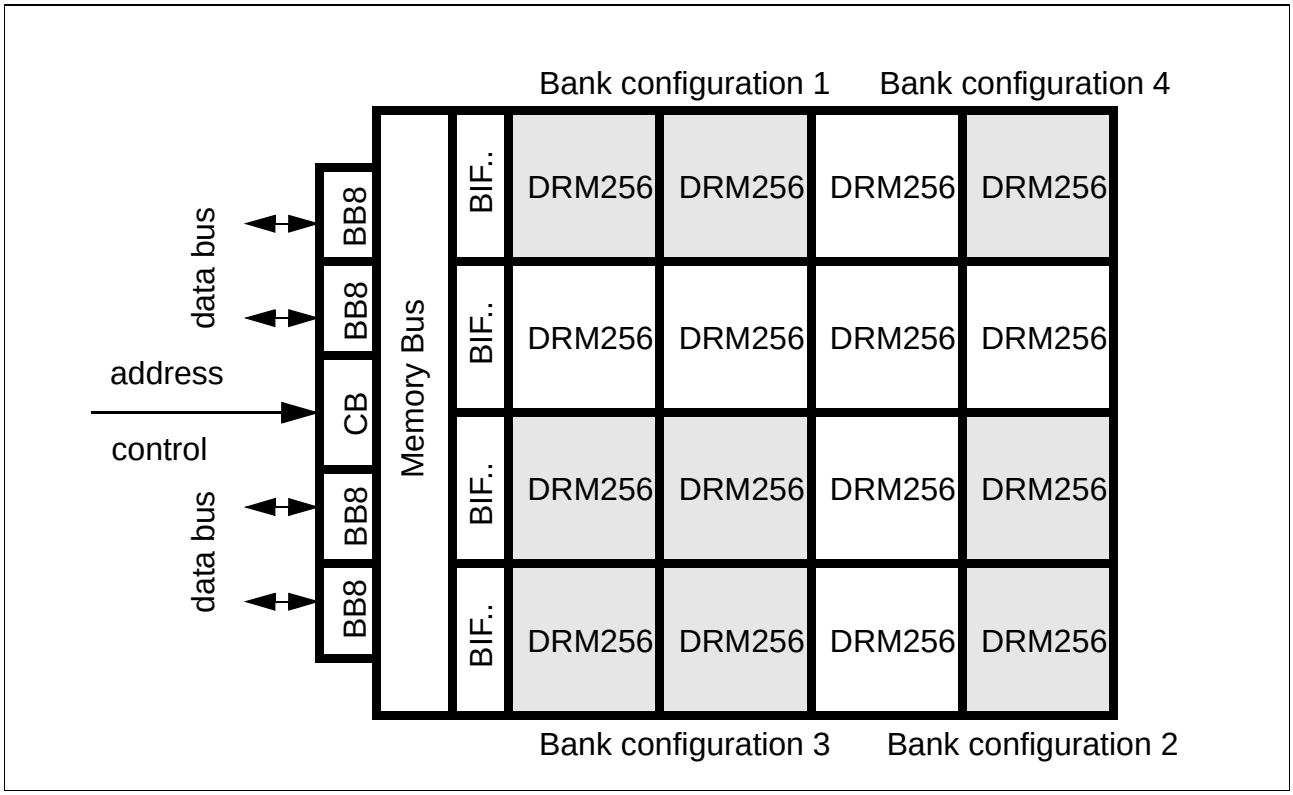

Figure 7
Possible Bank Configurations

The memory block contains a bank decoder part, which is configured by Siemens to the request of the actual design. Several different bank configurations are possible. Figure 7 shows examples, they are described below. Each configuration has its own area of application. However, a memory module may only contain identical banks, as opposed to the module sketched in figure 7.

Bank Configuration 1

One memory stripe is connected to all data bits of the data bus. This configuration provides a 2K page size with a data bus of up to 64 bits, depending on the choice of bus interface and bus bridge. It provides optimized power consumption, because only one bus interface is needed for 512 Kbit of memory.

Bank Configuration 2

Two memory blocks are connected in parallel to the memory bus. Again, there are 512 Kbit with a 2K page size, but the bus interface width is doubled as compared to configuration 1. This configuration is useful, if a wide data bus is needed and also a large number of banks is required.

Bank Configuration 3

Four memory blocks are combined to one bank with a bus interface of 128 bit. This configuration gives a pagelength of 4096 bit together with a wide data bus.

Bank Configuration 4

A single memory block could also be a memory bank. This allows a large number of memory banks per memory module. As the number of sense amplifiers to be charged at a time is minimized, minimum power consumption results. Note that the maximum supported number of banks is 16.

3.3 VHDL Model

Modular embedded DRAM comes with a VHDL model for early simulation. The VHDL model is foreseen for the logic- and gate-level simulation with leapfrog. Upcoming additional packages will provide all timing values for the gate level simulation for the three modes “slow” (worst), “typical” and “fast” (best).

3.4 Specification of a Memory Module

This section summarizes the parameters that are necessary to fully specify an embedded DRAM module.The following table gives parameter, possible range and a short description.

Table 7
Memory Module Specification

Parameter	Range	Description
memory size	256Kbit .. 16 Mbit	These two parameters are redundant as one block has 256 Kbit = 262 144 Bit
no. of 256 Kbit blocks	1 .. 64	
no. of blocks in x - direction	1 .. 8	increases possible bus width (refer to figure 6 on page 14)
no. of blocks in y - direction	1 .. 8	increases length of bit lines (see section 3) with constant interface width
Width of the data bus	8 .. 512 bit	
size of one bank in x- direction		all banks have to be equal; no. of blocks per bank must be 1, 2, 4, or 8
size of one bank in y- direction		

4 Operation of the Memory Module

Operation of the memory module is controlled via the command bus, the latency setting, the bank address, column address and row address. Data is read and written via the data bus.

4.1 Data Bus

The width of the data bus depends on the actual implementation. It may be configured in a range from 8 bit to 512 bit. DI[] and DO[] can be tied together in order to get a bidirectional bus. In that case the /OE signal must be used for arbitration. The layout of the memory module is prepared for such applications, i.e. the DI[] and DO[] signals are paired for each bit.

4.2 Command Bus

The command bus CMD[3..0] is divided in two parts in order to allow operations in different banks with „hidden precharge“. Tables 8 and 9 give the possible row and column commands as controlled by CMD[3:0].

Table 8
ROW Commands

CMD3	CMD2	State	Description
1	1	NOP	No operation
1	0	-	Reserved for future use
0	1	ACTIVATE	One row of a bank is opened for access
0	0	PRECHARGE	The open row is copied back to the memory

Table 9
COLUMN Commands

CMD1	CMD0	State	Description
1	1	NOP	No operation
1	0	-	Reserved for future use
0	1	READ	Read data from the open row
0	0	WRITE	Write data to the open row

The command bus allows two operations in parallel. ACTIVATE/PRECHARGE of one bank can be combined with READ/WRITE of another bank. This way, multibank operation is provided giving accelerated data transmission with hidden precharge.

4.3 Address Bus

The address bus is divided into four parts: column address ACOL, row address AROW, and bank addresses BCOL and BROW.

As one block has 256 rows, the AROW bus is always 8 bit wide. The width of the ACOL bus depends on the number of columns in one bank, the page length. It is 10 bit for a 1024 bit page, 11 bit for a 2K-page etc.

BCOL and BROW have the same width, given by $\log_2$ of the number of implemented banks. Note that two banks require a single signal to select the banks. However, if only one bank is implemented, the signals BCOL and BROW still exist. They then have to be tied to GND for proper operation.

4.4 Latency Modes

A programmable pipe line of three registers in the interface logic allows to trade clock frequency for latency during operation. The clock frequency for LATENCY 3 is higher than for LATENCY 1. „LATENCY 1“ means that the data is available on DO[] one clock cycle after a given command. „LATENCY 2“ means the data is available two clock periods after the command, etc.

4.5 Byte Write Enable

Setting a bit on BWE to „1“enables writing of the corresponding byte only instead of the complete data word. This allows to write bytes of 8 bits each separately on a given location into an addressed word. The following figure gives an example for a memory module with a 32 bit interface using the byte write capability. As the 32 bit word contains four 8-bit bytes, BWE is a 4-bit wide bus selecting the corresponding bytes of the data word. If all four bits of BWE are set to „1“during a WRITE; all 32 data bits are written into the memory block. Setting only the LSB of BWE to „1“only writes the data on DI[7..0] into the memory block without affecting the other bits.

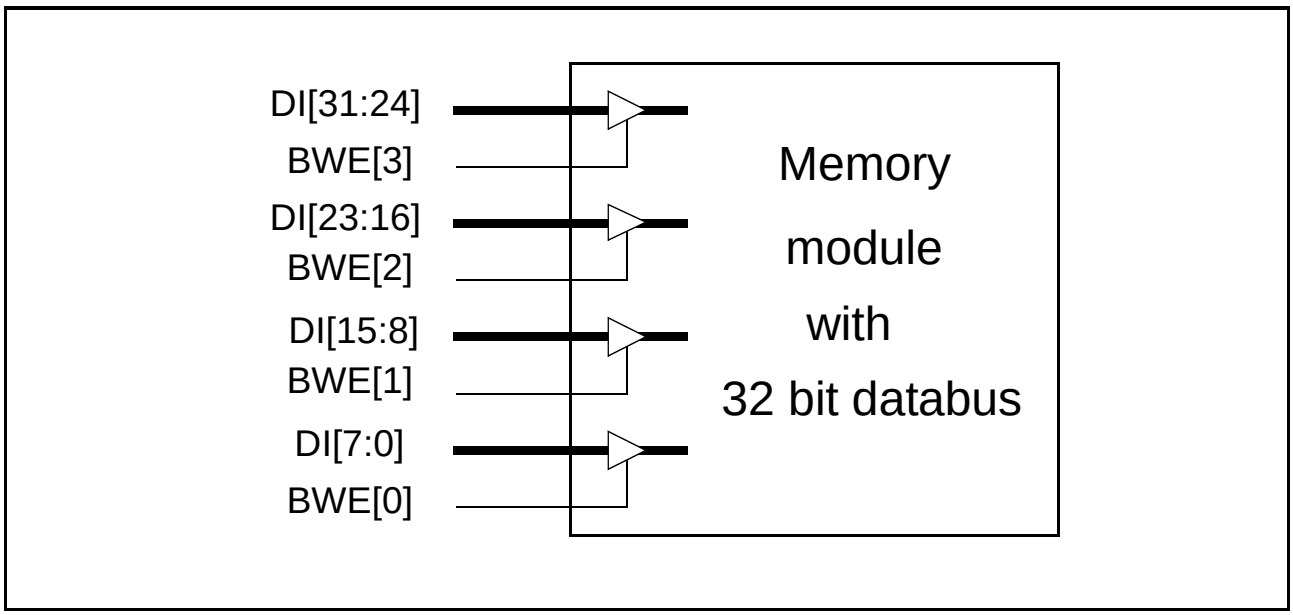

Figure 8
Use of the BYTE WRITE ENABLE Signal

5 Test Controller

Embedded DRAM requires a dedicated solution for testing, derived from common DRAM test methods and taking into account that it is combined with logic like CPU cores, SRAM, ROM, etc. The test controller supportethree ways to access and communicate with the embedded DRAM core:

- pure direct access, allocating an external pin for every pin of the DRAM core
- direct access but with the help of multiplexer logic and registers to reduce the number of pins which must be accessed simultaneously
- built-in logic to partially support algorithmic pattern generation and expected-value comparison.

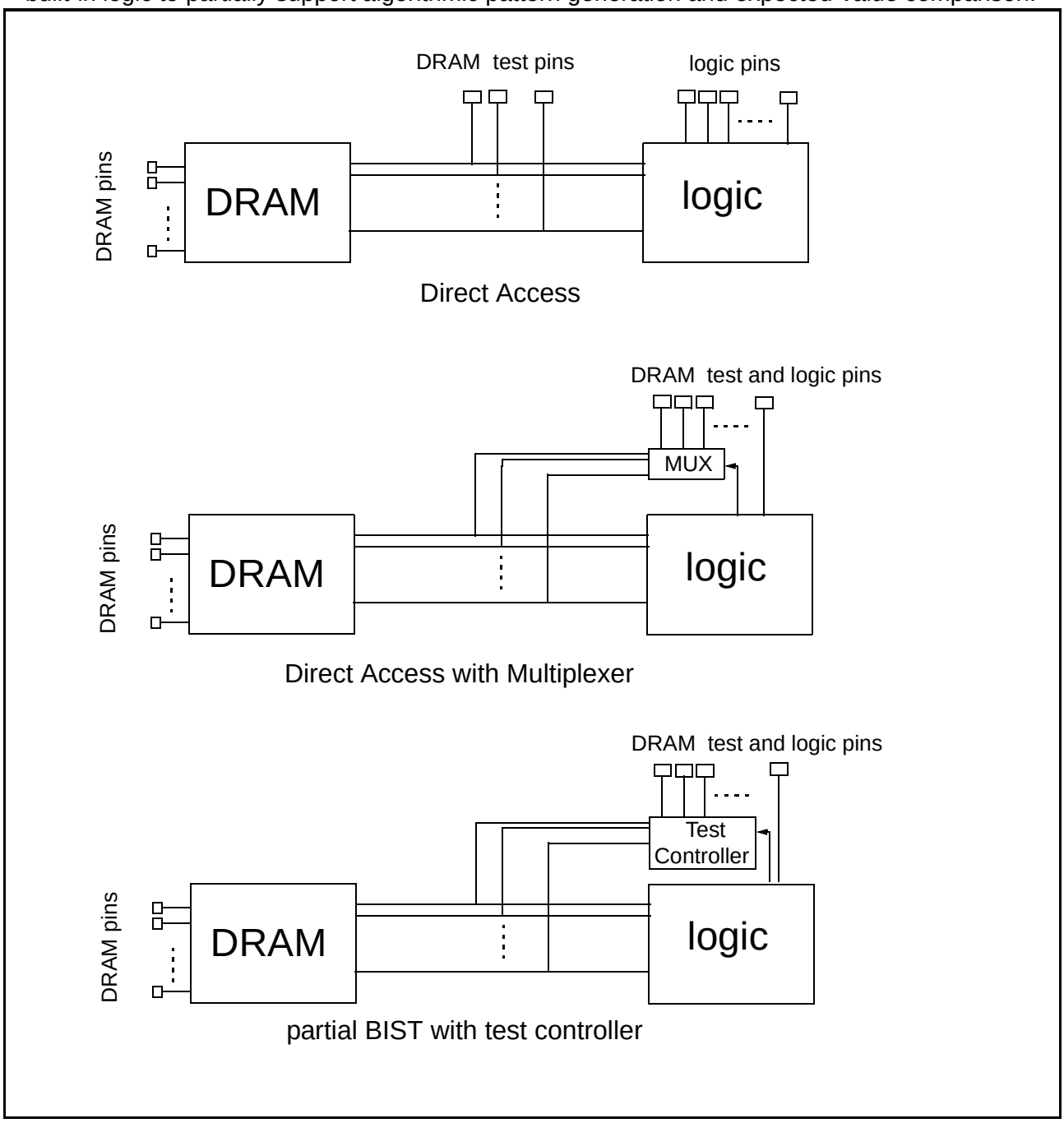

Figure 9
DRAM Test Methods

See figure 9 for an illustration of different test methods. Direct access requires additional pins or multiplexer logic and registers. It allows the use of standard memory test software. Thus, existing memory test software may be used for wafer test and fusing. However, a tester with memory test option “MTO” capability is required.

On-chip Algorithmic Pattern Generation logic allows to use any standard tester. For package test, where no wafer fail map is generated, internally generated patterns can be applied and the results analyzed as pass/fail. Such a test can be performed by any standard logic tester.

The embedded DRAM test concept is based on an on-chip test controller. It provides the necessary multiplexers to allow direct access as well as optional additional logic to partially support algorithmic pattern generation and expected-value comparison. This provides the following advantages:

- efficient production test to standard DRAM quality,
- information recovery for repair & yield statistics,
- transparent access for fault analysis

The test concept is derived from Siemens’ 16 Mbit technology and offers a quality level comparable to that achieved for standard DRAM components in this technology. All of the tests used for 16 Mbit EDO and SDRAM are available.

The test controller comes in the form of a synthesizeable VHDL description which is configured for the particular design. This VHDL code is integrated in the customer VHDL code. The test controller has a 16-bit control/address interface and a n 8-bit, 16-bit or 32-bit data interface as options. The width of the data bus can be selected depending on the application.

It provides two operating modes, *direct access* and *pattern generation (partial BIST)*. The *direct access* mode reduces the number of external pins needed for direct DRAM access. It corresponds to the middle diagram in figure 9.

6 Operating Conditions

Table 10
Operating Conditions

Symbol	Parameter	min	max	Unit
V_{DD}	Supply voltage	3.0	4.6	V
T_{OP}	Operating temperature	-25 [1)]	70	°C

1) -25 °C is the technological limit. For consumer applications it is recommended to use a higher limit of 0 °C.

6.1 DC Parameters

Table 11
Electrical Parameters

Symbol	Parameter	min	max	Unit
I_{DD}	Supply current		t.b.d.	mA
C_I	Input capacitance of CLK, TCLK		200	fF
C_I	Input capacitance of all other inputs		15	fF
C_O	Output capacitance of DO, TDO		t.b.d.	fF

6.2 AC Parameters

The following table contains all timing parameters of the timing diagrams in the next chapters. The given values are pre-silicon and based on simulations with a high production yield as main design target.

Table 12
Timing Parameters

Symbol	Parameter	min	max	Unit	Notes
t_{CLL}	Clock low time	4		ns	
t_{CLH}	Clock high time	4		ns	
t_{CLR}	Clock rise time		1	ns	
t_{CLF}	Clock fall time		1	ns	
t_{SU}	Setup time	2		ns	
t_{HO}	Hold time	0		ns	

Symbol	Parameter	min	max	Unit	Notes
t_{SUL}	Setup time for LATENCY	2		clocks	
t_{HOL}	Hold time for LATENCY	2		clocks	
t_{ZHL}	Delay time, buffer tri-state to buffer active		3	ns	
t_{HLZ}	Delay time, buffer active to buffer tri-state		3	ns	
t_{RLO}	Reset low time with inactive memory	200		ns	
t_{RVV}	Delay time from RESET inactive to first ACTIVATE	200		ns	
t_{APD}	Delay time between ACTIVATE and PRECHARGE	30		ns	
$t_{PAD\ (1)}$	Delay time between PRECHARGE and ACTIVATE of same row	30	see t_{PAD} (2)	ns	1)
$t_{PAD\ (2)}$	Refresh period for one memory row	see t_{PAD} (1)	64	ms	2)
t_{ACD}	Delay time between ACTIVATE and COLUMN operation to the same bank	25		ns	
t_{CL1}	Clock period for LATENCY 1	19+n		ns	3)
t_{AA1}	Address access time for LATENCY 1	44+n		ns	3)
t_{CO1}	Clock to valid output delay at LATENCY 1		19+n	ns	3), 4)
t_{DH1}	Clock to output hold at LATENCY 1	2		ns	
t_{MO1}	Modify time: t_{CL1} - t_{CO1} - t_{SU}				
t_{CL2}	Clock period for LATENCY 2	15+n		ns	3)
t_{AA2}	Address access time for LATENCY 2	42+n		ns	3)
t_{CO2}	Clock to valid output delay for LATENCY 2 and LATENCY 3		4	ns	4)
t_{DH2}	Clock to output hold at LATENCY 2	2		ns	
t_{MO2}	Modify time: t_{CL2} - t_{CO2} - t_{SU}				
t_{CL3}	Clock period for LATENCY 3	12+n		ns	3)
t_{AA3}	Address access time for LATENCY 3	42+n		ns	3)

Symbol	Parameter	min	max	Unit	Notes
t_{CP3}	Delay between COLUMN operation and PRECHARGE to the same bank, LATENCY 3	2 * t_{CL3}			5)
t_{MO3}	Modify time: t_{CL3} - t_{CO2} - t_{SU}				

1) The same parameter is relevant for the refresh period.

2) During the refresh period all 256 rows of one memory block must be activated and precharged.

3) If the number of memory blocks in a memory stripe is less or equal than 4 then n = 0. For all other values *n = (number of blocks in stripe) - 4*.

4) Output load 1 pF

5) Due to LATENCY 3 a rising clock edge is required during t_{CP3}.

7 Maximum Ratings

Stresses above those listed in the table below may cause permanent damage to the device. Exposure to conditions beyond those indicated below may affect device reliability.

This is a stress rating only and functional operation of the device under these conditions or at any other condition beyond those indicated in the operational conditions of this specification is not implied. It is not implied, that more than one of these conditions can be applied simultaneously.

Table 13
Maximum Ratings

Parameter	Limit Values		Unit
	min.	max.	
positive Supply Voltage	3.0	4.6	V
Voltage applied at any input	tbd	tbd	V

8 Environmental Requirements

8.1 Storage and Transportation

The rated (limited capability) storage and transportation temperature range prior to printed board assembly shall be - 50 to +150°C (without supply voltage)

8.2 Operating Ambient

The operating ambient temperature shall be within 0 °C to +70 °C