

SANYO**DRE3**

Silicon Diffused Junction Type

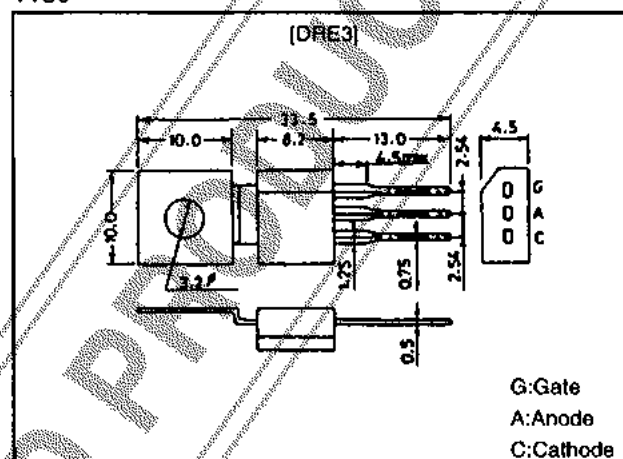
3.0A Reverse Blocking Thyristor**Features**

- Glass passivation for high reliability.
- Peak OFF-state (reverse) voltage : 100 to 600V.
- Average ON-state current : 3A.
- TO-202 package.

Package Dimensions

unit:mm

1150

**Specifications****Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$**

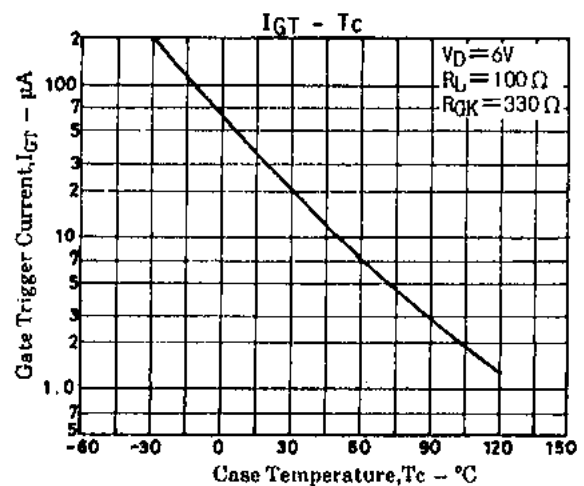
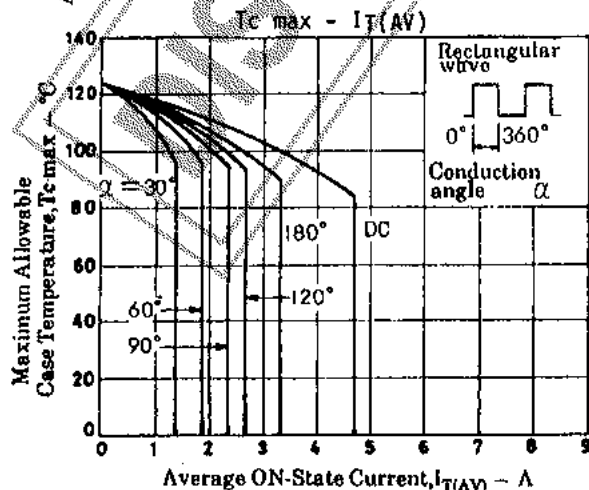
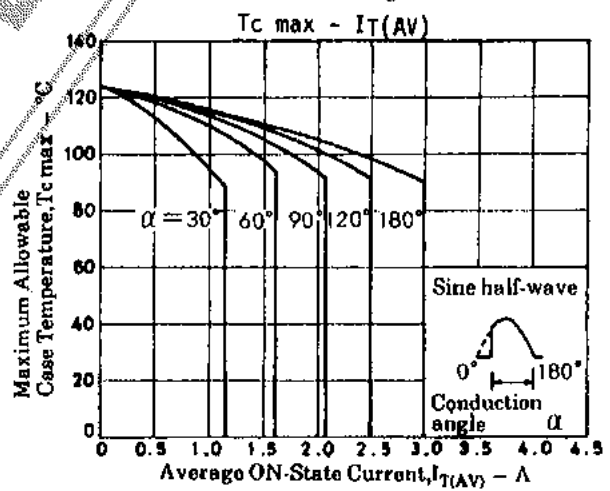
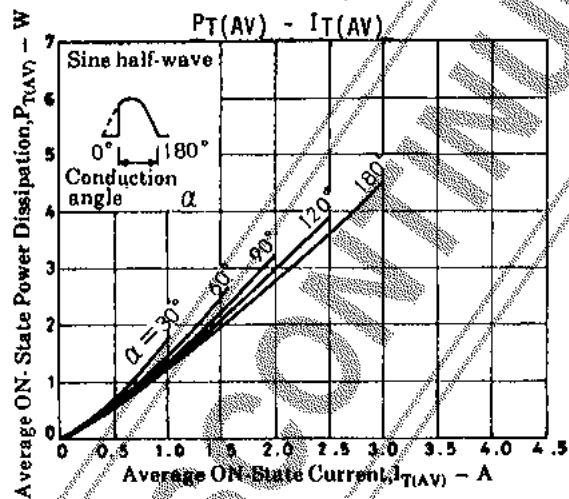
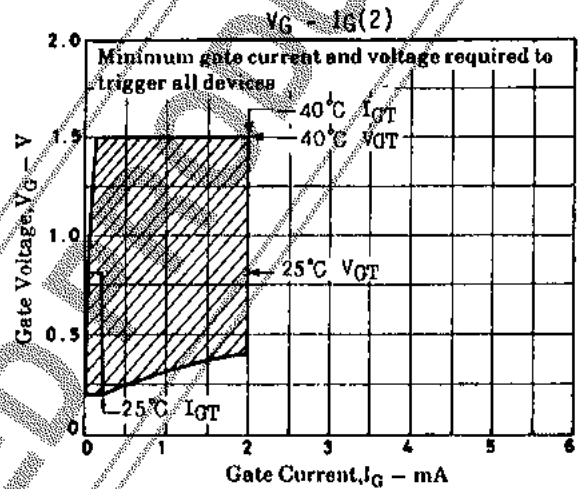
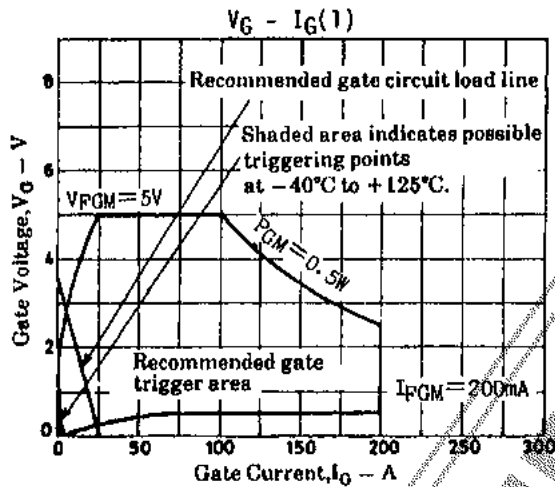
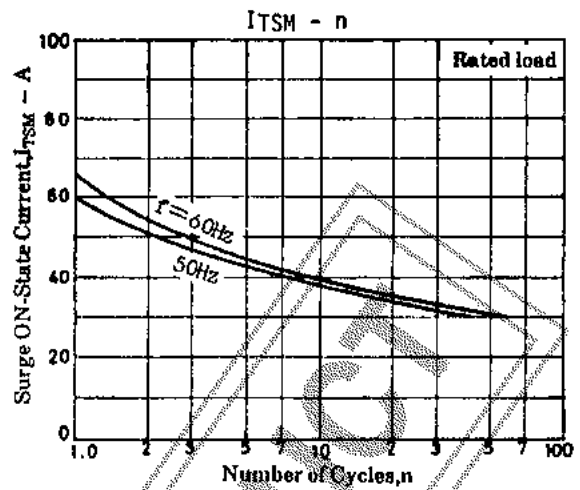
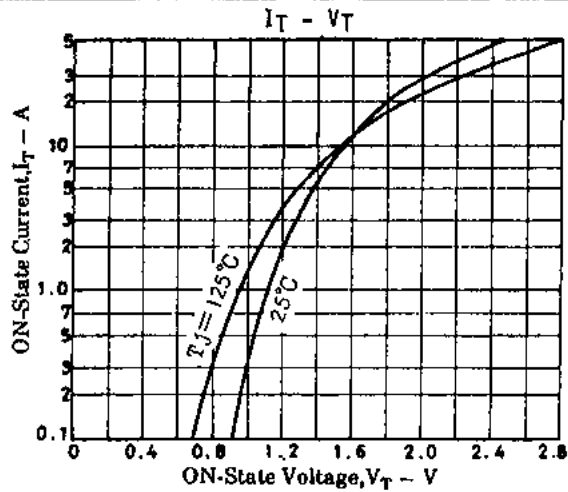
Parameter	Symbol	Conditions	DRE3B	DRE3C	DRE3E	DRE3G	Unit
Repetitive Peak OFF-State Voltage	V_{DRM}	$R_{GK}=330\Omega$	100	200	400	600	V
Non-Repetitive Peak Reverse Voltage	V_{RRM}	$R_{GK}=330\Omega$	150	300	500	720	V
Repetitive Peak Reverse Voltage	V_{RRM}	$R_{GK}=330\Omega$	100	200	400	600	V
Average ON-State Current	$I_T(AV)$	$T_a=90^\circ\text{C}$, single phase half-wave	→	→	→	3	A
RMS ON-State Current	$I_T(RMS)$		→	→	→	4.7	A
Surge ON-State Current	I_{TSM}	Sine half-wave, 1 cycle, 50Hz	→	→	→	60	A
Ampere Squared-Seconds	I^2t	$t_{rms} \leq 10\text{ms}$	→	→	→	20	A ² S
Peak Gate Power Dissipation	P_{GM}	$f \geq 50\text{Hz}$, $duty \leq 10\%$	→	→	→	0.5	W
Average Gate Power Dissipation	$P_{G(AV)}$		→	→	→	0.05	W
Peak Gate Forward Current	I_{FGM}	$f \geq 50\text{Hz}$, $duty \leq 10\%$	→	→	→	0.2	A
Peak Gate Reverse Voltage	V_{RGM}		→	→	→	5	V
Junction Temperature	T_J		→	→	→	125	$^\circ\text{C}$
Storage Temperature	T_{stg}		→	→	→	-40 to +125	$^\circ\text{C}$
Weight			→	→	→	1.5	g

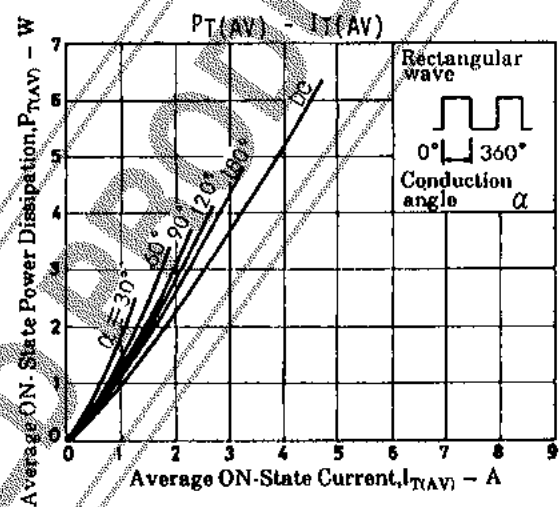
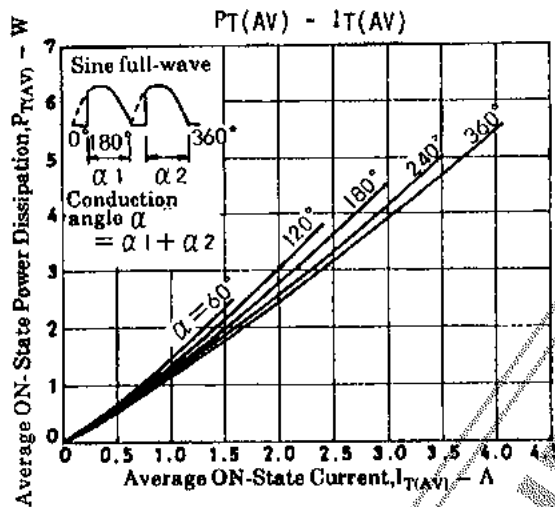
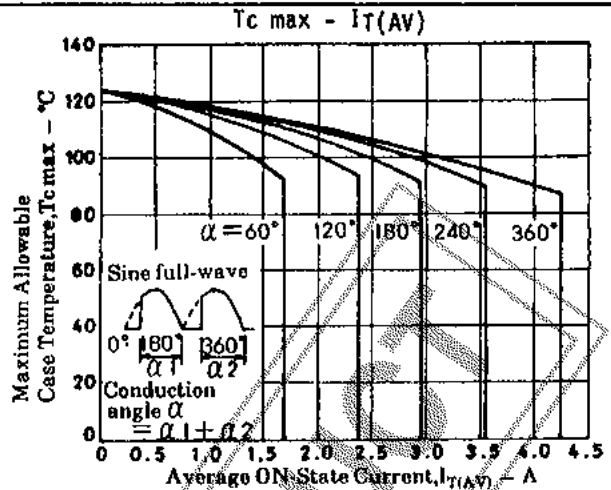
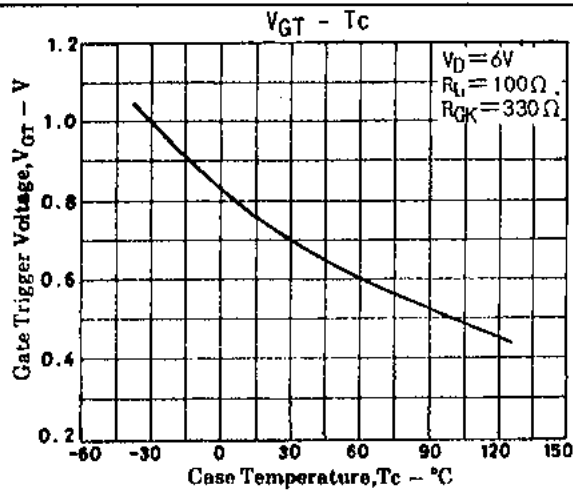
Electrical Characteristics at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Repetitive Peak OFF-State Current	I_{DRM}	$T_J=125^\circ\text{C}$, $V_D=V_{DRM}$, $R_{GK}=330\Omega$			2	mA
Repetitive Peak Reverse Current	I_{RRM}	$T_J=125^\circ\text{C}$, $V_D=V_{RRM}$, $R_{GK}=330\Omega$			2	mA
Peak ON-State Voltage	V_{TM}	$I_{TM}=12\text{A}$			1.6	V
Critical Rate of Rise of OFF-State Voltage	dv/dt	$T_J=75^\circ\text{C}$, $V_D=2/3V_{DRM}$, $R_{GK}=330\Omega$		50		V/ μs
Holding Current	I_H	$R_L=100\Omega$, $R_{GK}=330\Omega$		1		mA
Gate Trigger Current	I_{GT}	$V_D=6\text{V}$, $R_L=100\Omega$, $R_{GK}=330\Omega$			200	μA
Gate Trigger Voltage	V_{GT}	$V_D=6\text{V}$, $R_L=100\Omega$, $R_{GK}=330\Omega$			0.8	V
Gate Nontrigger Voltage	V_{GD}	$T_a=125^\circ\text{C}$, $V_D=2/3V_{DRM}$, $R_{GK}=330\Omega$	0.2			V
Thermal Resistance	$R_{th}(j-c)$				6.0	$^\circ\text{C/W}$

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