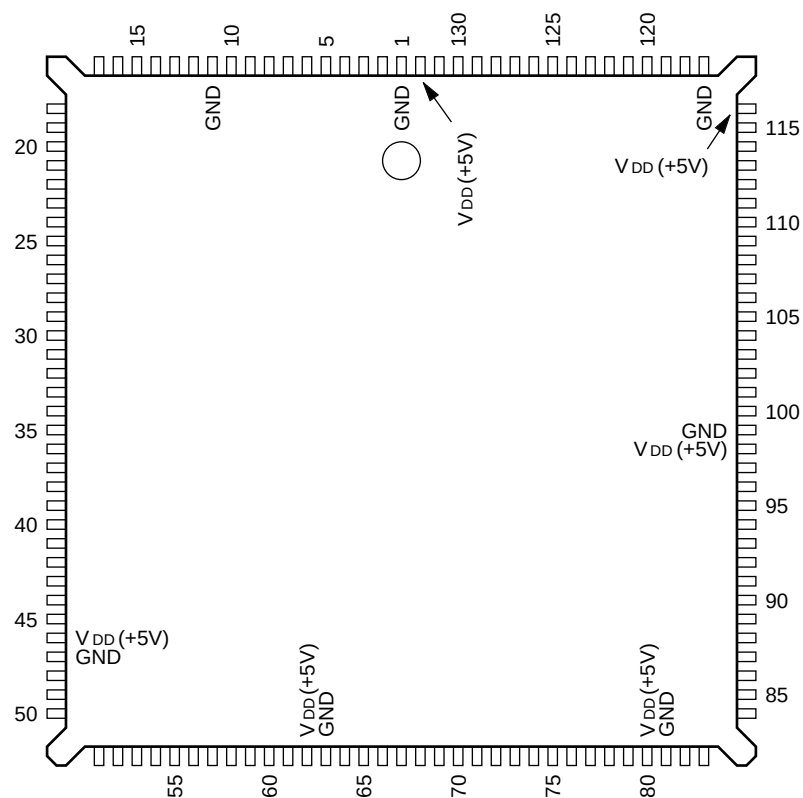

C-MOS SYSTEMS-ORIENTED NETWORK INTERFACE CONTROLLER (SONIC) - TOP VIEW -



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	–	GND	34	I	B $\overline{\text{SCK}}$	67	O	A21	100	I/O	D23
2	–	ANGND	35	I	B $\overline{\text{MODE}}$	68	O	A20	101	I/O	D22
3	I/O	X1	36	I	M $\overline{\text{REO}}$	69	O	A19	102	I/O	D21
4	I	X2	37	I	C $\overline{\text{S}}$	70	O	A18	103	I/O	D20
5	I	EXT	38	I	S $\overline{\text{AS}}$	71	O	A17	104	I/O	D19
6	I	P $\overline{\text{REJ}}$	39	I	S $\overline{\text{DS}}$	72	O	A16	105	I/O	D18
7	I,O	COLI/COLO	40	O	S $\overline{\text{MACK}}$	73	O	A15	106	I/O	D17
8	I,O	R $\overline{\text{XD}}$ /R $\overline{\text{XD}}$ O	41	I/O	D $\overline{\text{SACK1}}$ /R $\overline{\text{DY}}$ O	74	O	A14	107	I/O	D16
9	I,O	R $\overline{\text{XC}}$ /R $\overline{\text{XC}}$ O	42	I/O	D $\overline{\text{SACK0}}$ /R $\overline{\text{DY}}$ I	75	O	A13	108	I/O	D15
10	I,O	C $\overline{\text{RS}}$ /C $\overline{\text{RS}}$ O	43	O	B $\overline{\text{GACK}}$	76	O	A12	109	I/O	D14
11	–	GND	44	O	B $\overline{\text{R}}$ /HOLD	77	O	A11	110	I/O	D13
12	I,O	T $\overline{\text{XC}}$ /T $\overline{\text{XC}}$ O/S $\overline{\text{TERM}}$	45	O	I $\overline{\text{NT}}$ /I $\overline{\text{NT}}$	78	O	A10	111	I/O	D12
13	O	LBK	46	–	V $\overline{\text{DD}}$	79	O	A9	112	I/O	D11
14	O	TXD	47	–	GND	80	–	V $\overline{\text{DD}}$	113	I/O	D10
15	O	TXE	48	O	S2	81	–	GND	114	I/O	D9
16	O	TX–	49	O	S1	82	O	A8	115	I/O	D8
17	O	TX+	50	O	S0	83	O	A7	116	–	V $\overline{\text{DD}}$
18	–	TXGND	51	O	M $\overline{\text{RW}}$ /M $\overline{\text{WR}}$	84	O	A6	117	–	GND
19	–	TXV $\overline{\text{DD}}$	52	O	D $\overline{\text{S}}$	85	O	A5	118	I/O	D7
20	–	PLL V $\overline{\text{DD}}$	53	O	E $\overline{\text{CS}}$	86	O	A4	119	I/O	D6
21	–	R $\overline{\text{XV}}$ V $\overline{\text{DD}}$	54	O	A $\overline{\text{S}}$ /A $\overline{\text{DS}}$	87	O	A3	120	I/O	D5
22	I	R $\overline{\text{X}}$ –	55	O	A31	88	O	A2	121	I/O	D4
23	I	R $\overline{\text{X}}$ +	56	O	A30	89	O	A1	122	I/O	D3
24	I	CD–	57	O	A29	90	I/O	D31	123	I/O	D2
25	I	CD+	58	O	A28	91	I/O	D30	124	I/O	D1
26	O	P $\overline{\text{COMP}}$	59	O	A27	92	I/O	D29	125	I/O	D0
27	I	SEL	60	O	A26	93	I/O	D28	126	I	RA5
28	I	B $\overline{\text{RT}}$	61	O	A25	94	I/O	D27	127	I	RA4
29	I	R $\overline{\text{ESET}}$	62	–	V $\overline{\text{DD}}$	95	I/O	D26	128	I	RA3
30	I	S $\overline{\text{RW}}$ /S $\overline{\text{WR}}$	63	–	GND	96	I/O	D25	129	I	RA2
31	I/O	USR1	64	O	A24	97	I/O	D24	130	I	RA1
32	I/O	USR0	65	O	A23	98	–	V $\overline{\text{DD}}$	131	I	RA0
33	I	H $\overline{\text{LDA}}$ /B $\overline{\text{G}}$	66	O	A22	99	–	GND	132	–	V $\overline{\text{DD}}$

3	X1	LBK	13	INPUT	
4	X2	TXD	14	BG	; BUS GRANT (BMODE=1)
5	EXT	TXE	15	BMODE	; BUS MODE
6	PREJ	TX-	16	BRT	; BUS RETRY
22	RX-	TX+	17	BSCK	; BUS CLOCK
23	RX+	PCOMP	26	CD (+, -)	; COLLISION (+, -) (EXT=1)
24	CD-	SMACK	40	COLI	; COLLISION DETECT INPUT (EXT=1)
25	CD+	BGACK	43	CRSI	; CARRLER SENSE INPUT (EXT=1)
27	SEL	BR/HOLD	44	CS	; CHIP SELECT
28	BRT	INT/INT	45	EXT	; EXTERNAL ENDEC SELECT
29	RESET			HLDA	; HOLD ACKNOWLEDGE (BMODE=0)
30	SRW/SWR	S2	48	MRE0	; MEMORY REPUEST
		S1	49	PREJ	; PACKET REJECT
31	USR1	S0	50	RA0-RA5	; REGISTER ADDRESS BUS
32	USR0			RDYI	; READY INPUT (BMODE=0)
		MRW/MWR	51	RESET	; RESET
33	HLDA/BG	DS	52	RXCI	; RECEIVE CLOCK INPUT (EXT=1)
34	BSCK	ECS	53	RXDI	; RECEIVE DATA INPUT (EXT=1)
35	BMODE	AS/ADS	54	RX (+, -)	; RECEIVE (+, -) (EXT=1)
36	MRE0			SAS	; SLAVE ADDRESS STROBE
37	CS	A31	55	SDS	; SLAVE DATA STROBE
38	SAS	A30	56	SEL	; MODE SELECT (EXT=0)
39	SDS	A29	57	SRW	; SLAVE READ/WRITE STROBE (BMODE=1)
		A28	58	STERM	; SYNCHRONOUS TERMINATION (BMODE=1)
41	DSACK1/RDYO	A27	59	SWR	; SLAVE READ/WRITE STROBE (BMODE=0)
42	DSACK0/RDYI	A26	60	TXCI	; TRANSMIT CLOCK INPUT (EXT=1)
		A25	61	X2	; CRYSTAL FEEDBACK INPUT
90	D31	A24	64	OUTPUT	
91	D30	A23	65	A1-A31	; ADDRESS BUS
92	D29	A22	66	ADS	; ADDRESS STROBE (BMODE=0)
93	D28	A21	67	AS	; ADDRESS STROBE (BMODE=1)
94	D27	A20	68	BGACK	; BUS GRANT ACKNOWLEDGE (BMODE=1)
95	D26	A19	69	BR	; BUS REQUEST (BMODE=1)
96	D25	A18	70	COLO	; COLLISION OUTPUT (EXT=0)
97	D24	A17	71	CRSO	; CARRIER SENSE OUTPUT (EXT=1)
100	D23	A16	72	DS	; DATA STROBE
101	D22	A15	73	ECS	; EARLY CYCLE START
102	D21	A14	74	HOLD	; HOLD REQUEST (BMODE=0)
103	D20	A13	75	INT	; INTERRUPT (BMODE=0)
104	D19	A12	76	INT	; INTERRUPT (BMODE=1)
105	D18	A11	77	LBK	; LOOPBACK
106	D17	A10	78	MRW	; MEMORY READ / WRITE STROBE (BMODE=1)
107	D16	A9	79	MWR	; MEMORY READ / WRITE STROBE (BMODE=0)
108	D15	A8	82	PCOMP	; PACKET COMPRESSION
109	D14	A7	83	RDYO	; READY OUTPUT (BMODE=0)
110	D13	A6	84	RXDO	; RECEIVE DATA OUTPUT (EXT=0)
111	D12	A5	85	RXCO	; RECEIVE CLOCK OUTPUT (EXT=0)
112	D11	A4	86	S0-S2	; BUS STATUS
113	D10	A3	87	SMACK	; SLAVE AND MEMORY ACKNOWLEDGE
114	D9	A2	88	TXCO	; TRANSMIT CLOCK OUTPUT (EXT=0)
115	D8	A1	89	TXD	; TRANSMIT DATA
118	D7			TXE	; TRANSMIT ENABLE
119	D6	COLI/COLO	7	TX (+, -)	; TRANSMIT (+, -) (EXT=1)
120	D5	RXDI/RXDO	8		
121	D4	RXCI/RXCO	9		
122	D3	CRSI/CRSO	10	INPUT/OUTPUT	
123	D2	TXCI/TXCO/STERM	11	D0-D31	; DATA BUS
124	D1		12	DSACK (0, 1)	; DATA AND SIZE ACKNOWLEDGE (0, 1) (BMODE=1)
125	D0			USR (0, 1)	; USER DEFINABLE (0, 1)
				X1	; CRYSTAL DRIVE OR EXTERNAL OSCILLATOR INPUT
126	RA5				
127	RA4				
128	RA3				
129	RA2				
130	RA1				
131	RA0				

