DG858BW45

GATE TURN-OFF THYRISTOR

APPLICATIONS

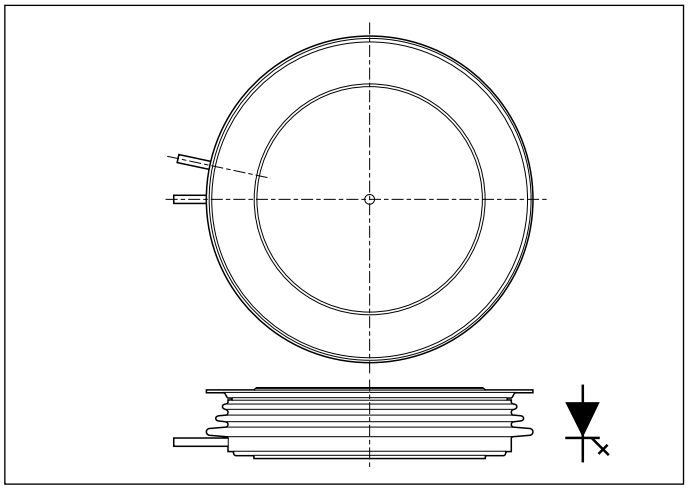
- Variable speed A.C. motor drive inverters (VSD-AC).
- Uninterruptable Power Supplies
- High Voltage Converters.
- Choppers.
- Welding.
- Induction Heating.
- DC/DC Converters.

KEY PARAMETERS

I_{TCM}	3000A
V_{DRM}	4500V
$I_{T(AV)}$	1180A
dV_D/dt	1000V/μs
di_T/dt	300A/μs

FEATURES

- Double Side Cooling.
- High Reliability In Service.
- High Voltage Capability.
- Fault Protection Without Fuses.
- High Surge Current Capability.
- Turn-off Capability Allows Reduction In Equipment Size And Weight. Low Noise Emission Reduces Acoustic Cladding Necessary For Environmental Requirements.



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VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage V_{DRM} V	Repetitive Peak Reverse Voltage V_{RRM} V	Conditions
DG858BW45	4500	16	T_{vj} = 125°C, I_{DM} = 100mA, I_{RRM} = 50mA

CURRENT RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TCM}	Repetitive peak controllable on-state current	V_D = 66% V_{DRM}, T_j = 125°C, di_{GQ}/dt = 40A/μs, Cs = 3μF	3000	A
$I_{T(AV)}$	Mean on-state current	T_{HS} = 80°C. Double side cooled. Half sine 50Hz.	1180	A
$I_{T(RMS)}$	RMS on-state current	T_{HS} = 80°C. Double side cooled. Half sine 50Hz.	1850	A

SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine. T_j = 125°C	20.0	kA
I^2t	I^2t for fusing	10ms half sine. T_j =125°C	2.0 x 10^6	A^2s
di_T/dt	Critical rate of rise of on-state current	V_D = 3000V, I_T = 3000A, T_j = 125°C, I_{FG} > 40A, Rise time > 1.0µs	300	A/µs
dV_D/dt	Rate of rise of off-state voltage	To 66% V_{DRM}; $R_{GK} \leq 1.5\Omega$, T_j = 125°C	130	V/µs
		To 66% V_{DRM}; V_{RG} = -2V, T_j = 125°C	1000	V/µs
L_S	Peak stray inductance in snubber circuit	I_T = 3000A, V_D = V_{DRM}, T_j = 125°C, $dI/_{GQ}$ = 40A/µs, Cs = 3.0µF	200	nH

GATE RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{RGM}	Peak reverse gate voltage	This value maybe exceeded during turn-off	-	16	V
I_{FGM}	Peak forward gate current		20	100	A
$P_{FG(AV)}$	Average forward gate power		-	20	W
P_{RGM}	Peak reverse gate power		-	24	kW
di_{GQ}/dt	Rate of rise of reverse gate current		20	60	A/µs
$t_{ON(min)}$	Minimum permissable on time		50	-	µs
$t_{OFF(min)}$	Minimum permissable off time		100	-	µs

THERMAL RATINGS AND MECHANICAL DATA

Symbol	Parameter	Conditions		Min.	Max.	Units
$R_{th(j-hs)}$	DC thermal resistance - junction to heatsink surface	Double side cooled		-	0.011	°C/W
		Anode side cooled		-	0.017	°C/W
		Cathode side cooled		-	0.03	°C/W
$R_{th(c-hs)}$	Contact thermal resistance	Clamping force 40.0kN With mounting compound	per contact	-	0.0021	°C/W
T_{vj}	Virtual junction temperature			-40	125	°C
T_{OP}/T_{stg}	Operating junction/storage temperature range			-40	125	°C
-	Clamping force			36.0	44.0	kN

CHARACTERISTICS

T_j = 125°C unless stated otherwise					
Symbol	**Parameter**	**Conditions**	**Min.**	**Max.**	**Units**
V_{TM}	On-state voltage	At 4000A peak, $I_{G(ON)}$ = 10A d.c.	-	4.0	V
I_{DM}	Peak off-state current	V_{DRM} = 4500V, V_{RG} = 0V	-	100	mA
I_{RRM}	Peak reverse current	At V_{RRM}	-	50	mA
V_{GT}	Gate trigger voltage	V_D = 24V, I_T = 100A, T_j = 25°C	-	1.2	V
I_{GT}	Gate trigger current	V_D = 24V, I_T = 100A, T_j = 25°C	-	4.0	A
I_{RGM}	Reverse gate cathode current	V_{RGM} = 16V, No gate/cathode resistor	-	50	mA
E_{ON}	Turn-on energy	V_D = 2000V	-	2700	mJ
t_d	Delay time	I_T = 3000A, dI_T/dt = 300A/µs	-	2.0	µs
t_r	Rise time	I_{FG} = 40A, rise time < 1.0µs	-	6.0	µs
E_{OFF}	Turn-off energy	I_T = 3000A, V_{DM} = V_{DRM} Snubber Cap Cs = 3.0µF, di_{GQ}/dt = 40A/µs	-	13500	mJ
t_{gs}	Storage time		-	25.0	µs
t_{gf}	Fall time		-	2.5	µs
t_{gq}	Gate controlled turn-off time		-	27.5	µs
Q_{GQ}	Turn-off gate charge		-	12000	µC
Q_{GQT}	Total turn-off gate charge		-	24000	µC
I_{GQM}	Peak reverse gate current		-	950	A

CURVES

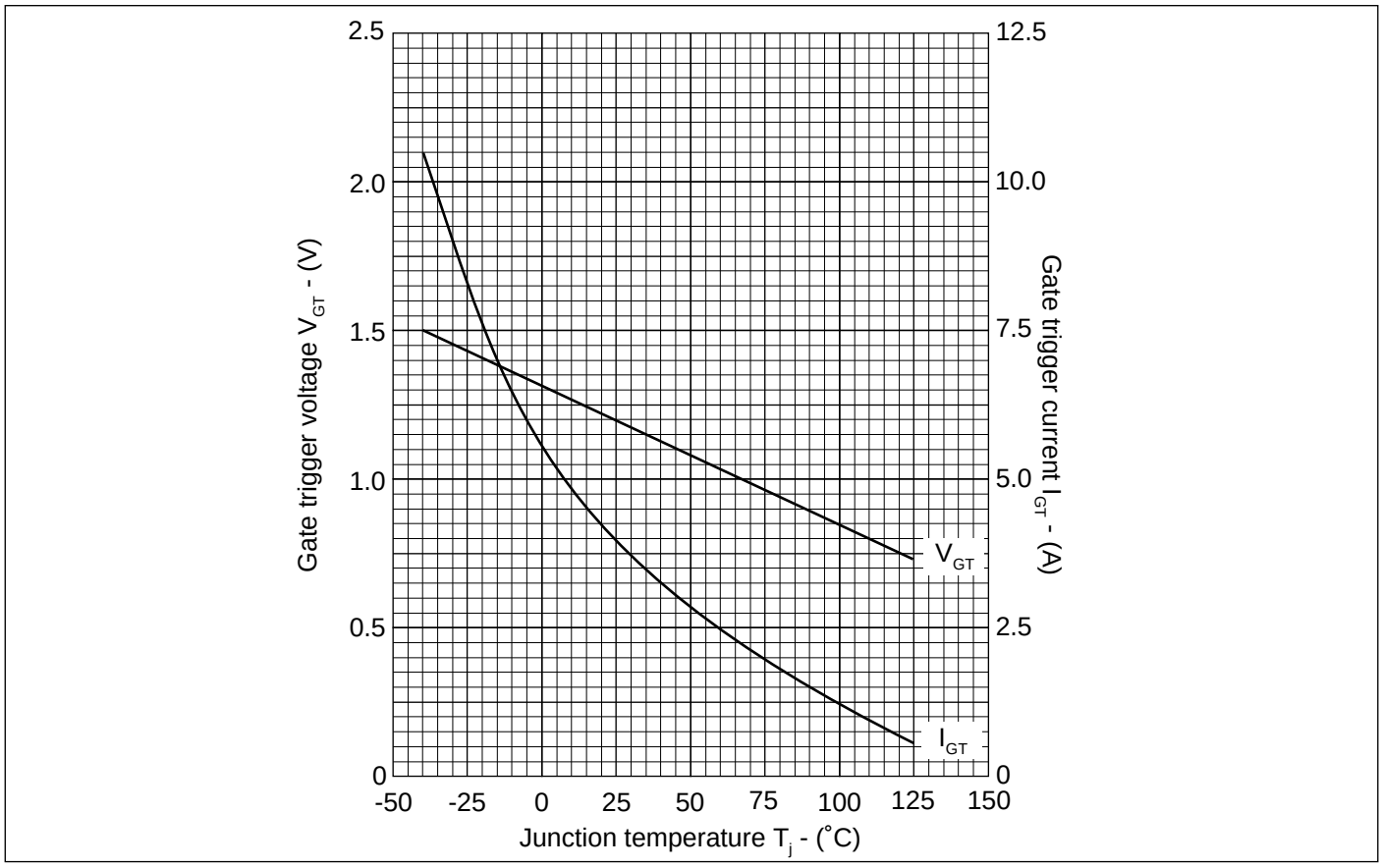


Fig.1 Maximum gate trigger voltage/current vs junction temperature

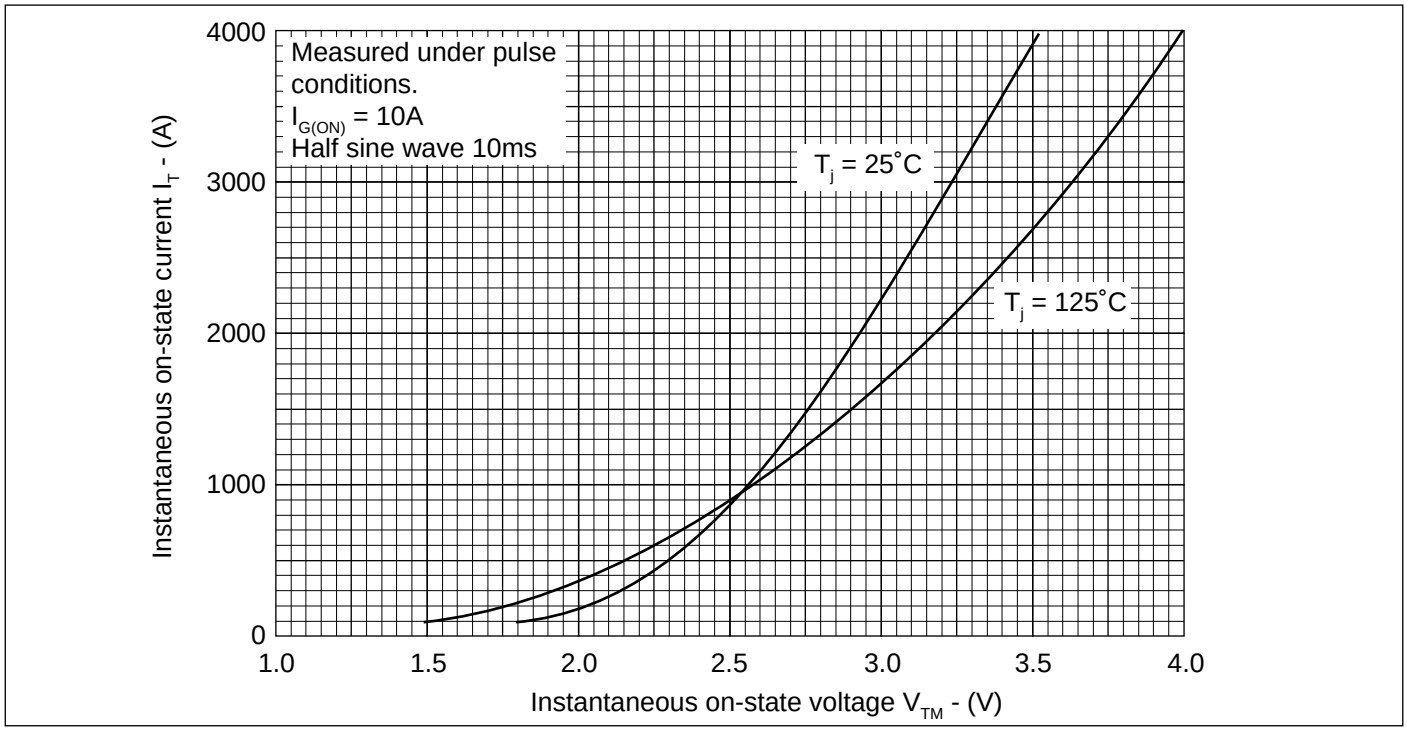


Fig.2 On-state characteristics

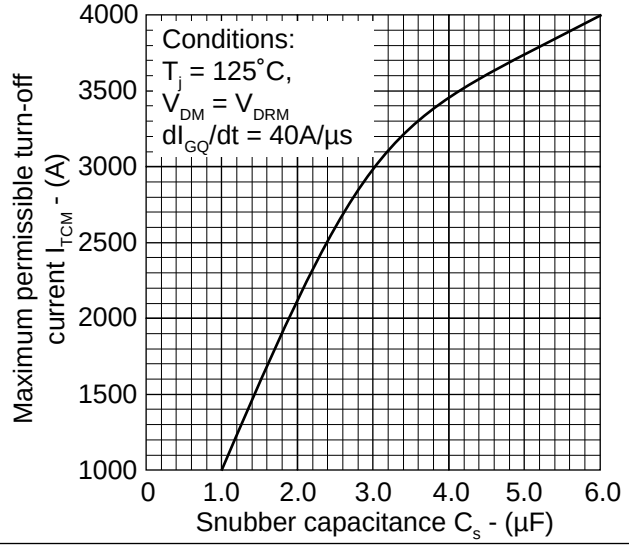


Fig.3 Maximum dependence of I_{TCM} on Cs

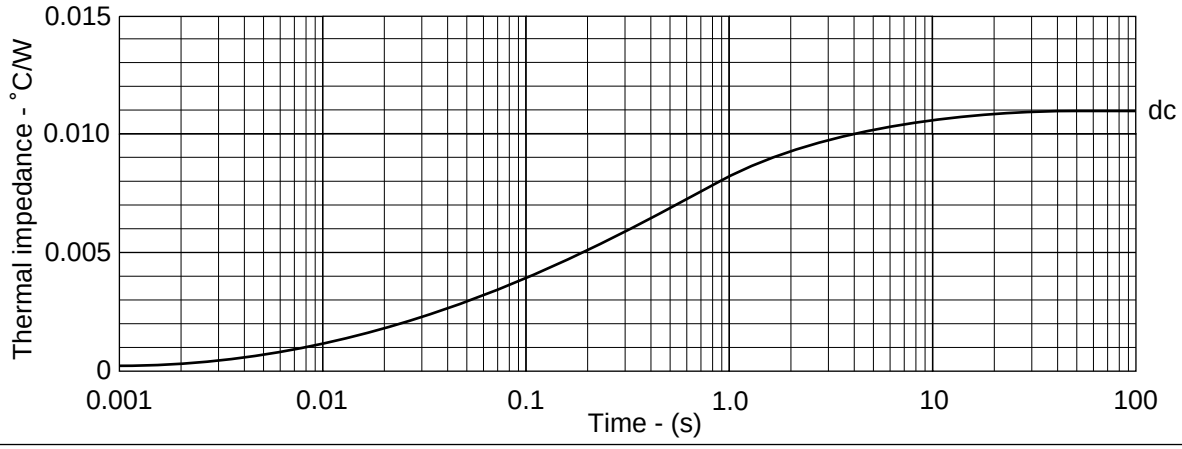


Fig.4 Maximum (limit) transient thermal impedance - double side cooled

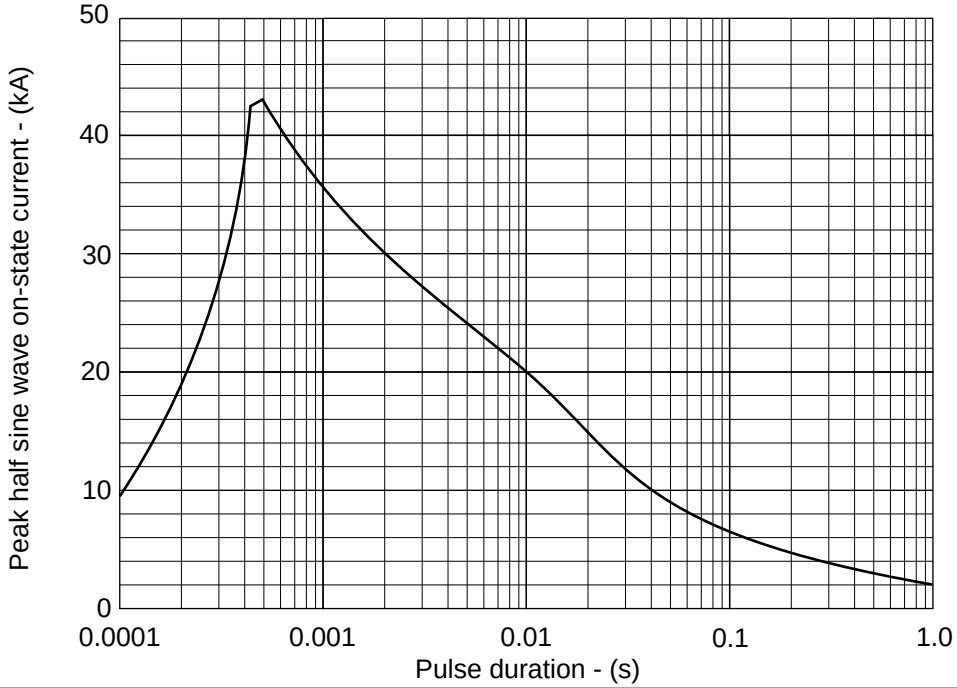


Fig.5 Surge (non-repetitive) on-state current vs time

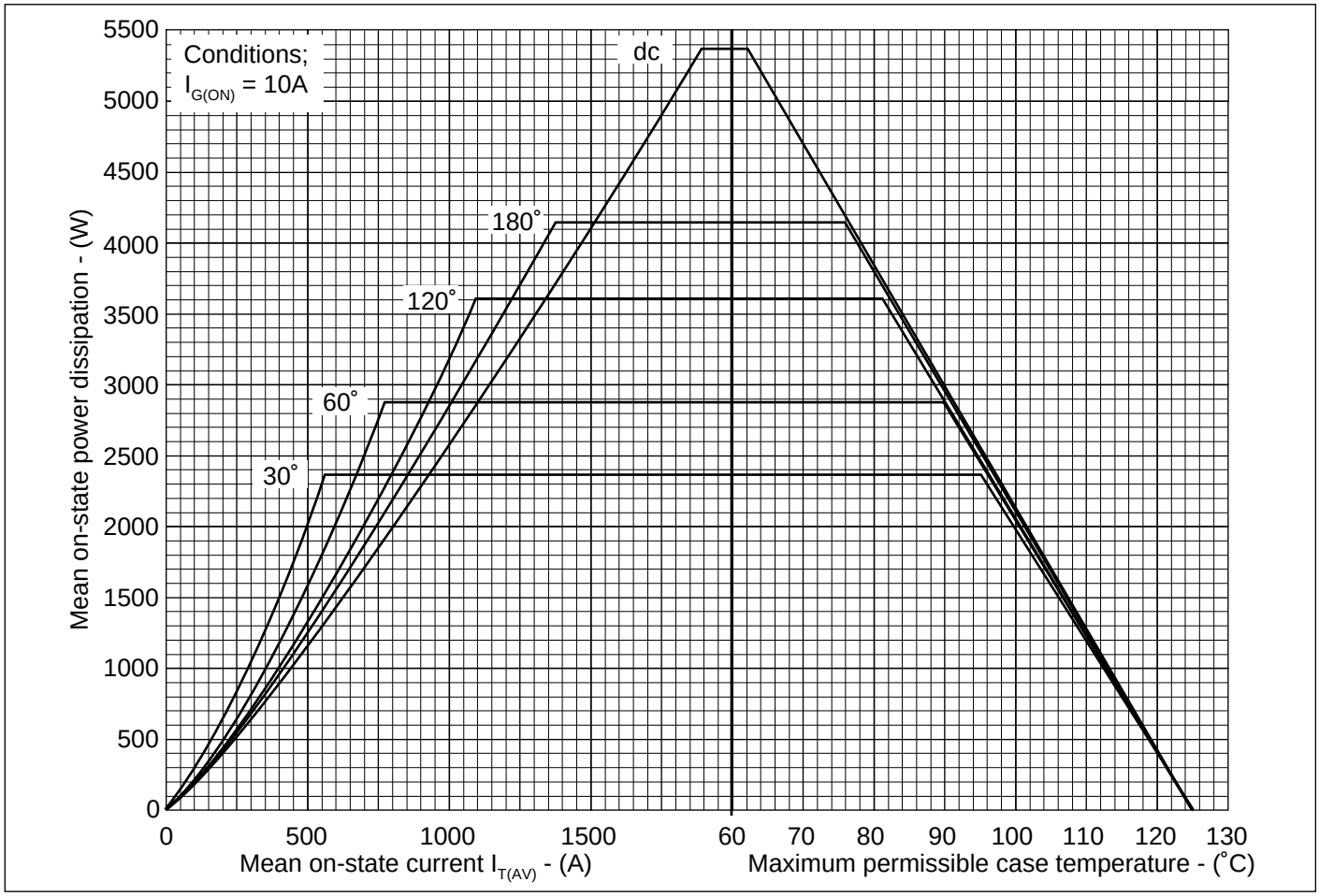


Fig.6 Steady state rectangular wave conduction loss - double side cooled

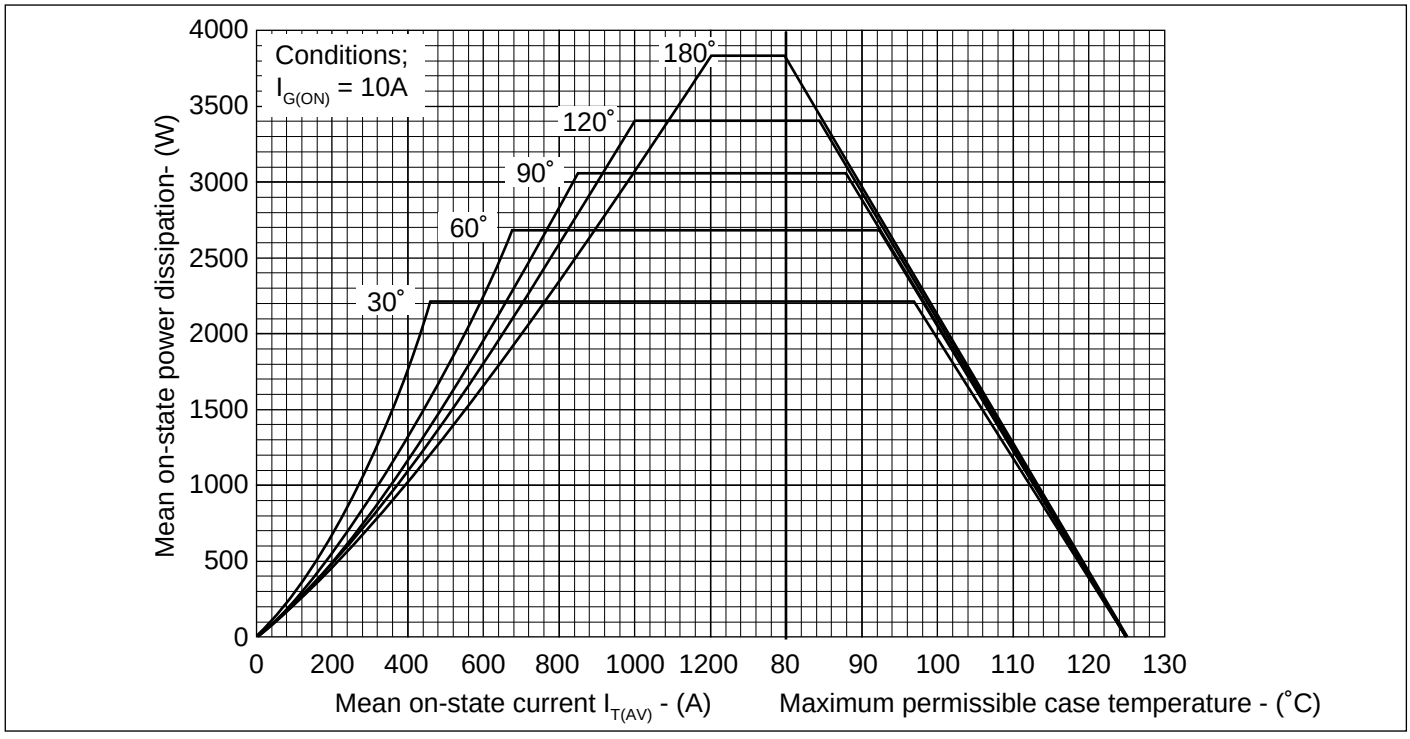


Fig.7 Staedy state sinusoidal wave conduction loss - double side cooled

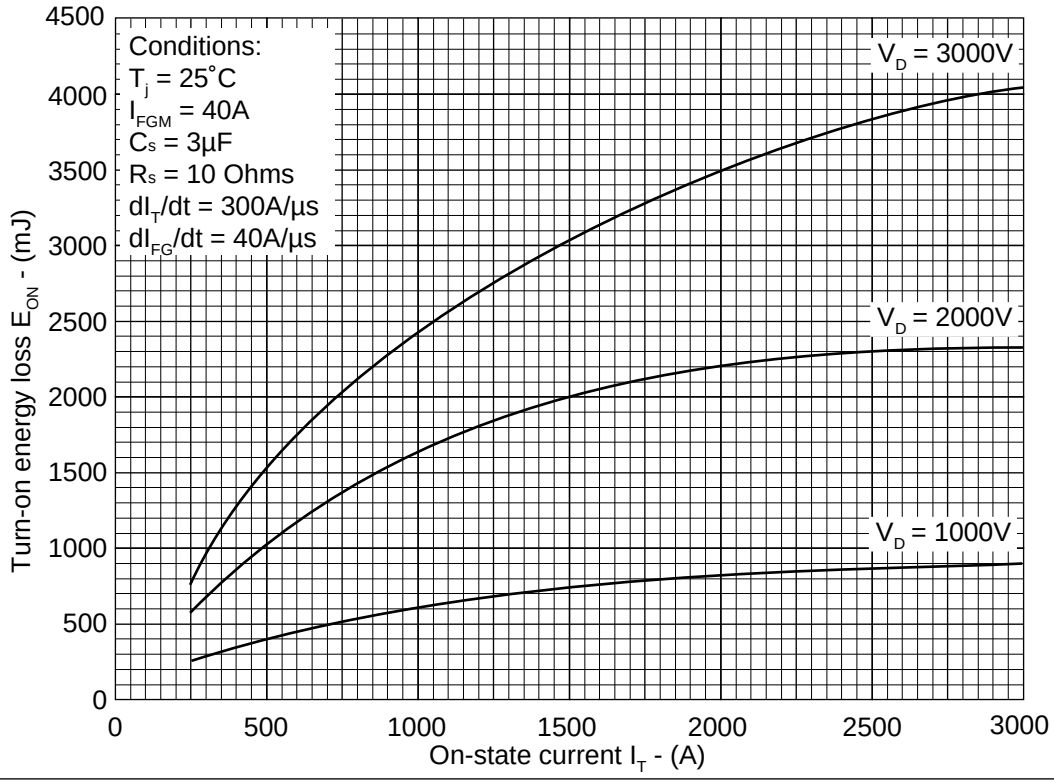


Fig.8 Turn-on energy vs on-state current

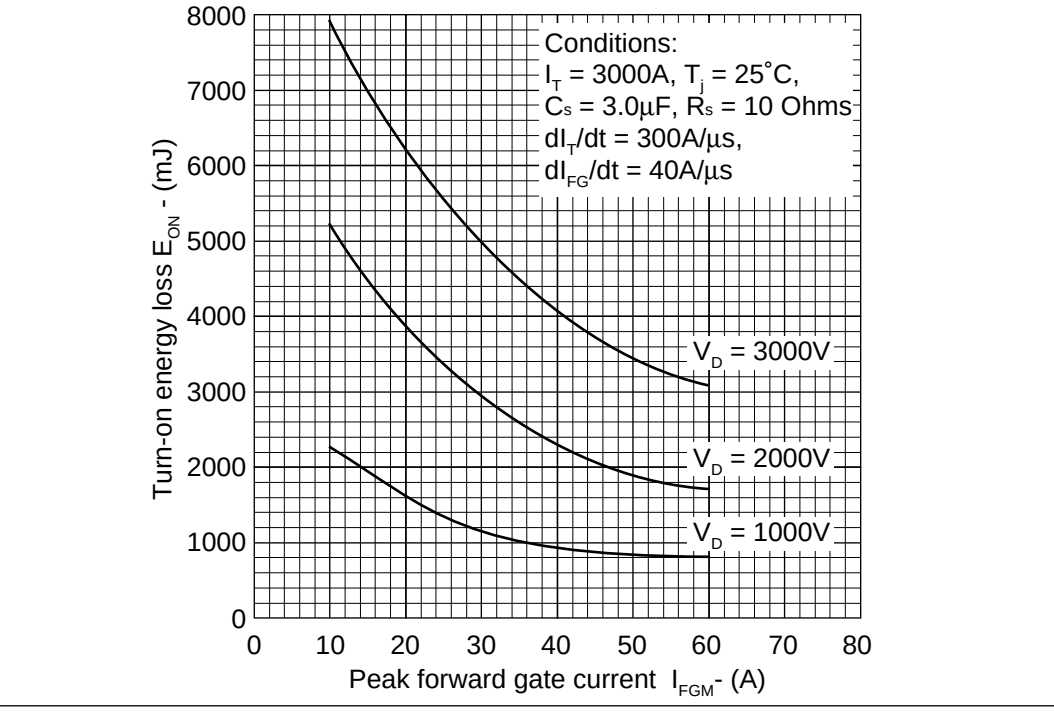


Fig.9 Turn-on energy vs peak forward gate current

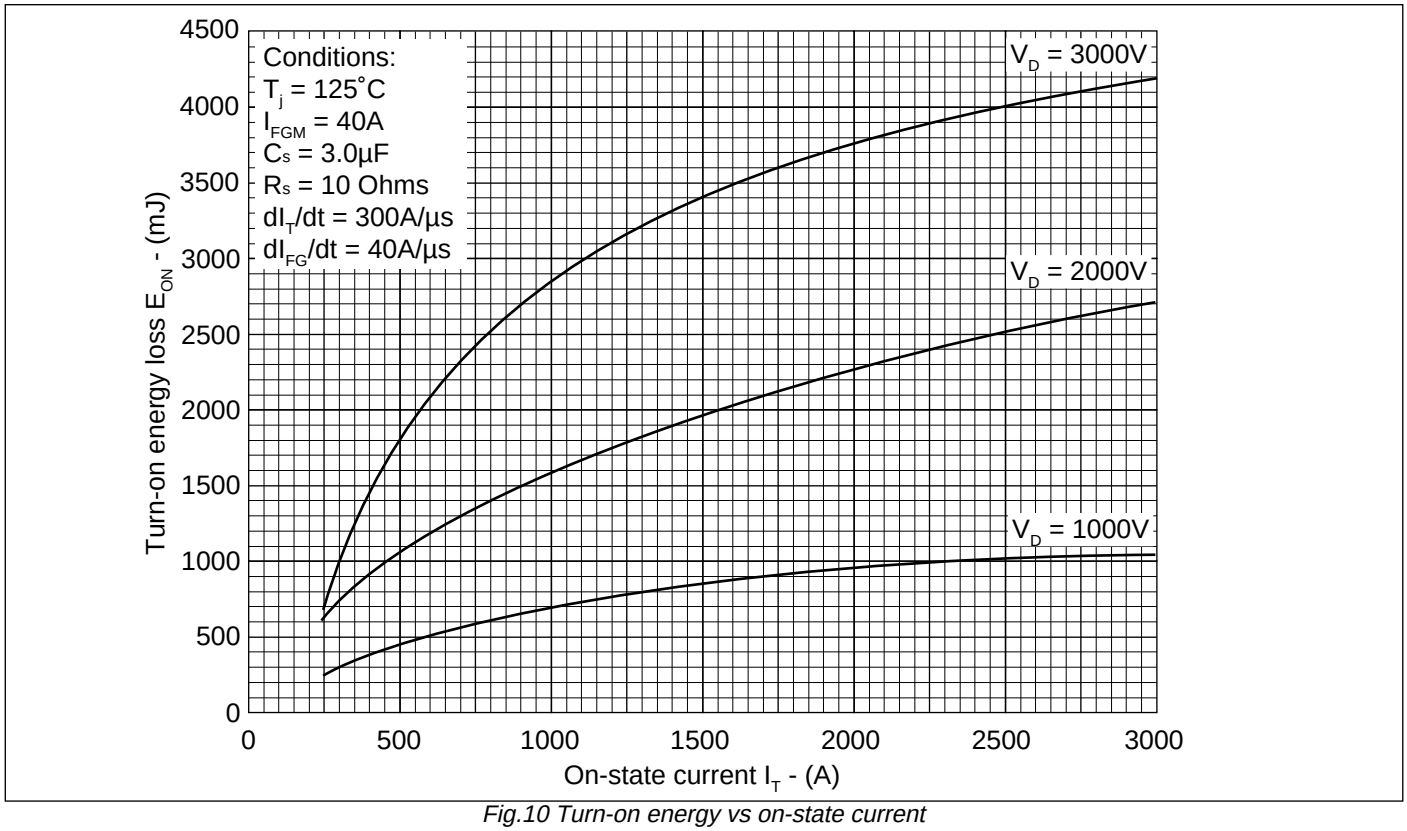


Fig.10 Turn-on energy vs on-state current

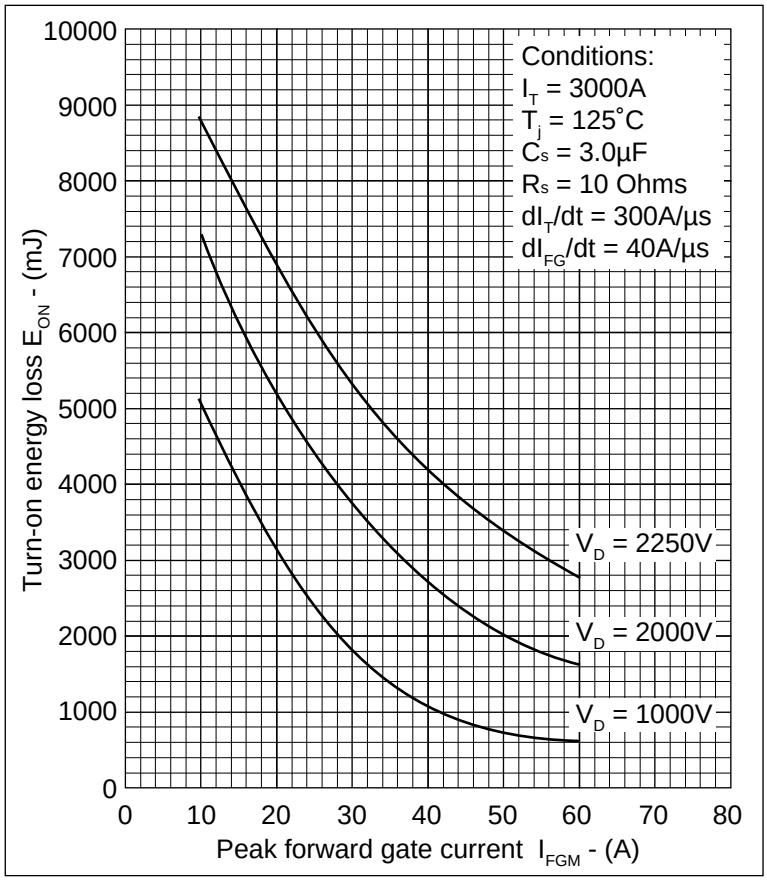


Fig.11 Turn-on energy vs peak forward gate current

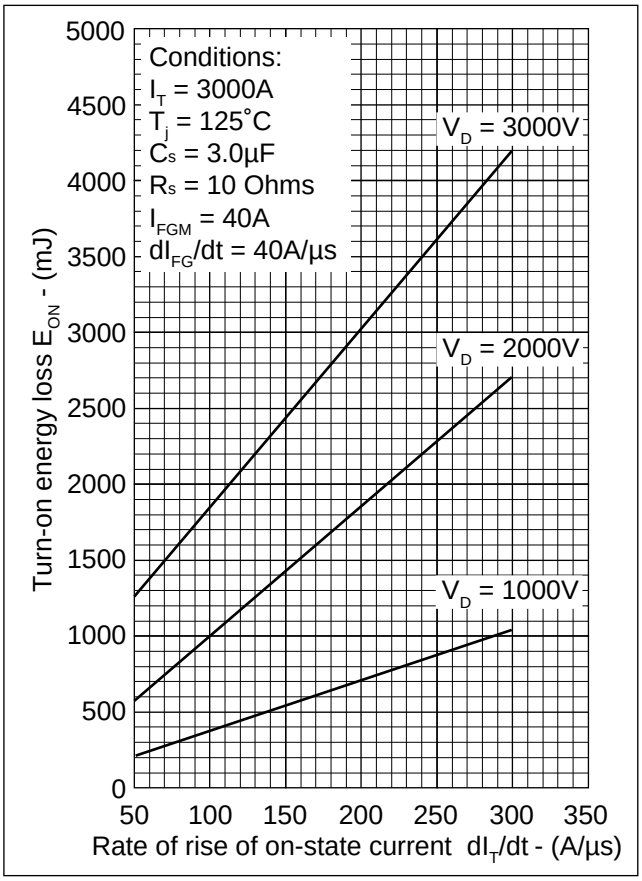


Fig.12 Turn-on energy vs rate of rise of on-state current

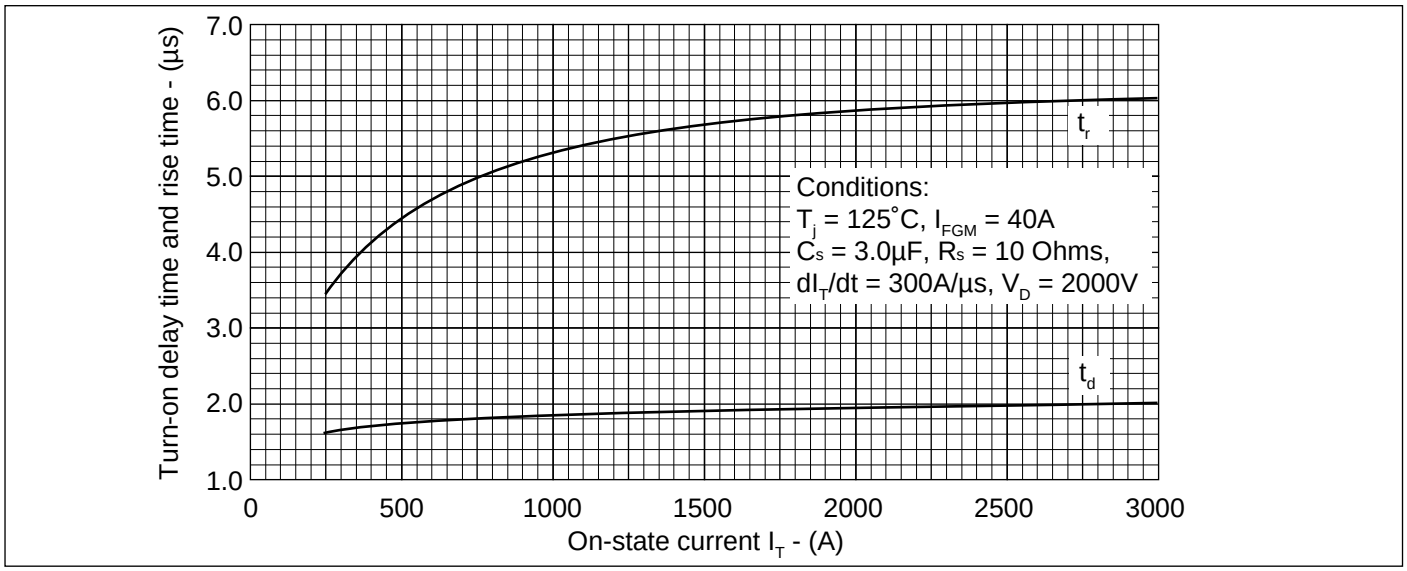


Fig.13 Delay and rise time vs on-state current

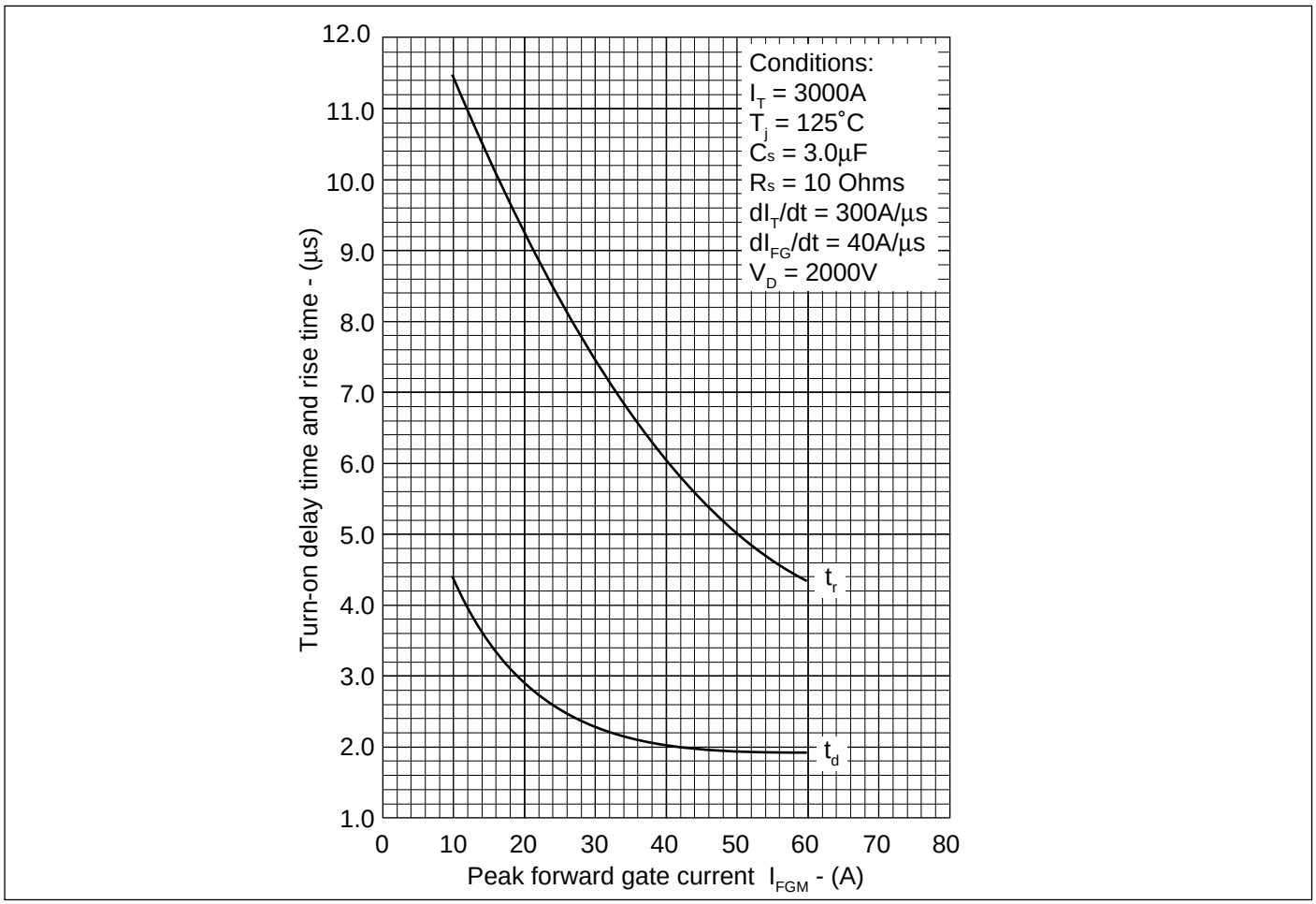


Fig.14 Delay and rise time vs peak forward gate current

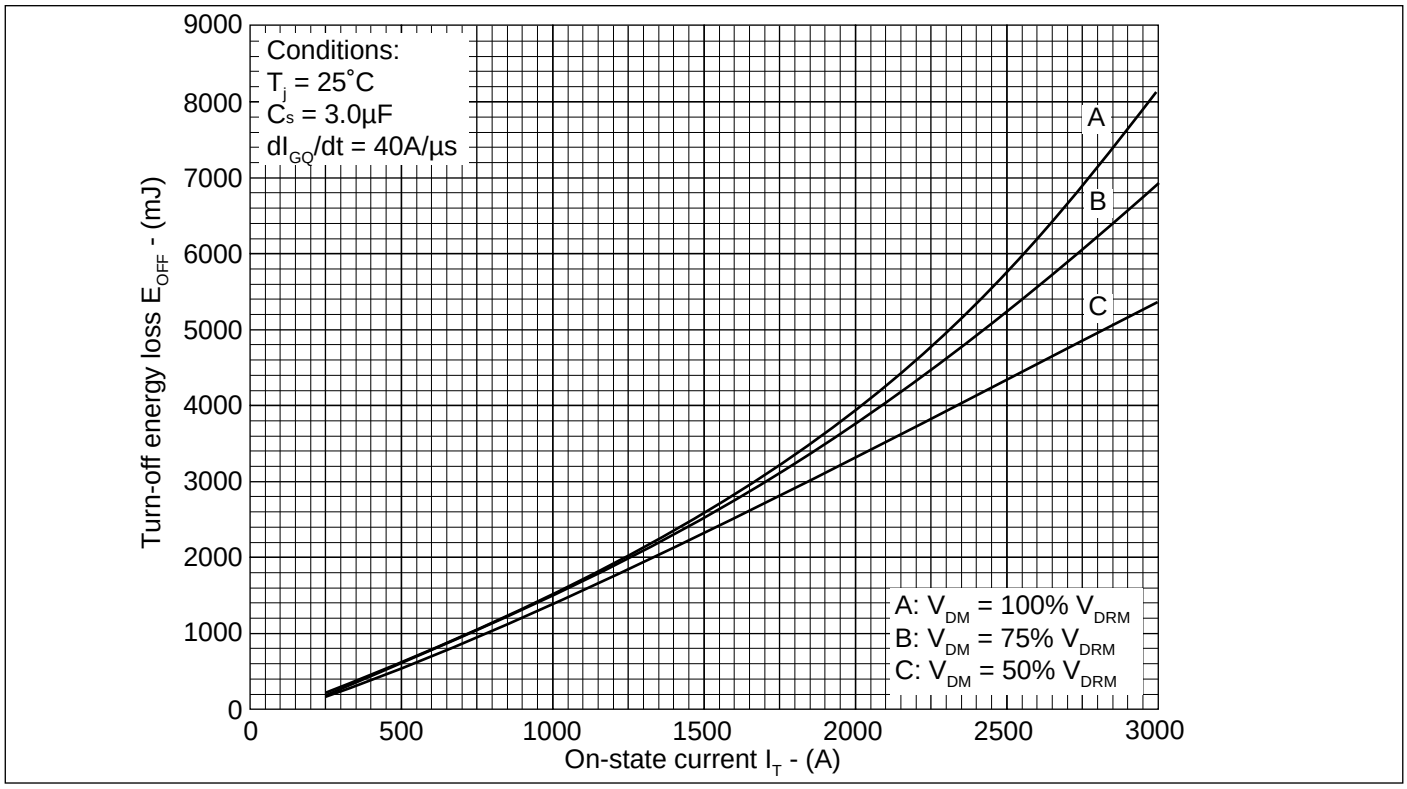


Fig.15 Turn-off energy loss vs on-state current

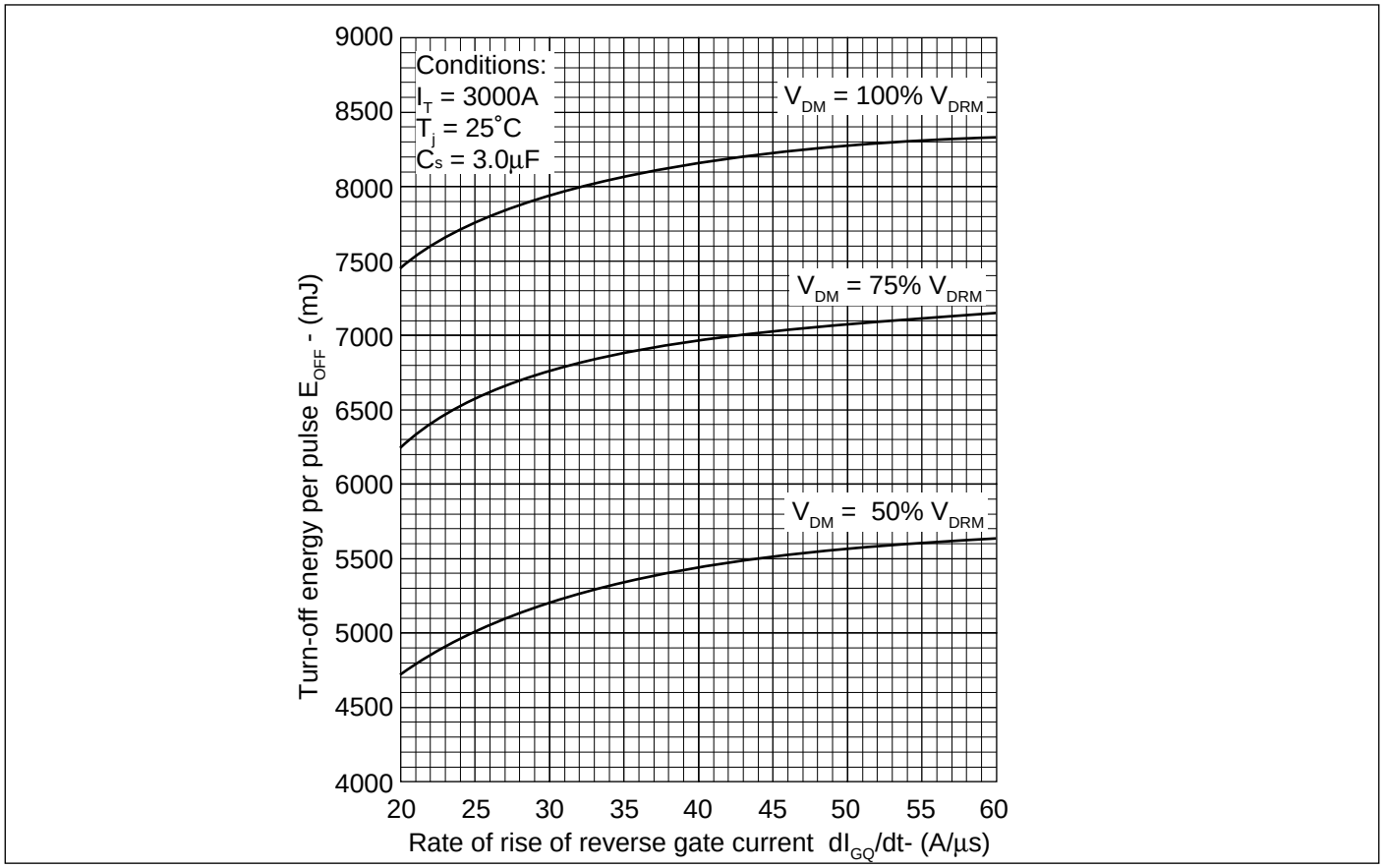


Fig.16 Turn-off energy vs rate of rise of reverse gate current

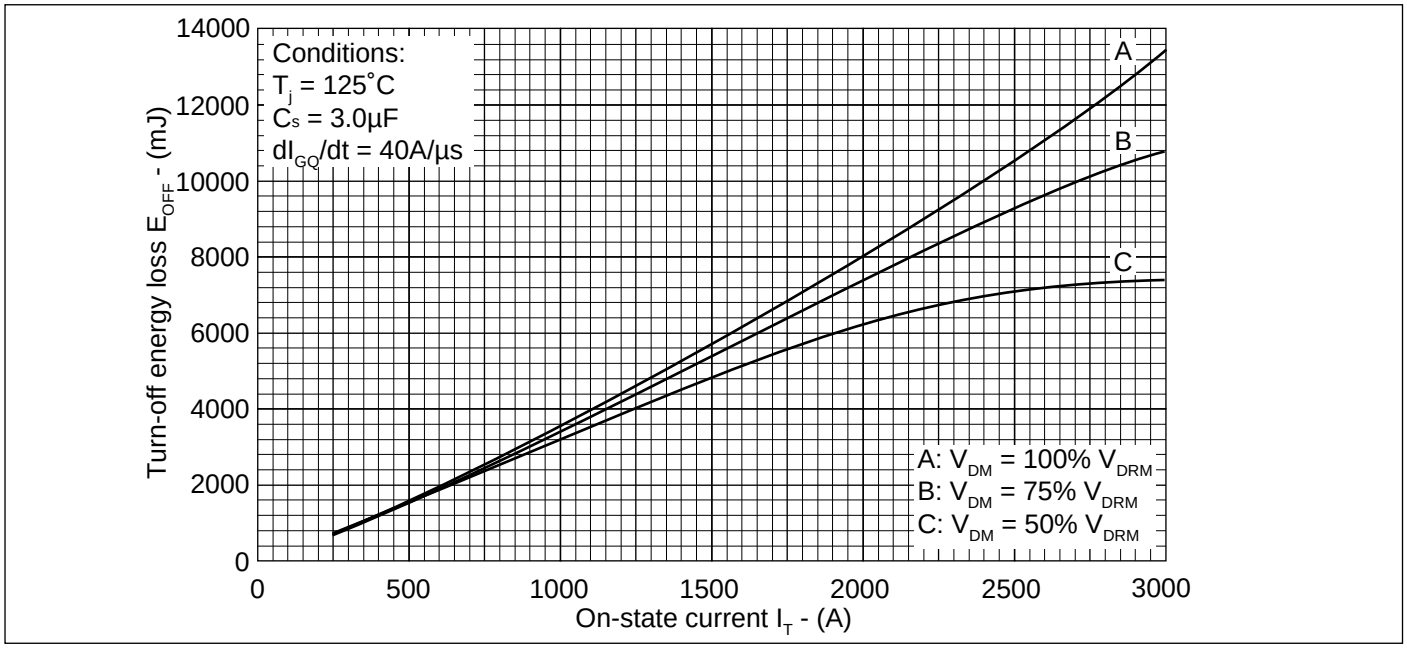


Fig.17 Turn-off energy vs on-state current

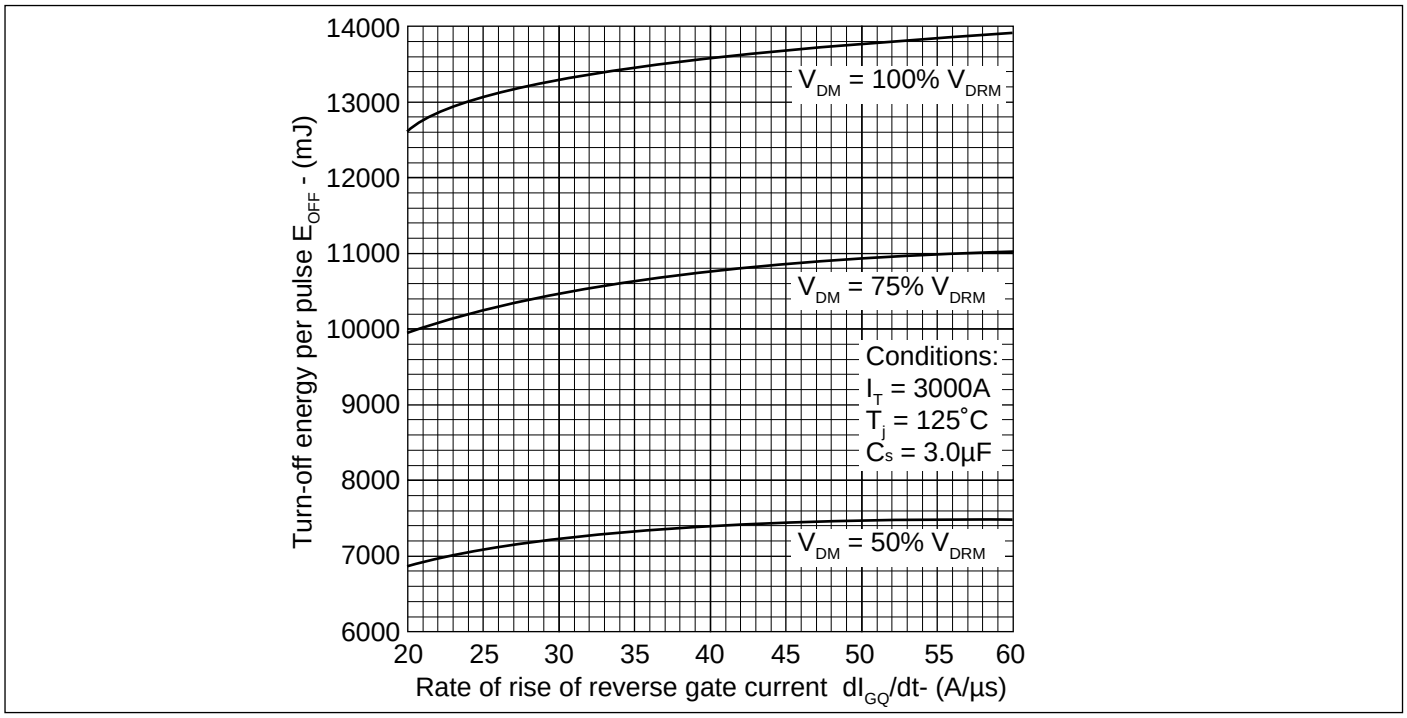


Fig.18 Turn-off energy loss vs rate of rise of reverse gate current

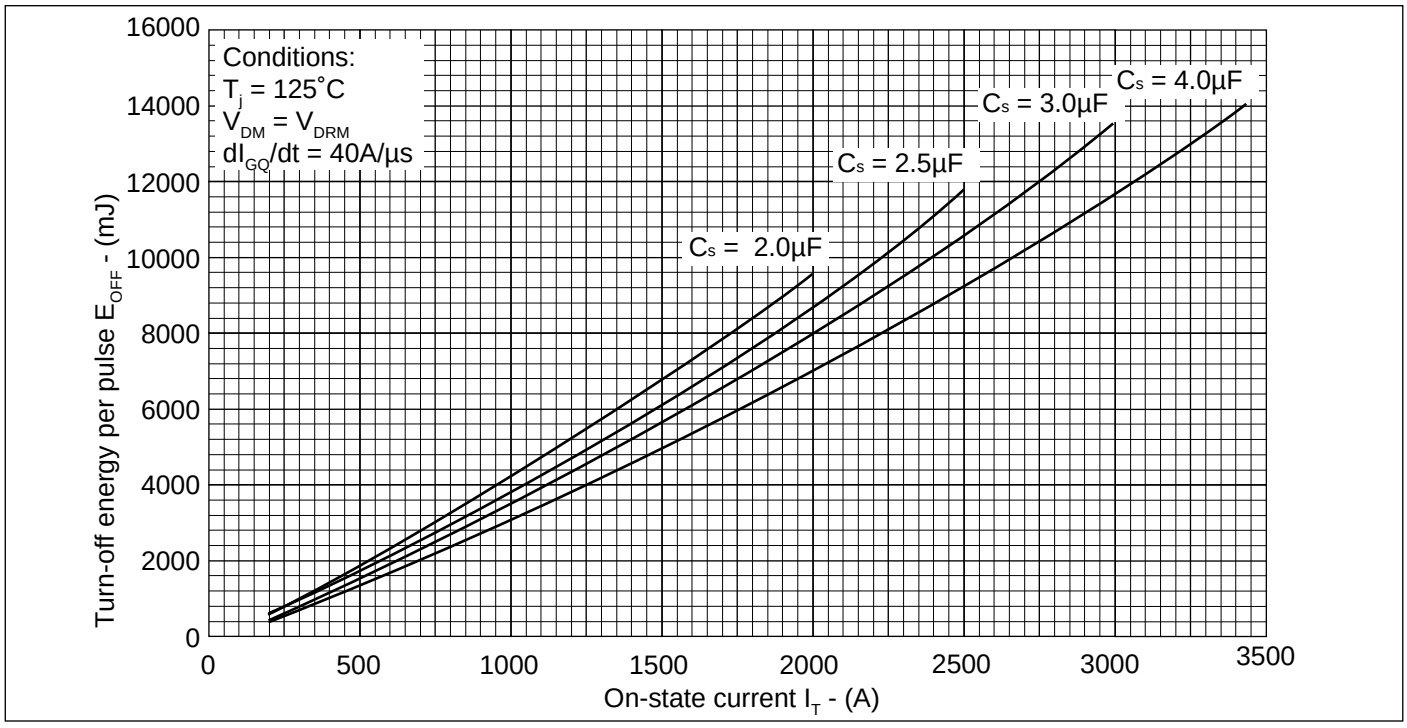


Fig.19 Turn-off energy vs on-state current

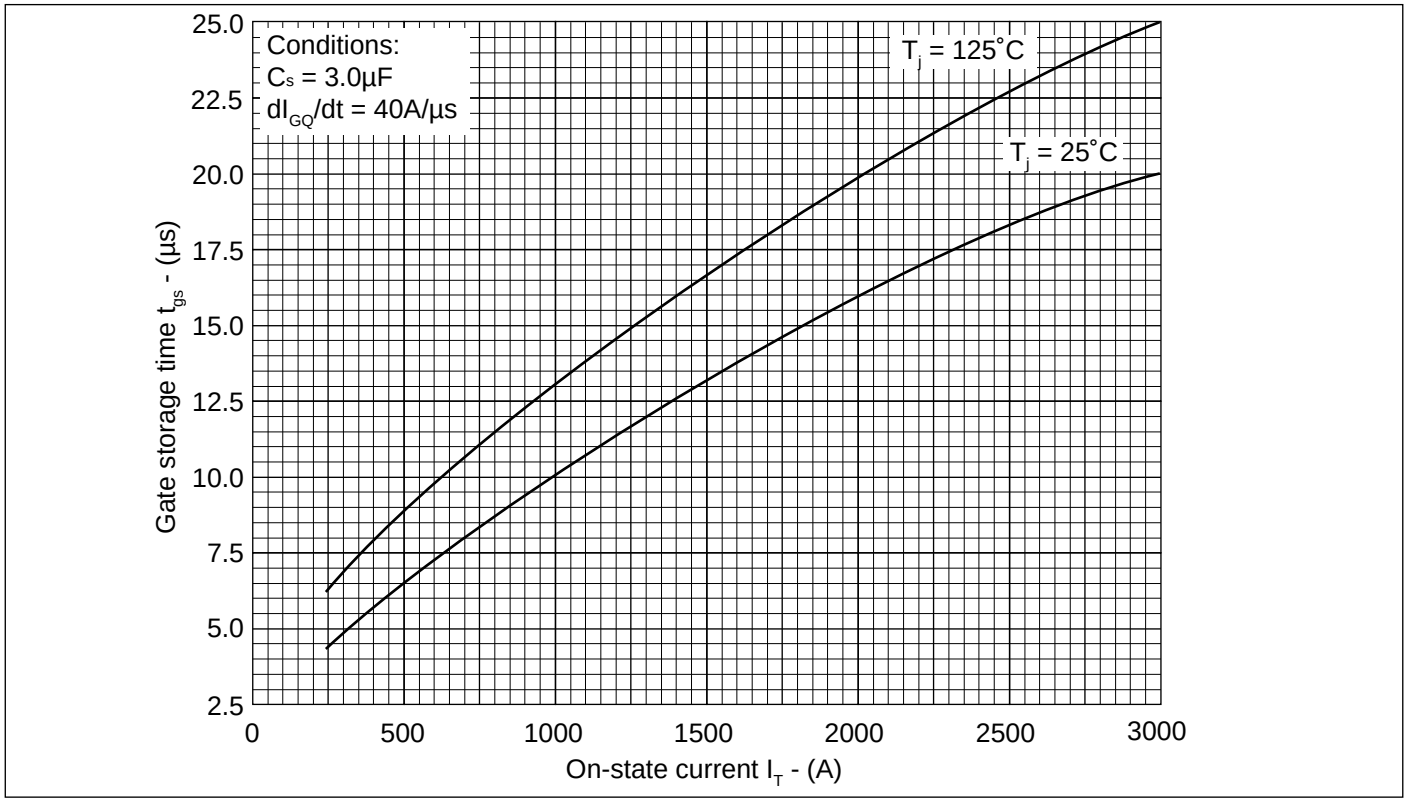


Fig.20 Gate storage time vs on-state current

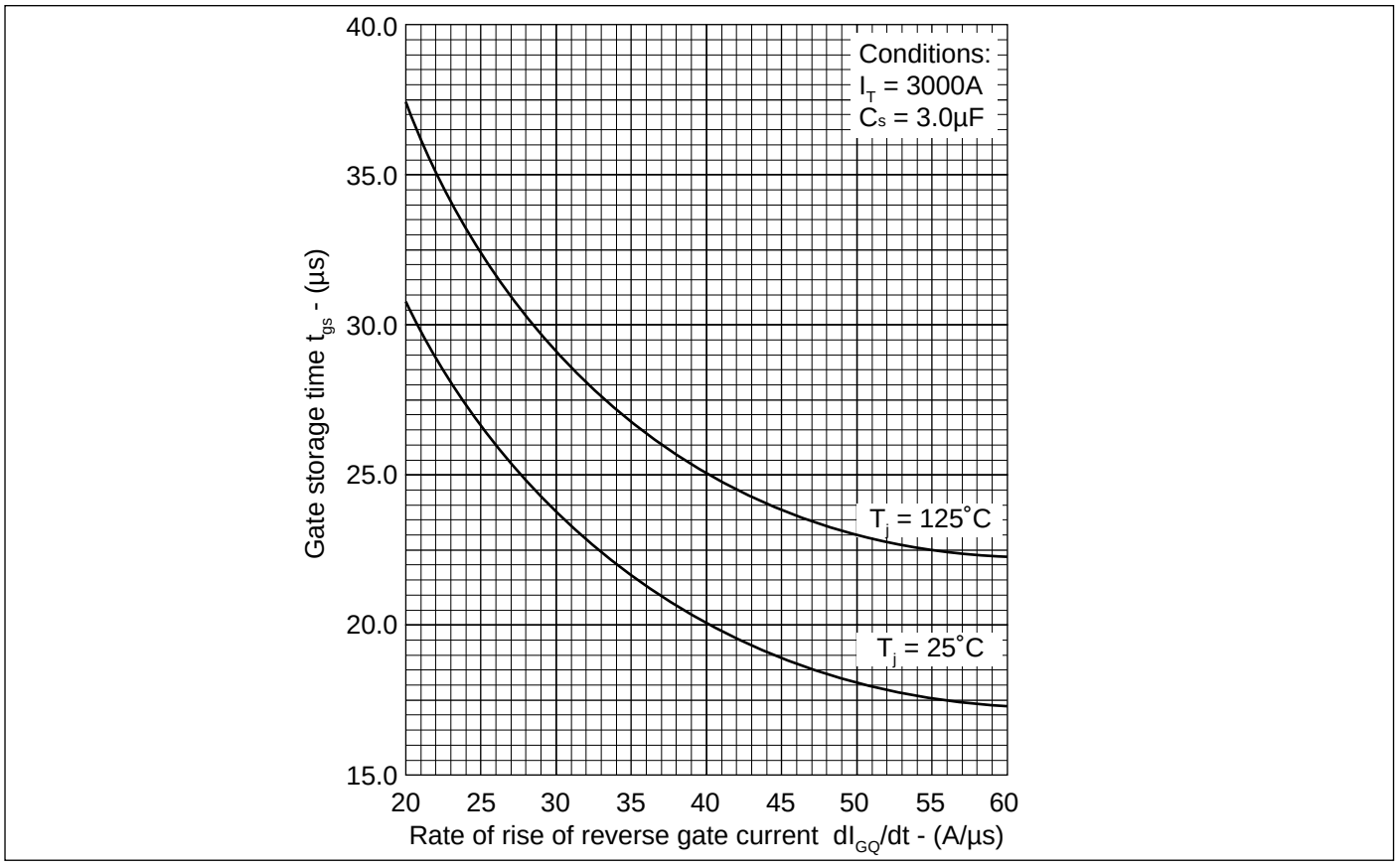


Fig.21 Gate storage time vs rate of rise of reverse gate current

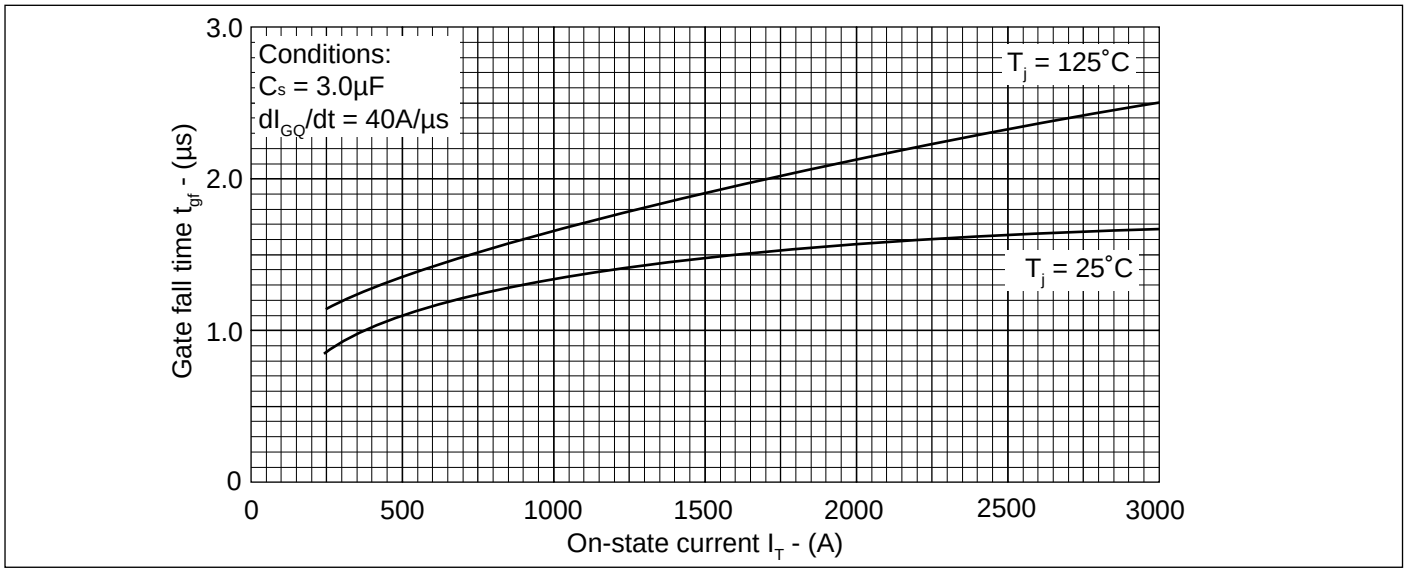


Fig.22 Gate fall time vs on-state current

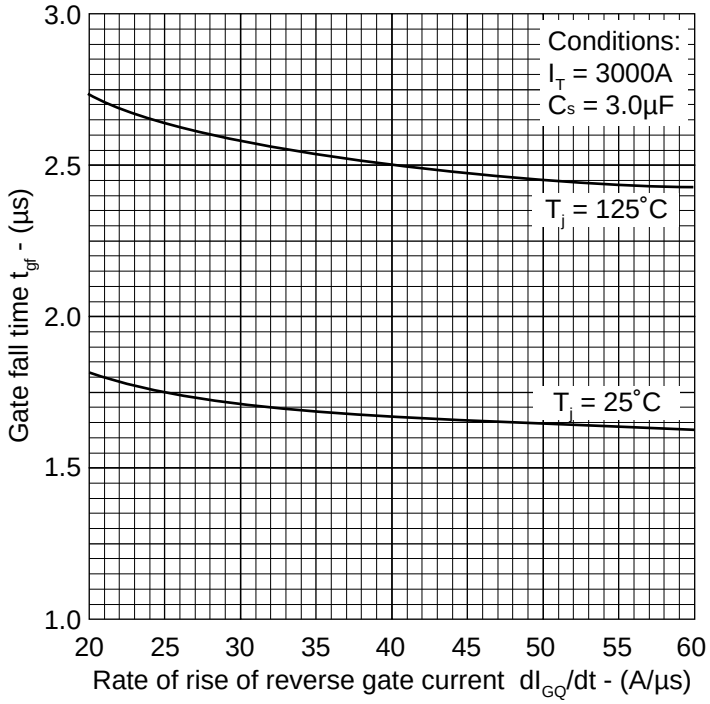


Fig.23 Gate fall time vs rate of rise of reverse gate current

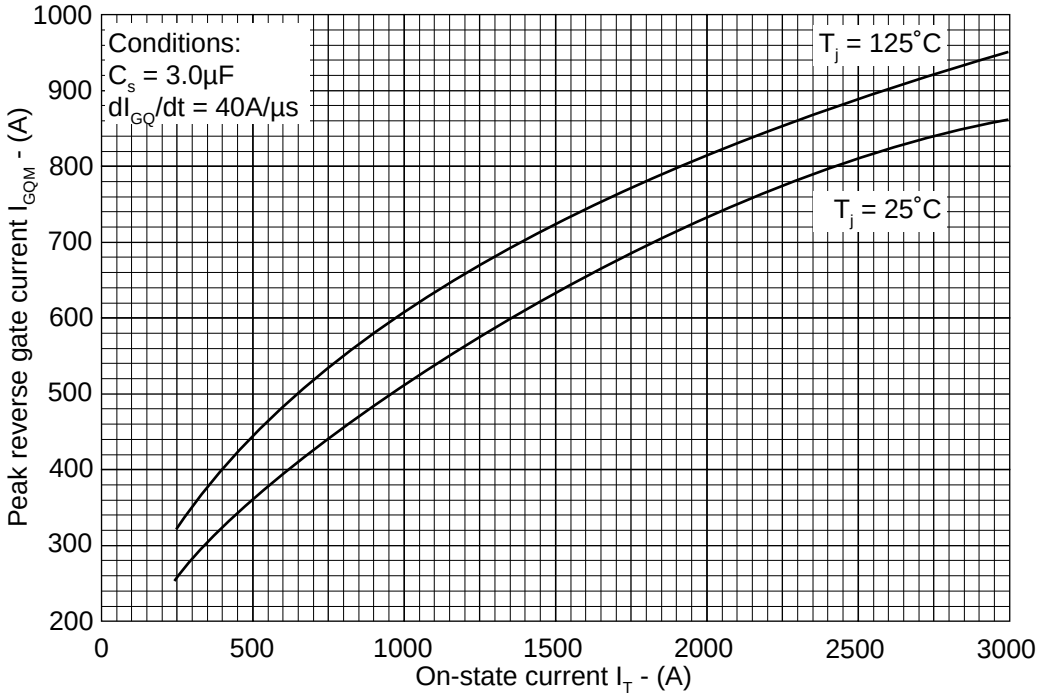


Fig.24 Peak reverse gate current vs on-state current

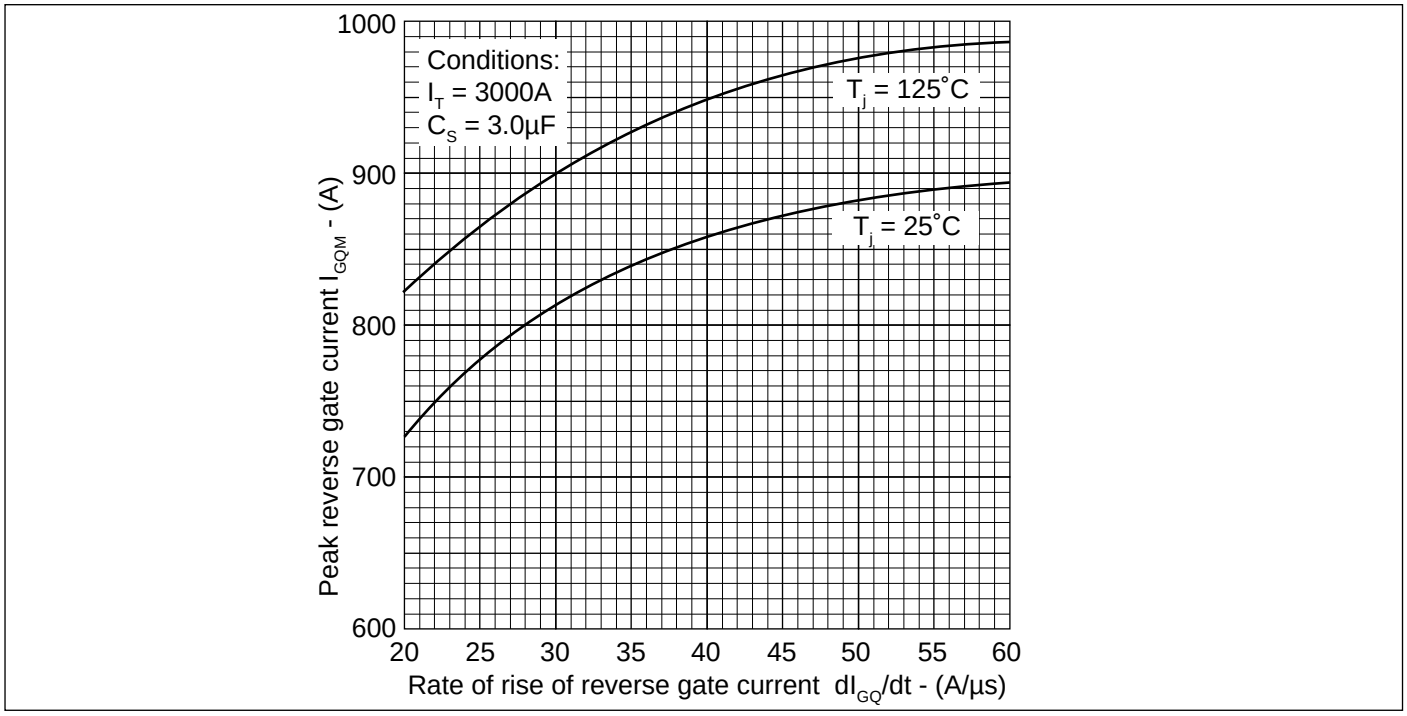


Fig.25 Reverse gate current vs rate of rise of reverse gate current

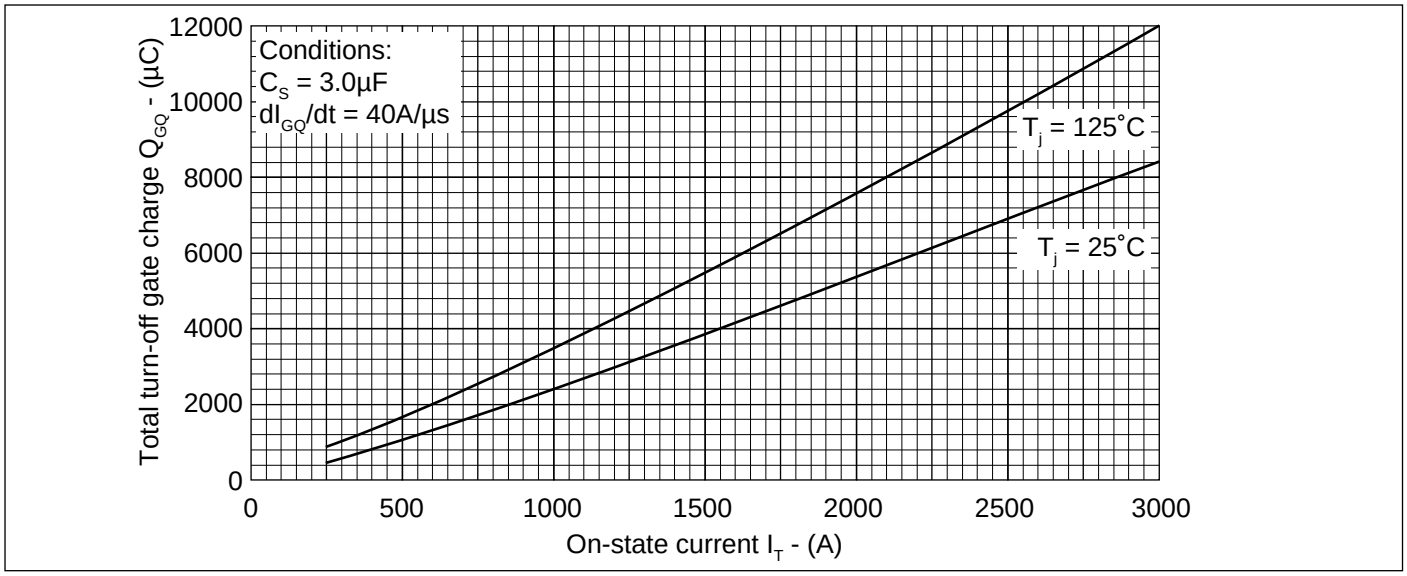


Fig.26 Turn-off gate charge vs on-state current

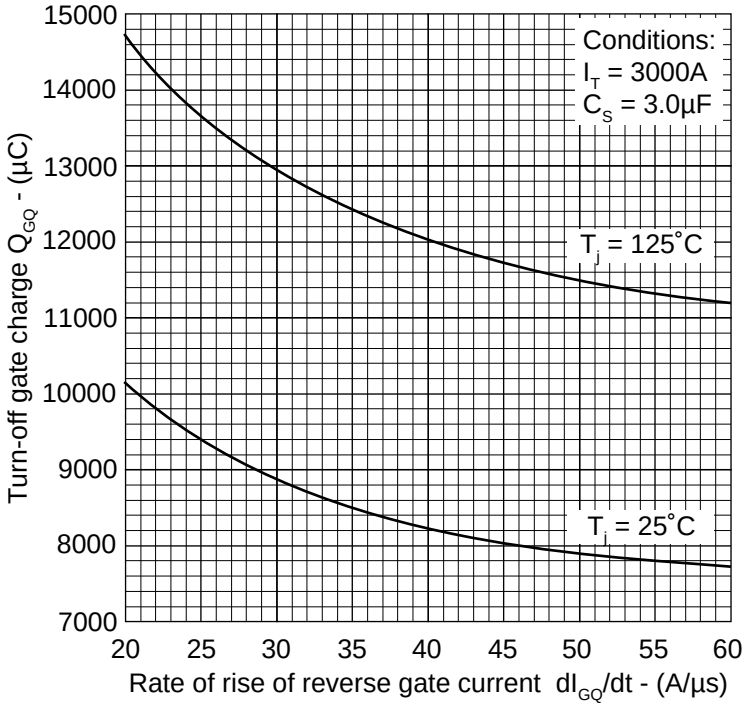


Fig.27 Turn-off gate charge vs rate of rise of reverse gate current

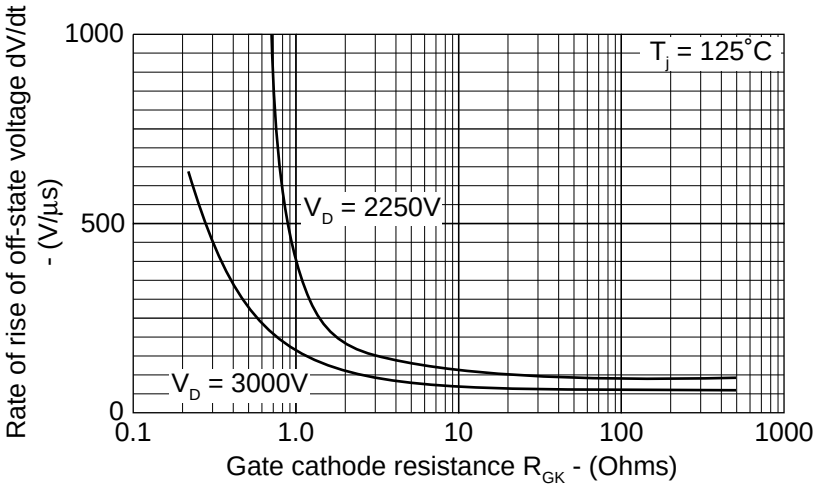
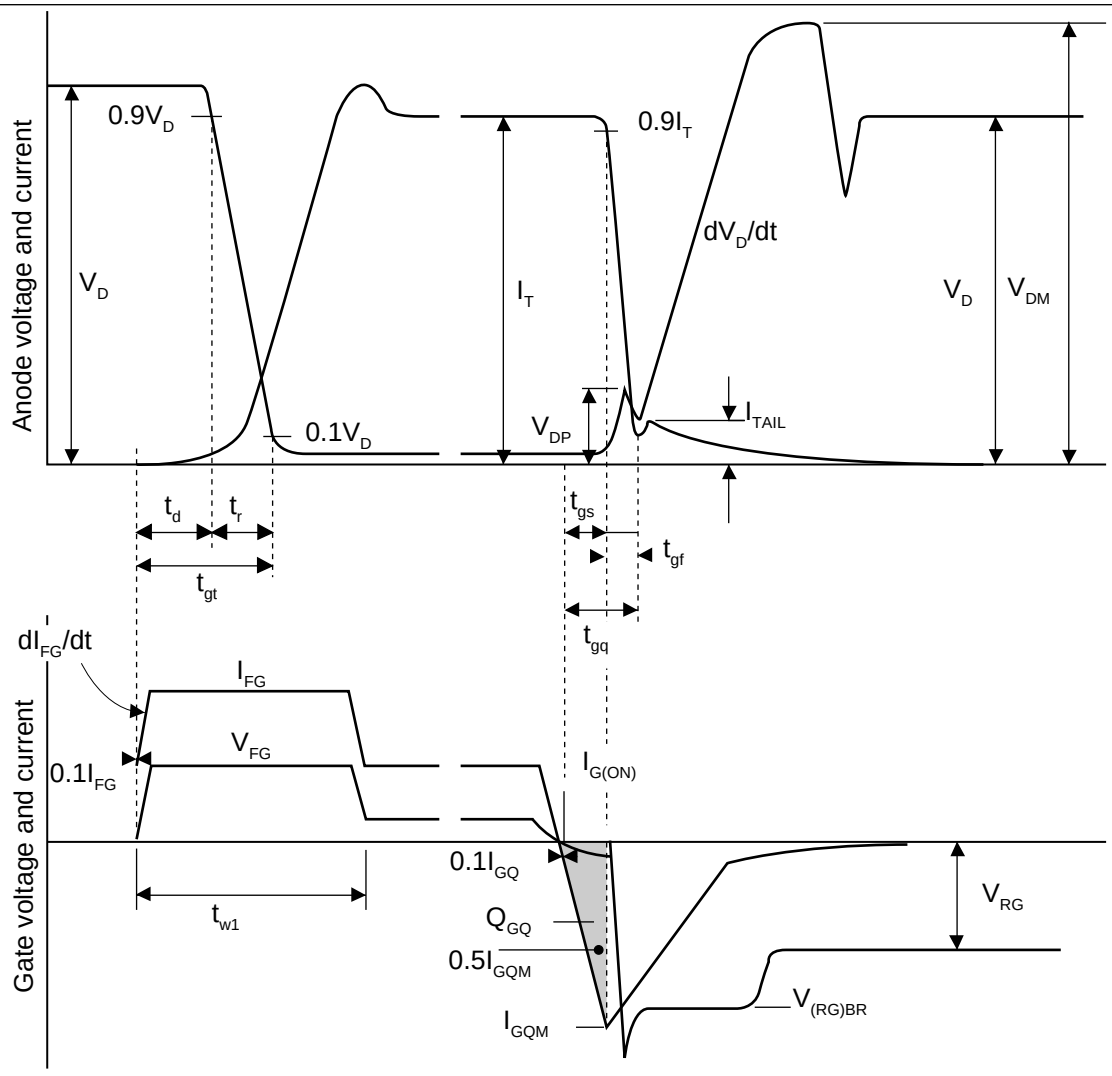


Fig.28 Rate of rise of off-state voltage vs gate cathode resistance



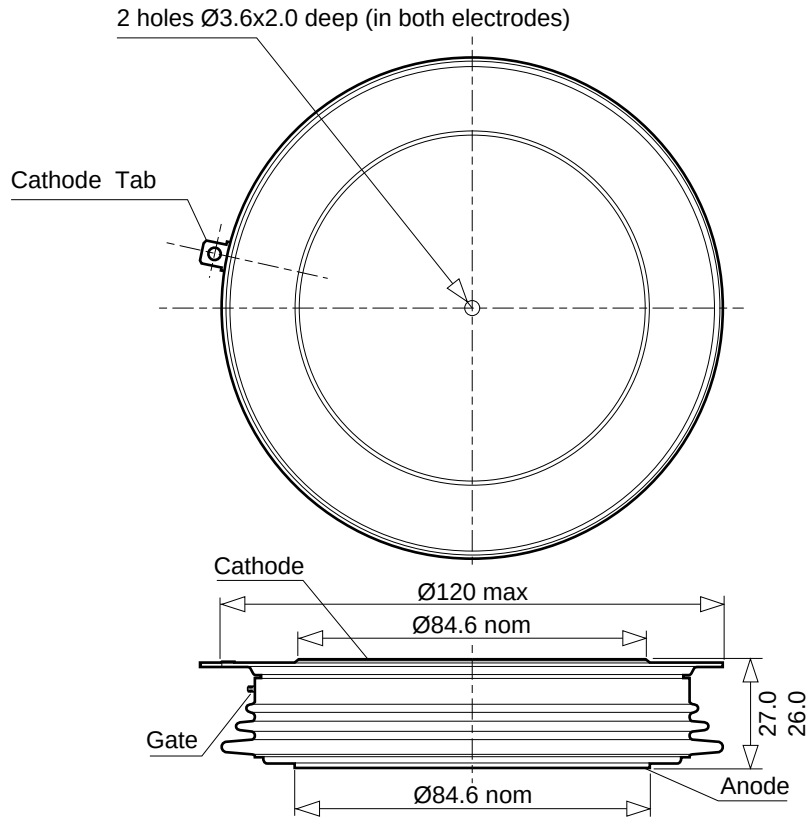
Recommended gate conditions:
I_{TCM} = 3000A
I_{FG} = 40A
$I_{G(ON)}$ = 10A d.c.
$t_{w1(min)}$ = 20µs
I_{GQM} = 1200A
di_{GQ}/dt = 40A/µs
Q_{GQ} = 12000µC
$V_{RG(min)}$ = 2V
$V_{RG(max)}$ = 18V

These are recommended GEC Plessey Semiconductor conditions. Other conditions are permitted according to users gate drive specifications.

Fig.29 General switching waveforms

PACKAGE DETAILS - W

For further package information, please contact your local Customer Service Centre. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



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