

DS3506-7.3

JUNE 1995

DE6003 DIGITAL RADIO TRANSCEIVER

(Supersedes DS3506-6.3, September 1994)

The DE6003 is a high performance frequency hopping microwave radio, designed for spread spectrum operation. It operates in the 2.4 to 2.5GHz band. Portions of this band are available for data transmission on an unlicensed basis in most countries on a shared basis with existing users (that include microwave ovens, intruder alarms etc).

The radio is highly resistant to interference and has many other design features that ensure the most reliable data transfer possible (when used in conjunction with an advanced protocol).

Co-location with other simultaneous users (as well as interferers) is possible, giving an unsurpassed data density in a given area.

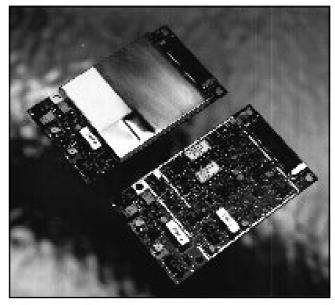
The radio has been designed specifically for portable computer applications (including use 'on the move'). It is also suitable for a wide variety of other applications including inventory control, point of sale terminals (including handheld) and data logging.

FEATURES

- Rapid Frequency Hopping with 1MHz Channels 2.4 to 2.5GHz
- Designed To Meet World Wide Standards
- 625 kb/s Data Rate
- Highly Selective Receiver, Wide Dynamic Range
- High Simultaneous User Density
- Diversity for Mobile Applications
- Fast Switching for Support of Advanced, Interference Resistant Protocols
- Miniature Size with Low Power Consumption for Handheld Use

ORDERING INFORMATION

DE6003-001 Max. transmit power: +20dBm DE6003-002 Max. transmit power: +22dBm



DE6003 digital radio transceiver

RELATED DOCUMENTS

GPS Outline drawing number: M50633-A2 FCC Rule 15.247 ETSI ETS 300-328 Japanese specification number RCR STD-33 ISO9000 Quality Manuals GPS application notes AN142,143,144,145, 154 and 203 for further design information

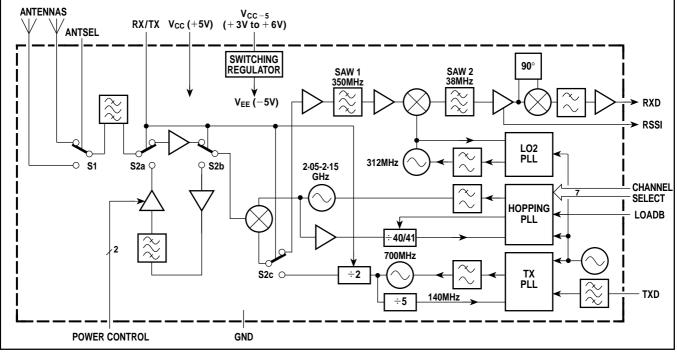


Fig.1 DE6003 functional block diagram

EXTERNAL INTERFACE

The DE6003 transceiver has a simple external interface, with all but three interface connections having CMOS compatible switching levels: some inputs have pull-down or pull-up resistors. The DE6003 connection list, Table 2, is followed by a description of each of the external connections in pin number order.

On power up, the DE6003 transceiver should have its control inputs set to receive with the power amplifier off. On power switch-on, a channel within the 101 channels is selected by the value that is on the select data inputs SD(6:0); the correct channel should be loaded by placing the channel number on the select data inputs and strobing the channel data in with LOADB.

The antenna select input (ANTSEL) is used to switch between the two antenna ports; this input should be set to antenna 1 for transmit and only switched when the transceiver is in receive mode for antenna diversity selection.

The data input (TXD) has data applied in simple non-return to zero (NRZ) format with the maximum consecutive '1's or '0's limited to 16. Receive data (RXD) is demodulated and output in NRZ format with no clock extracted. The RXD output is designed to drive a high impedance CMOS input with a maximum load capacitance of 6pF. Loads in excess of 6pF will extend the negative edge time of the output data resulting in pulse stretching.

ELECTRICAL CHARACTERISTICS

The Electrical Characteristics are guaranteed over the following range of operating conditions, unless otherwise stated: $T_{AMB} = 0^{\circ}C$ to +55°C, $V_{CC} = 5V\pm5\%$, $V_{CC-5} = +3V$ to +6V.

		Value			
Characteristic	Symbol	Min.	Max.	Units	Conditions/comments
All Inputs Input voltage low Input voltage high	V _{IL} V _{IH}	0 3·5	1∙5 V _{CC}	V V	
PAOFF, PWRLO, ANTSEL Input current low Input current high	I _{IL} I _{IH}		-10 10	μΑ μΑ	$V_{IN} = 0V$ $V_{IN} = V_{CC} = 5.25V$
RX/TX Input current low Input current high	I _{IL} I _{IH}	-400 50	-600 150	μΑ μΑ	$V_{IN} = 0V$ $V_{IN} = V_{CC} = 5.25V$
LOADB Input current low Input current high	I _{IL} I _{IH}	-250	-400 10	μΑ μΑ	$V_{IN} = 0V$ $V_{IN} = V_{CC} = 5.25V$
STDBY Input current low Input current high	I _{IL} I _{IH}		-10 200	μΑ μΑ	$V_{IN} = 0V$ $V_{IN} = V_{CC} = 5.25V$
SD (6:0), TXD Input current low Input current high	I _{IL} I _{IH}		-10 200	μΑ μΑ	
SYNLOK Output voltage low Output voltage high	V _{OL} V _{OH}	0 V _{CC} −0•5	0∙5 V _{CC}	V V	Note: Not CMOS compatible switching levels. at 1mA sink at 1mA source
RXD Output voltage low Output voltage high Rise/fall time	V _{OL} V _{OH}	0 3·8 75	1.2 V _{CC} 150	V V ns	V _{CC} =+5V at 100μA V _{CC} =+5V at 100μA Load = 6pF
CLK Output current low Output current high	I _{OL} I _{OH}	-0·25 0·25	-1.6 1.6	mA mA	Note: Not CMOS compatible switching levels. For load impedance $\leq 300\Omega$ See AN142 for interface circuit
RSSI Output voltage low Output voltage high	V _{OL} V _{OH}	0	3.3	V V	Note: Analog output, source impedance $10k\Omega - not$ CMOS compatible. See Fig 9.
ANT1, ANT2 Isolation between ports		10	30	dB	Nominal 50 Ω load on each port
Negative Supply, V_{EE} Output current Output voltage Ripple and noise	I _{EE} V _{EE}	0 -4·75	-15 -5∙25 50	mA V mVp-p	Test at V _{CC-5} = +5V at -15mA

2

EXTERNAL CONNECTIONS, 40-WAY CONNECTOR

Pin	Name	Description
1	FRMGND	Frame Ground. Connects to antistatic circuits on DE6003 and internally connected to ground.
2,4,6	V _{CC}	+5V supply pins.
3	PWRLO	Power Level Control. Sets transmitter power to high (PWRLO = '1') or low (PWRLO = '0').
5	ANTSEL	Diversity Control. This signal is used to select antenna port ANT1 (ANTSEL = '0') or antenna port ANT2 (ANTSEL = '1'). This can be used to make use of diversity to overcome signal nulling due to destructive interference caused by multipath propagation.
7	RX/TX	Receive/Transmit control. Switches between Receive (RX/TX = '1') and Transmit (RX/TX = '0') functions. CMOS compatible with $10k\Omega$ nominal pull up resistor.
8	V _{EE}	-5V output from internal switching regulator, powered by external $+5V$ supply, V _{CC-5} , pin 15.
9	RXD	Received Data output. This low drive current data output is the output from the receiver demodulator. Total load on RXD should be less than 6pF.
10	V _{EE} GND	-5V Ground.
11	RXDGND	Receive Data Ground. See note 1.
12	PAOFF	Transmitter Power Amplifier Control. PAOFF is used to turn the transmitter power amplifier on and off, in conjunction with RX/TX.
13	INTERLOCK	Connected to ground and can be used to indicate that the DE6003 is connected. See note 2.
14,16,18,20	GND	+5V Ground. Internally connected to all other grounds 1, 10, 11,19, 23 and 33.
15	V _{CC-5}	Positive supply input for internal $-5VV_{EE}$ generator.
17	Test	Open circuit for normal mode, high for test mode. For factory use only.
19	GND-5	Ground for -5V regulator. Internally connected to all ground pins 1,10,11,14,16,18, 20, 23 and 33.
21,22,24, 26,27	NC	No Connection. These pins are not used, but no connection should be made to them as GPS re- serves the right to use them for future expansion.
23	CLKSHLD	System Clock Ground. See note 1.
25	CLK	System Clock. This synthesiser clock output at 10MHz is also made available during standby as well as being available during normal operation (it is not a recovered data clock). This output is a constant current sink/source which must be terminated such as to keep its voltage swing low. See note 2.
28	SYNLOK	Synthesiser Lock Monitor. Should only be used to indicate PLL failure. Lock (SYNLOK = '0') is defined as all three PLLs in lock. Unlock (SYNLOK = '1') is defined as an Error Condition. Note that when switching channels unlock may occur for short periods while locking on new channel.
29	TXD	Transmitter Data Input. CMOS compatible with no pull up/pull down resistor.
30	STDBY	Standby . When low, disables radio function, placing all ICs into a low current mode; however, the 10MHz clock and the $-5V$ regulator continue to run in Standby mode, providing a clock and $-5V$ output on the 40-way connector. CMOS compatible with $30k\Omega$ nominal pull down resistor.
31	RSSI	Receive Signal Strength Indicator. Received in-band signal level monitor. The analog RSSI output increases monotonically from 0V to +3V proportional to the logarithm of the input signal power. Source impedance is $10k\Omega$.
32 34 35 37 39 36 38	SD0 SD1 SD2 SD3 SD4 SD5 SD6	Channel Select Code, SD6:0. These 7 data lines determine the channel used for both transmit and receive. They are latched on the falling edge of LOADB and implemented on the rising edge of LOADB. and are CMOS compatible with $30k\Omega$ nominal pull down resistors. SeeTables 3 and 4.
33	RSSIGND	Received Signal Strength Indicator Ground. Internally connected to all ground pins 1, 10,14,16,18,19,20 and 23.
40	LOADB	Channel Select Load Pulse. This active low pulse loads SD (6:0) code into a data latch to set the required channel. CMOS compatible with $30k\Omega$ nominal pull up resistor. See Tables 3 and 4.

NOTES. 1. All ground pins (1, 10, 11, 14, 16, 18, 19, 20, 23 and 33) are internally connected. 2. See AN142, Designing with the DE6003, for further information.

Channel	Channel select code (SD0 = LSB)	Frequency (GHz)
0	0000000	2.400
1	0000001	2.401
2	0000010	2.402
3	0000011	2.403
		l
98	1100010	2.498
99	1100011	2.499
100	1100100	2.500

Table 3 Channel allocation

lllegal channel	Illegal channel select code	Default frequency (GHz)	Default channel	
101	1100101	2.500	100	
102	1100110	2.500	100	
103	1100111	2.500	100	
104	1101000	2.444	44	
105	1101001	2.445	45	
106	1101010	2.446	46	
107	1101011	2.447	47	
108	1101100	2.444	44	
109	1101101	2.444	44	
110	1101110	2.446	46	
111	1101111	2.446	46	
112	1110000	2.444	44	
113	1110001	2.445	45	
114	1110010	2.446	46	
115	1110011	2.447	47	
116	1110100	2.444	44	
117	1110101	2.444	44	
118	1110110	2.446	46	
119	1110111	2.446	46	
120	1111000	2.444	44	
121	1111001	2.445	45	
122	1111010	2.446	46	
123	1111011	2.447	47	
124	1111100	2.444	44	
125	1111101	2.444	44	
126	1111110	2.446	46	
127	1111111	2.446	46	

Table 4

Illegal Channel Allocation

In order to keep transmissions to within the 2.4 to 2.5GHz frequency band, channels 101 and above will default to the channels within this band as listed in Table 4.

Note that the channels used are dependent on the frequency allocation in the country of use and the drive circuit/control logic must limit the selected channels to within these frequency limits.

Antenna Ports

Two antenna ports are available (ANT1 and ANT2) for receiver diversity and are selected by ANTSEL (pin 5 on the 40-way connector). These ports have 50Ω nominal impedance. The port isolation is specified in Table 1.

TRANSCEIVER CHARACTERISTICS

General Electrical Performance

DC power supply requirements

The V_{CC} (+5V) power supply needs to be well regulated, low noise (less than 20mVp-p ripple and noise) and have a source impedance of less than 50m Ω at 1kHz. The V_{CC} supply has been separated from the input (V_{CC-5}) to the -5V (V_{EE}) generator to provide greater flexibility in the overall system design.

Extra care should be taken with ripple and noise suppression of the V_{CC} supply if the V_{CC-5} supply is connected to the radio's main V_{CC} supply. If supplied separately, ripple and noise on the V_{CC-5} supply should be less than 100mVp-p at 1kHz.

NOTE: Ripple and noise on the +5V power supply (V_{CC}) modulates the transmitter output and levels above those specified will result in increased spurious output from the DE6003, and will also cause degradation in receiver sensitivity.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V _{CC}	0V to +6V
Supply voltage to V_{EE} generator, V_{CC-5}	0V to +6V
Input voltage	-0.3 to V _{CC} $+0.3$
Operating temperature	0°C to +55°C
Storage temperature	-20°C to +70°C
Transmitter duty cycle	See Fig. 2
Maximum RF input	30dBm

Stresses above those listed may cause permanent damage to the transceiver. These are stress ratings only and functional operation of the transceiver at those conditions, or at any other condition above those indicated in the operation section of this data sheet is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

NOTE: The V_{CC-5} supply must be applied not less than 10ms before the V_{CC} supply. Failure to observe this requirement could result in premature failure of the transceiver.

Parameter	V _{cc}	= 5V, +2	5°C	V _{CC} = 5·25V, 0°C to +55°C	Units		
Farameter	Min.	Тур.	Max.	ax. Max 30 1			
V_{CC-5} supply current at 3V	-	-	-	30	mA		
V_{CC-5} supply current at 5V	-	-	-	18	mA		
V _{CC-5} supply current at 6V	-	-	-	15	mA		
V _{CC} supply current standby	8	14	20	30	mA		
V _{CC} supply current receive	80	120	140	150	mA		
V_{CC} supply current transmit	200	330	384	400	mA		

NOTES

1. Currents shown are for the transceiver only.

Peak input current requirements are>100mA as the 100µF capacitor has to be charged

3. V_{EE} may be supplied from an external source, in which case V_{CC-5} should not be connected. See AN142 for further information.

Table 5 Supply currents

Environmental Limiting Conditions of Use

- Operational Temperature: 0°C to +55°C.
- Storage Temperature -20°C to +70°C.
- Humidity: 95% non-condensing.
- ESD: Human body model, 4000V.
- Vibration Testing: 10 t0 2000Hz, displacement ±1mm, acceleration 2G.

Operating temperature

When in operation the transmitter power amplifier (PA) dissipates the highest amount of power and creates the highest temperature. In order to keep the temperatures to a safe level the environment in which the radio is operated must be kept within the values specified in Environmental Limiting Conditions of Use, above.

The radio dissipates this heat from the whole of its surface, in particular from the metallic screen; steps must be taken to prevent overheating as early failure of the radio may occur. Depending on the air temperature surrounding the radio, the PA duty cycle must be set to keep the dissipation to a safe value.

The transmitter power amplifier derating curve of Fig.2 shows the derating factors that should be applied in order not to exceed the maximum working temperature. Running at the maximum permitted temperature on the PA will (as with all semiconductor devices) result in shorter operational life than running at lower temperatures. The thermal time constant of the radio is 1 minute and this derating curve can only be applied to transmitter for continuous transmit times of less than 20 seconds; above this time the duty cycle should be considered 100%. For continuous operation the case temperature should not exceed 40°C.

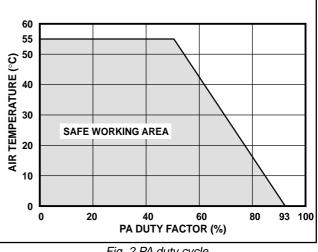


Fig. 2 PA duty cycle

TIMING SPECIFICATIONS AND CONDITIONS OF USE

The timing diagrams, Figs. 3 to 8, show some of the normal sequences used in the control of the DE6003 and are used to illustrate timing relationships. Table 6 is the truth table for these signals values for which are given in Table 7. Each entry in Table 7 is described on pages 9 and 10.

STDBY	RX/TX	PAOFF	PWRLO	ANTSEL	SD (6:0)	LOADB	State
L	х	Х	Х	Х	Х	Х	Standby
н	н	L	L	L	0000000		Receive, ANT 1, low power, PA off, setting Channel 0
Н	Н	L	L	Н	0001000		Receive, ANT 2, low power, PA off, setting Channel 8
Н	Н	L	Н	L	0010000		Receive, ANT 1, high power, PA off, setting Channel 16
н	Н	L	н	н	Х	н	Receive, ANT 2, high power, PA off
н	L	L	L	L	Х	н	TX ready, ANT 1, low power, PA off
Н	L	Н	L	L	Х	Н	Transmit, ANT 1, low power, PA on
Н	L	Н	Н	L	Х	н	Transmit, ANT 1, high power, PA on

Table 6 Control signals truth table

DYNAMIC CHARACTERISTICS

These Characteristics are guaranteed over the following range of operating conditions and apply to both the DE6003-001 and DE6003-002 unless otherwise stated:

 $T_{AMB} = 25^{\circ}C$, $V_{CC} = 5V \pm 5\%$, $V_{CC-5} = +3V$ to +6V, data rate = 625kb/s. Refer to Figs. 3 through 8 and Notes on pages 9 and 10.

Characteristic	Symbol	V _{CC} = +5V at 25°C			V _{CC} = 5\ 0°C to	/±5% at <u>55°C</u>	Units	Note
	-	Min.	Тур.	Max.	Min.	Max.		
DE6003-001 output power (high) See note (i)		15.5	18	20	-	-	dBm	1
DE6003-002 output power (high) See note (i)		15.5	18	22			dBm	1
Output power (high) ripple		0	1	3	-	-	dB	1
Output power (low)		6.5	12	16		-	dBm	1
Output power (low) ripple		0	1	3	-	-	dB	1
Power amplifier rise time to 90% full power	t ₁	-	-	4	-	4	μs	2
Power amplifier fall time to 10% full power	t ₂	-	-	4	-	10	μs	2
Maximum continuous transmit time		-	-	-	-	20	ms	3
Minimum time between consecutive transmissions		-	-	-	80	-	μs	3
Transmitter delay		-	-	-	-	800	ns	4
RX/TX to PA on	t ₆	-	-	-	1	-	μs	5
Receive mode to valid transmit data	t ₇	-	5.7	-	-	-	μs	5
TX/RX frequency agility	t ₁₀	-	80	95	-	110	μs	9
Modulated transmitter bandwidth for –20dBc. See note (i)		-	-	-	-	1	MHz	6
Transmitter out of band spurious emissions. See note (i)	Testeo	to con	form to	the reg	ulatory li	mits (se	i e page	7)
Transmitter out of band spurious emissions, Chan. 84. See note (i)		-	-	-30	-	-	dBc	
Transmitter in band spurious emissions		-	-50	-40	-	-40	dBc	31
Power off to transmit		-	-	-	-	10	ms	7
Standby to transmit		-	-	-	-	1	ms	8
LOADB pulse data setup time	t ₁₃	0	-	-	0	-	ns	10
LOADB pulse width	t ₁₄	1	-	-	1	-	μs	10
LOADB pulse data hold time	t ₁₅	-	-	-	10	-	ns	10
Receiver sensitivity for BER ≤1×10 ⁻⁵		-	-81	-77	-	-77	dBm	11
Receiver sensitivity for BER $\leq 1 \times 10^{-5}$, Chan. 84. See note (i)		-	-	-77	-	-	dBm	11
Max. input signal for BER ≤1×10 ⁻⁵		-	-	-	-15	-	dBm	12
Bit period of received data, pseudo random (single bit)	t ₁₆	1.35	1.6	1.85	-	-	μs	13
Bit period of received data (unbalanced)	t ₁₆	-	1.6	-	1.20	2.0	μs	13
Received data delay	t ₁₈	-	-	-	-	3.5	μs	14
Frequency hop time to valid received data	t ₁₉	-	80	95	-	110	μs	15
Transmit mode to receive data valid	t ₂₀	-	18	24	6	30	μs	16
RF burst response to valid data	t ₂₁	-	18	24	-	-	μs	17
RF burst response to valid data	t ₂₁	-	-	-	-	30	μs	17
Time to valid data after antenna selection	t ₂₂	-	18	-	6	30	μs	18
Receiver selectivity $f_0 = \pm 1.5 MHz$ (unmodulated)		60	-	-	-	-	dB	20
Receiver selectivity $f_0 = \pm 2MHz$ (modulated)		25	35		20	-	dB	19
Receiver selectivity $f_0 = \pm 3$ MHz (modulated)		31	41	-	30	-	dB	19
Receiver selectivity $f_0 = \pm 10$ MHz (modulated)		40	47	-	40	-	dB	19
Receiver spurious rejection performance <1.8GHz		-	-	-	-50	-	dBc	21
RSSI output at -80dBm. See note (i)		0.8	1.4	2.0	0.7	2.5	V	22
RSSI output at -38dBm		2.2	2.8	3.3	2.0	3.3	V	22

NOTE (i) Additionally measured on Channel 84 for RCR STD-33

Cont...

DYNAMIC CHARACTERISTICS (Continued)

Characteristic		V _{CC} = +5V at 25°C			V _{CC} = 5V±5% at 0°C to 55°C			Note
		Min.	Тур.	Max.	Min.	Max.		
RSSI delay time	-	-	-	-	-	4.5	μs	23
Frequency hop time to valid RSSI	t ₂₃	-	50	70	-	-	μs	24
Frequency hop time to valid RSSI	t ₂₃	-	-	-	-	80	μs	24
Transmit mode to receive valid RSSI	t ₂₄	-	4	5	-	-	μs	25
Transmit mode to receive valid RSSI	t ₂₄	-	-	-	-	6	μs	25
Time to valid RSSI after antenna selection	t ₂₆	-	-	-	-	5	μs	26
Receiver conducted emissions ≤1GHz	-	-	-77	-57	-	-57	dBm	27
Receiver conducted emissions ≤1GHz, Chan. 84. See note (i)	-	-	-	-57	-	-	dBm	27
Receiver conducted emissions ≥1GHz	-	-	-56	-47	-	-47	dBm	27
Power off to receive valid data/RSSI	t ₂₇	-	-	-	-	10	ms	28
Standby to receive valid data/RSSI	t ₂₈	-	-	-	-	1	ms	29
Frequency stability	-	-	-	-	-	±20	ppm	30

Table 7 (Continued)

UNWANTED EMISSIONS

The DE6003 has been characterised to meet the RCR STD-33, ETSI ETS 300-328 and FCC15.247 regulatory limits when used correctly and during test the production units are checked for conformity. When the radio is required to comply with FCC 15-247 regulations, the protocol must permit the radio to transmit any one channel for a total time not exceeding 20ms in any 100ms period. For correct use a suitable protocol, timing and timing sequences must be used as indicated in application note AN142.

The antennas used will also determine if conformity to the above regulations is possible; effects of both gain and harmonic response must be considered. Substitution by the end user of alternative antennas to those supplied with the equipment should not be possible if FCC regulations are to be complied with.

The 2-4GHz ISM band is allocated such that there are

strict limits on the amount of radiation allowed outside, but adjacent to, the band. Because the modulated signal is not infinitely small, certain constraints exist in the proximity of the operating channel to the edge of the allocated band.

For maximum network throughput, it advisable to arrange that stations do not attempt to use adjacent channels, but to use channels separated by at least 2MHz from any other channel that is in use.

NOTE: To comply with the regulations, it is recommended that the following channels are used, allowing 'guard bands' at each end of the usable frequency allocation:

ETSI and FCC: Channels 01 to 82 (2402 to 2482MHz); RCR: Channels 72 to 95 (2473 to 2495MHz).

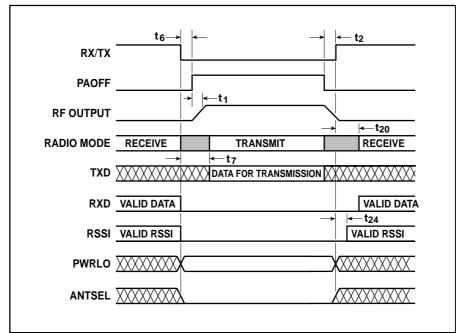


Fig. 3 Timing control diagram

DE6003

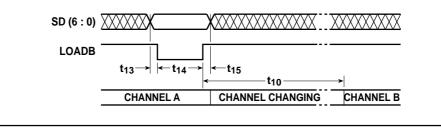


Fig. 4 Channel strobe timing diagram

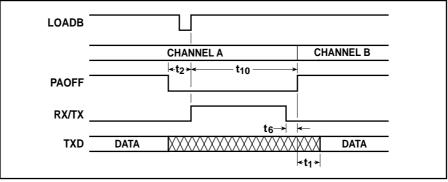


Fig. 5 Transmit-channel hop-transmit timing diagram RX/TX = 0)

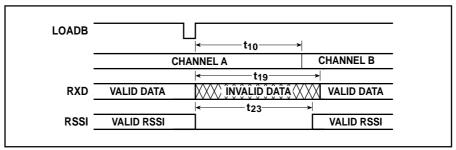


Fig. 6 Receive-channel hop-receive timing diagram (RX/TX = 1)

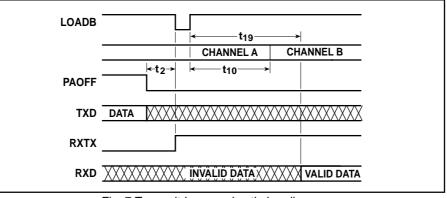


Fig. 7 Transmit-hop-receive timing diagram

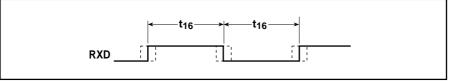


Fig. 8 Bit period of received data

Dynamic Characteristics – Notes to Table 7

1. Transmitter Power Output

Selectable by control line, to high or low output power setting. Power levels are for any channel into 50Ω and measured at ANT1. Output ripple is measured over 5 channels.

2. Transmitter Power Amplifier Control, PAOFF

 $(t_1, t_2 \text{ and } t_6 - \text{ see Fig. 3})$

This control is used in conjunction with the RX/TX. PAOFF is included to allow the power amplifier to be turned on after RX/TX has been set low to transmit (t_6 , rising to 90% in t_1) and off before being set high to receive (t_2). The power amplifier has been designed to switch on and off in this controlled way to avoid generating unwanted emissions which would be caused by simply turning the transmit power on and off.

3. Transmit Times

When in transmit mode, the transmit (700 MHz) PLL is opened, preventing the PLL tracking the low frequency components of the transmitted data. This puts a limit on the maximum length of the data block which can be transmitted and places a requirement of a delay between switching to receive mode and transmit mode, in order for the PLL to gain lock.

4. Transmit Delay

This is the time to convert the TXD data to the specified frequency (FSK) for transmission. It is specified as the delay from the 50% point of TXD to the output frequency reaching 50% of its deviation.

5. Receive Mode to Valid Transmit Data (t₇ – see Fig. 3) This is the cumulative minimum time taken to:
a. switch from receive to transmit mode, b. Transmit to PA on delay (RX/TX to PA switch-on delay that must be allowed between switching from receive to transmit and turning on the PA in order for sufficient energy to be built up in the transmit chain before the PA is switched on),
c. Switch on PA and d. Transmit delay

6. Transmitter Modulation (Data onto Carrier)

Spectrally shaped Continuous Phase Frequency Shift Keying, spectrum-compliant with FCC 15.247. The DE6003 uses Spread Spectrum communication employing Frequency Hopping with spectrally shaped CPFSK as the modulation format. Spectral shaping is achieved with a Gaussian approximation pre-modulation filter. 90% of the power is within 1MHz bandwidth.

7. Power On to Transmit Time

This is the time from V_{CC} being applied to the start of transmission of valid data at the antenna port. This value is very dependent on the power supply used, as all the decoupling capacitors on the DE6003 have to be charged and this energy must be supplied by the power supply.

8. Standby to Transmit (t₉)

This is the time from standby to the start of transmission of valid data at the antenna port.

Transmitter/Receiver Frequency Agility (t₁₀ – see Figs. 4,5,6 and 7)

The DE6003 is designed to be used in a Frequency Hopping Spread Spectrum Radio System. This requires fast channel switching, which is defined as the time taken from the rising edge of LOADB to the required channel being within 40kHz of the frequency required. The operating channel should not be switched until the output power has fallen to less than 10% after the power amplifier has been switched off when in transmit mode.

10.Transmit/Receive Frequency Select (t₁₃, t₁₄ and t₁₅ – see Fig. 4)

The DE6003 transceiver will operate over 101 channels spaced at 1MHz intervals within the frequency band 2.400 to 2.500GHz. This is selected by setting SD (6:0) to the desired channel number and strobing in the data by pulsing LOADB low. When LOADB is low data ripples through a transparent latch, and is loaded into synthesiser data hold register on the rising edge of LOADB.

11.Receiver Sensitivity

A modulated signal of amplitude greater than or equal to the value specified in Table 7 injected at either antenna port will exhibit a Bit Error Rate of no more than 10⁻⁵ at 625 kb/s. GPS measure this by applying a signal modulated with a pseudo random DATA stream (2¹⁵–1)and modulated with an Anritsu MD6420A Transmission analyser, together with a Marconi Instruments 2031 signal source for TXD and a signal shaping filter with the characteristics of the DE6003 transmitter filter. The receive data clock used is the transmit data clock delayed by 400ns to enable centre-bit sampling (optimum sampling).

12.Receiver Max. Input Signal

This is defined for all channels as the maximum receiver input signal level for a 10^{-5} bit error rate.

13. Receiver Data Bit Period (t₁₆ – see Fig. 8)

Data bit period (t_{16}) is the nominal time between each successive data bit. This period is subject to jitter on receive and will be continually changing within the bit period specification.

The DE6003 is configured for 625 kb/s and data run length of contiguous '0's or '1's limited to 16 or less; any deviation from this may result in a lowering of sensitivity. The received RXD data stream will meet the bit width restrictions for '1's and '0's as defined in Table 7. This is referenced to the nominal centre of a bit period. Two bit width measurements are used to determine the correct operation of the demodulation circuitry, the first for pseudorandom data and the second to measure the effects of continuous patterns of 16 '1's followed by a single '0' and of 16 '0's followed by a single '1'.

NOTE: Received data (RXD) is considered valid when these specifications have been met.

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14.Receive Delay (t₁₈)

As measured for 50% of the change of input frequency deviation at either antenna port to the output on the RXD pin (9) of the 40 way connector.

15.Frequency Hop Time to Valid Received Data (t₁₉see Figs. 6 and 7)

This is specified as the time from the rising edge of LOADB to data being within the bit period specification. (see note 13).

16.Transmit to Valid Received Data (t_{20} – see Fig. 3)

Transmit to valid received data (t_{20}) is specified as the time from the rising edge of RX/TX (this assumes that the PA has been instructed to turn off (PAOFF low) and PA fall time allowed to elapse before the rising edge of RX/TX) to data being within the edge jitter requirements.

17.RF Burst to Valid Data (t₂₁)

RF burst to valid data (t_{21}) is specified as the time from the start of a valid RF burst of data to valid data at RXD being within the bit period specification.

18. Time to Valid Data after Antenna Selection (t₂₂)

Time to valid data after antenna selection (t_{22}) is specified as the time from the change of ANTSEL line to data being within the bit period specification.

19.Channel Rejection (Modulated)

The receiver selectivity is the ratio of the interfering signal to wanted signal power levels at which the Bit Error Rate on the wanted signal is degraded to 10^{-5} . The wanted signal is applied at 10dB above the measured sensitivity level using a PRBS data pattern. The interferer is modulated by a different PRBS data pattern with the same deviation as the wanted signal. The interferer is then increased in level until the BER as measured on the wanted channel degrades to 10^{-5} .

This is the rejection to unwanted signals and is measured at $\pm 2,~\pm 3$ and ± 10 MHz from the selected channel.

20.Channel Selectivity (Unmodulated)

Minimum rejection of signals at a frequency offset of \pm 1.5MHz from the wanted signal, as defined in Table 7.

21. Receiver Spurious Rejection

Minimum rejection of signals in the bands below 1.8GHz and above 3.3GHz. All spurious responses better than the value defined in Table 7.

22. Receive Signal Strength Indicator (RSSI)

The RSSI output should be used for relative measurement purposes only. The output, which is a measure of the second IF energy level, is neither calibrated for a given input signal strength nor to take account of production tolerance variation of the receiver's gain and losses. Typical RSSI response is shown in Fig. 9.

23.RSSI Delay

This is measured for 50% changed input amplitude at either antenna port to the time at which the RSSI output (pin 31 on the 40-way connector) is within 10% of its final value.

24. Frequency Hop Time to Valid RSSI (t_{23} – see Fig. 6)

This is specified as the delay from the rising edge of

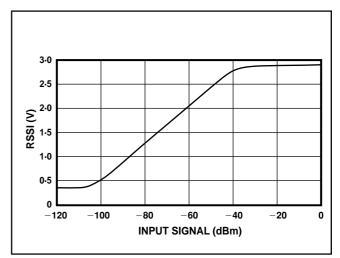


Fig. 9 Typical RSSI response

LOADB to valid RSSI, when the RSSI output is within 10% of its final value.

25. Transmit Mode to Receive Valid RSSI

(t₂₄ - see Fig. 3)

This is specified as the delay from the rising edge of RX/TX to valid RSSI, when the RSSI output is within 10% of its final value.

26.Time to Valid RSSI after Antenna Selection (t₂₆)

Time to valid RSSI after antenna selection $(t_{26})\mbox{is}$ specified as the time from the change of ANTSEL line to the time at which the RSSI output is within 10% of its final value.

27.Receiver Conducted Emissions

These are specified as the emissions measured, at either antenna port (terminated with 50Ω), with the transceiver in receive mode.

28. Power Off to Receive Valid Data/RSSI (t27)

This is the time from V_{CC} being applied to the reception of valid data being within the edge jitter requirements and when RSSI output is within 10% of its final value. These timing values are very dependent on the power supply used, as all the decoupling capacitors on the DE6003 have to be charged and this energy must be supplied by the power supply.

29.Standby to Receive Valid Data/RSSI (t28)

This is the time from STANDBY going high to the reception of valid data being within the edge jitter requirements to the time at which the RSSI output is within 10% of its final value.

30.Frequency Stability

In order to be able to demodulate data in all specified environmental conditions the 10MHz reference oscillator frequency stability is as specified in Table 7.

31. Transmitter In Band Spurious Emissions

These are emissions in the transmitter output which are in the frequency range of 2.4 to 2.5GHz.

MECHANICAL INFORMATION

Outline Drawing

Please note that outline drawing M50633 A2 with toleranced dimensions is available on request.

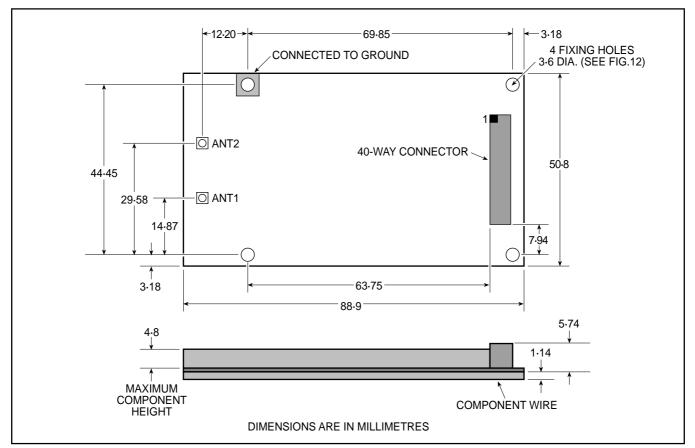


Fig. 10 DE6003 outline drawing

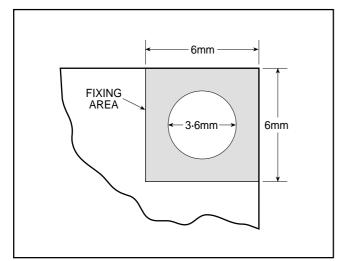


Fig. 11 Permissible fixing area for all 4 holes

40-Way Connector

The 40-way connector on the DE6003 board is:

AMP: AMPMODU 50/50 grid, Part Number 104655-5 The mating receptacle connector is:

AMP: AMPMODU 50/50 grid, Part Number 104652-4

The combined mated height of the connector pair is 0.250in (6.35mm).

Antenna Connectors

For the interface of each antenna, the connector is: RADIALL-TRANSRADIO, MMS Series surface mount coaxial connector, Part Number R209 406.

The mating connector and cable assembly is: RADIALL-TRANSRADIO, Part Number A209 080 500 XXX (XXX = the length in mm of the cable)

or 3M ELECTRONIC PRODUCTS DIVISION, Part Number 980028-017-XXX (XXX = the length of the cable in inches).

The antenna ports are designed for 50Ω impedance. It is advisable to terminate an unused antenna port with a 50Ω load, should only one antenna be used.

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