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## Short Information

### DDP 3310B

#### Display and Deflection Processor (68-Pin PLCC Package)

The DDP 3310B is a single-chip digital display and deflection processor, designed for high-quality back-end applications in 100/120Hz TV sets with 4:3 or 16:9 picture tubes. It can be combined with members of the DIGIT 3000 IC family (VPC 32xxA, CIP 3250A, TPU 3040) or it can be used with third party products. The IC contains the entire digital video component and deflection processing and all analog interface components. The main features are

#### Video processing

- digital input  $YC_rC_b$  (4:2:2 or 4:1:1)
- horizontal scaling (0.25 ... 4)
- panorama vision
- dynamic peaking
- soft limiter (gamma correction)
- color transient improvement
- programmable RGB matrix
- picture frame generator
- 3 x D/A converters
- two analog RGB/fastblank inputs

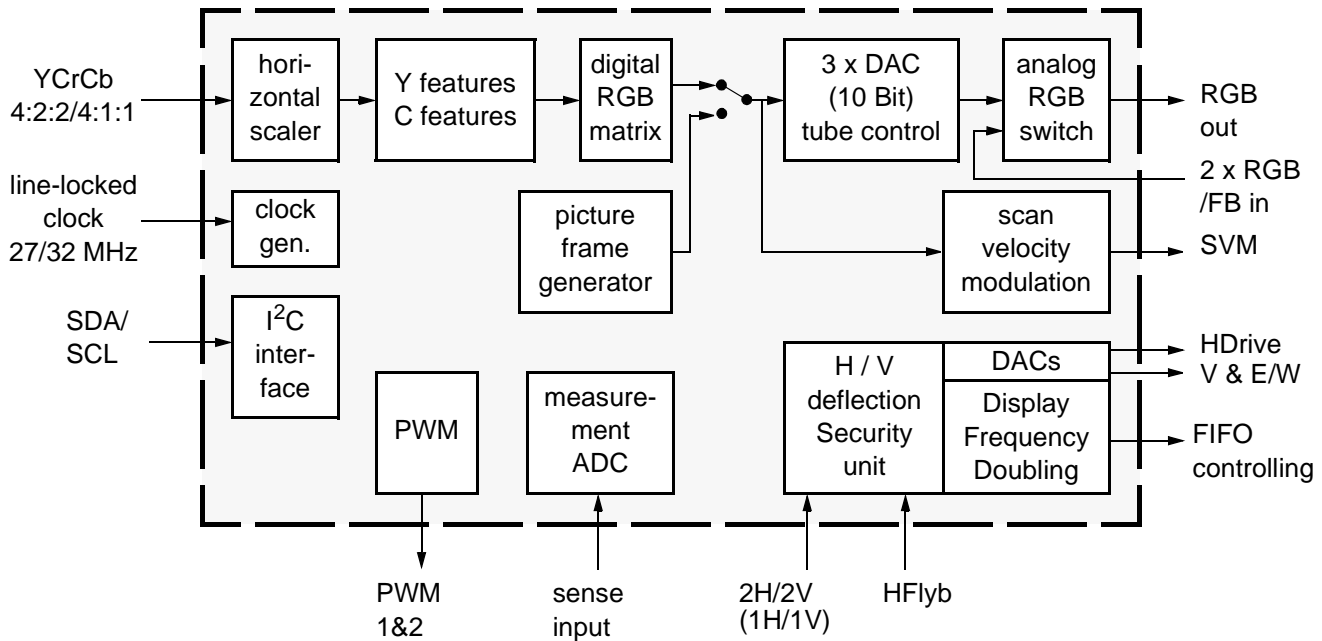
#### Miscellaneous

- clock input selectable for 27/32 MHz line-locked clock
- crystal oscillator for horizontal safety
- automatic picture tube adjustment (cutoff, whitedrive)
- separate ADC for tube measurements
- single 5 V power supply
- hardware for simple 50/60 Hz to 100/120 Hz conversion (display frequency doubling)
- two I<sup>2</sup>C controlled PWM outputs

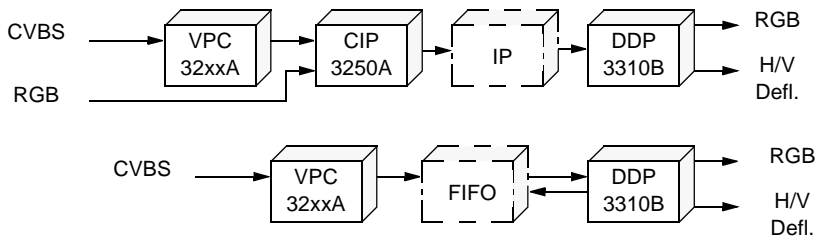
#### Deflection processing

- scan velocity modulation output
- high performance H/V deflection
- EHT compensation for vertical / east-west
- soft start/stop of H-drive
- vertical angle and bow
- differential vertical output
- vertical zoom via deflection
- horizontal and vertical protection circuit
- adjustable horizontal frequency for VGA/SVGA display

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**Fig. 1:** Block diagram of the DDP 3310B



**Fig. 2:** DDP 3310B applications

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Edition: Nov. 3, 1997  
 Order No. 6251-464-1SI