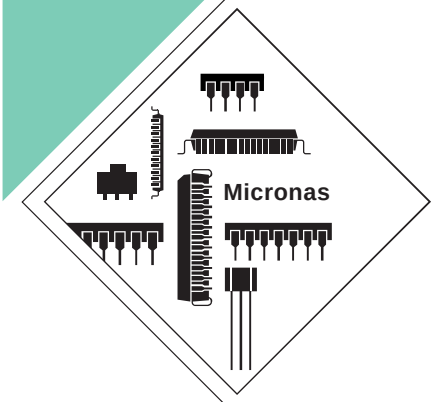

APPLICATION NOTE IC

DDP 3310B
Displaying VGA Signals with VPC 32xxA/C/D

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6251-464-2AN

MICRONAS

Contents

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1. Application Circuit

In 100-Hz TV applications, a VGA signal can be displayed. In this case, a VGA graphics card delivers the H, V, and RGB signals. These signals can be fed “directly” into the back-end signal processing. The VPC can generate a stable line-locked clock for the 100-Hz system in relation to the VGA sync signals. While the V-sync is connected to the VGAV pin directly, the H-sync has to be pulse-shaped and amplitude-adjusted until it is connected to one of the video input pins of the VPC. The recommended circuitry to filter the H sync is given in the figure below.

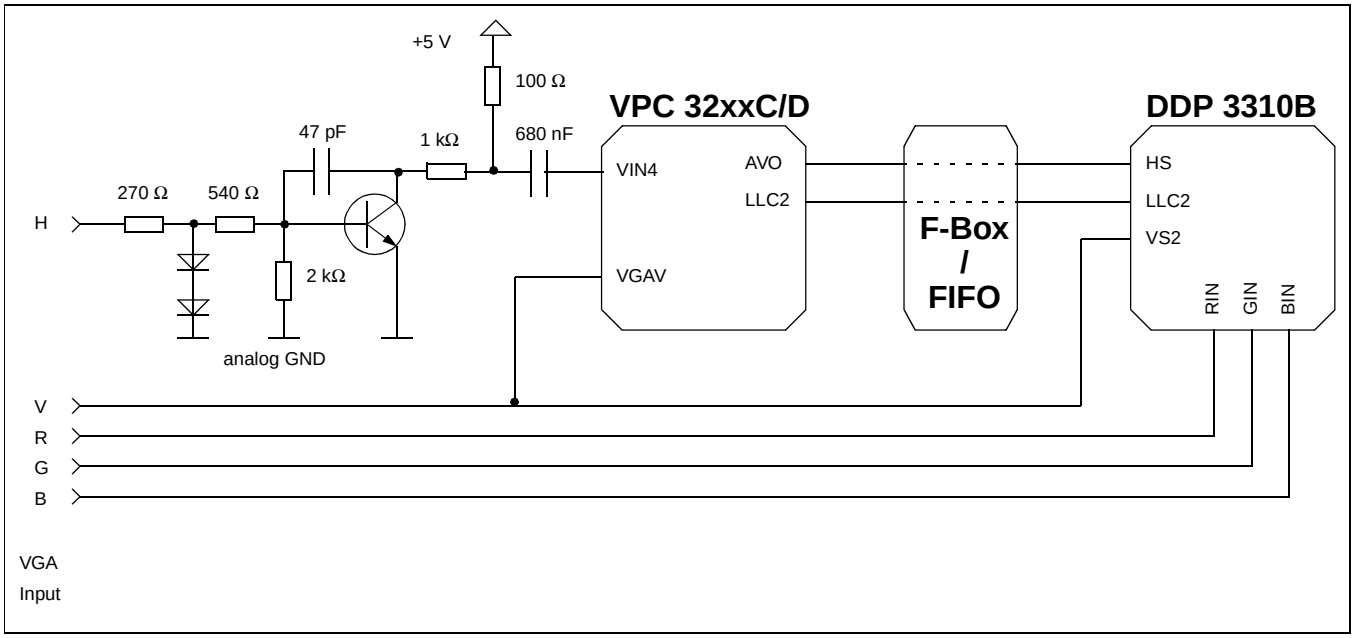

Fig. 1–1: Application circuit: VGA signal processing by means of VPC 32xxC/D and DDP 3310B

1.1. Brief Description for Setting Up the VGA Mode

1. Setup the VGA mode (VGA=1) in the VPC and select the corresponding horizontal frequency (f_{VGA} = 31.5, 35.2, 37.9 kHz) with VGAMODE.
2. Adjust the line-locked clock back-end of the VPC to the selected horizontal frequency, by changing:

   – $LINLEN = \frac{2 \times LLC_{MHz}}{f_{VGA}}$

   – Start / Stop values of AVO and HC must be adapted to the new LINLEN and the actual horizontal phase of the VGA Hsync signal. (The VPC locks to the rising edge of H, so the sync polarity changes the horizontal phase of AVO and HC). Both signals have half the horizontal frequency of the VGA Hsync signal!
3. With the connected VGA Vsync signal the VPC counts the number of lines per field. The register NLPF displays half the number of lines per field!
4. Adjust the back-end DDP to the correct horizontal frequency (HFREQ) and number of lines (LPFD).

2. Table of Supported VGA/SVGA Standards

Table 2–1: Table of VGA modes sorted by horizontal frequency

Resolution	Name	Pixel per Line	Lines per Field	Horizontal Frequency (kHz)	Vertical Frequency (Hz)
720 x 350	DOS 70 Hz	900	449	31.4	70
720 x 350	DOS 60 Hz	900	525	31.4	60
720 x 350	DOS 50 Hz	900	629	31.4	50
640 x 480	VGA3 60 Hz	800	525	31.4	60
640 x 480	VGA 50 Hz	800	629	31.4	50
800 x 600	VESA 1 56 Hz	1024	625	35.1	56
800 x 600	OAK800 56 Hz	1024	626	35.1	56
800 x 600	TSENG800 56 Hz	1016	634	35.4	56
640 x 480	VESA Standard 75 Hz	840	500	37.5	75
640 x 480	VESA 2 72 Hz	832	520	37.8	72.8
720 x 400	VESA? 84 Hz	954	449	37.7	84
800 x 600	VESA 5 60 Hz	1056	628	37.8	60

VGA Mode 0: VGA Mode 1: VGA Mode 3: VGA Mode 3:

Table 2–2: Table of VGA modes sorted by lines per field

Resolution	Name	Pixel per Line	Lines per Field	Horizontal Frequency (kHz)	Vertical Frequency (Hz)
720 x 350	DOS 70Hz	900	449	31.4	70
720 x 400	VESA? 84Hz	954	449	37.7	84
640 x 480	VESA Standard 75Hz	840	500	37.5	75
640 x 480	VESA 2 72Hz	832	520	37.8	72.8
720 x 350	DOS 60Hz	900	525	31.4	60
640 x 480	VGA3 60Hz	800	525	31.4	60
800 x 600	VESA 1 56Hz	1024	625	35.1	56
800 x 600	OAK800 56Hz	1024	626	35.1	56
800 x 600	VESA 5 60Hz	1056	628	37.8	60
720 x 350	DOS 50Hz	900	629	31.4	50
640 x 480	VGA 50Hz	800	629	31.4	50
800 x 600	TSENG800 56Hz	1016	634	35.4	56

VGA Mode 0: VGA Mode 1: VGA Mode 3: VGA Mode 3:

3. VPC 32xxA/C/D Register Settings

Table 3–1: Line locked clock specific settings

VGA Mode	Register Name	Address (hexadecimal)	Bit Slice	Value LLC1=13.5 MHz	Value LLC1=16 MHz
0 ... 3	LLC_CLOCKH	69 (FP)	11:0	42	4062
	LLC_CLOCKL	6A (FP)	11:0	2731	3336
	LLC_DFLIMIT	61 (FP)	11:0	54	48
	LLC_CLKC	6D (FP)	5:0	5	3

Table 3–2: General settings

VGA Mode	Register Name	Address (hexadecimal)	Bit Slice	Value LLC1=13.5 MHz	Value LLC1=16 MHz
0 ... 3	VIS for VPC 32xxC/D	21 (FP)	1:0	3	3
	VIS for VPC 321xA	21 (FP)	1:0	0	0
	VGA_EN[1)]	2F (FP)	10	1	1

[1)] Note: Register is available only in VPC 32xxC/D

Table 3–3: Mode specific settings

VGA Mode	Register Name	Address (hexadecimal)	Bit Slice	Value LLC1=13.5 MHz	Value LLC1=16 MHz
0 (31.5kHz ± 2%)	LINLEN	21 (16 I^2C)	10:0	857	1016
	VGAMODE	2F (FP)	1:0	0	0
	AVSTOP [1)]	29 (16 I^2C)	10:0	850	1012
	HCSTOP [1)]	27 (16 I^2C)	10:0	850	1012
1 (35.2kHz ± 2%)	LINLEN	21 (16 I^2C)	10:0	767	911
	VGAMODE	2F (FP)	1:0	1	1
	AVSTOP [1)]	29 (16 I^2C)	10:0	760	900
	HCSTOP [1)]	27 (16 I^2C)	10:0	760	900
2 (37.5kHz ± 2%)	LINLEN	21 (16 I^2C)	10:0	719	851
	VGAMODE	2F (FP)	1:0	2	2
	AVSTOP [1)]	29 (16 I^2C)	10:0	710	840
	HCSTOP [1)]	27 (16 I^2C)	10:0	710	840
3 (37.9kHz ± 2%)	LINLEN	21 (16 I^2C)	10:0	711	843
	VGAMODE	2F (FP)	1:0	2	2
	AVSTOP [1)]	29 (16 I^2C)	10:0	700	832
	HCSTOP [1)]	27 (16 I^2C)	10:0	700	832

[1)] Note: All registers, which refer to the number of pixel per line (LINLEN), must be smaller then LINLEN.

4. DDP 3310B Register settings

The DDP 3310B has the capability to accept different line-locked clock rates: 27 and 32 MHz. This external clock rate is converted internally to a clock rate of 40.5 or 40 MHz by means of a PLL. Selection of external clock frequency is done via pin CM1 and CM0. See Table 4–1 for clock frequency selection.

Table 4–1: Clock frequency selection

CM1	CM0	LLC2
GND	GND	27 MHz
GND	VDD	32 MHz

Table 4–2: General settings

VGA Mode	Register Name	Address (hexadecimal)	Bit Slice	Value LLC2=27 MHz	Value LLC2=32 MHz
0 ... 3	DFDSW	176	5:4	2	
	VSYPOL	176	8	0	
	VSYSRC	176	10	1	
	LPFD	153	9:0	2*NLPF(VPC)	
	VA_MODE	1E8	0	1	

Table 4–3: Mode specific settings

VGA Mode	Register Name	Address (hexadecimal)	Bit Slice	Value LLC2=27 MHz	Value LLC2=32 MHz
0 (31.5kHz ± 2%)	HFREQ	140	7:5	2	
1 (35.2kHz ± 2%)	HFREQ	140	7:5	1	
2 (37.5kHz ± 2%)	HFREQ	140	7:5	5	
3 (37.9kHz ± 2%)	HFREQ	140	7:5	6	

Since the number of pixels per line and lines per field varies in different VGA modes, all related parameters like blanking and picture position have to be adjusted accordingly.

Table 4–4: Horizontal timing registers

Register Name	Address (hexadecimal)	Bit Slice
HBST	1D3	10:0
HBSO	1D4	10:0
PFGHB	1D5	10:0
PFGHE	1D6	10:0
POFS2 [1)]	141	15:1
POFS3 [2)]	144	15:1
MADCLAT	15F	10:0

All registers, which refer to the number of pixel per line, must be smaller then LINLEN (of VPC) times 3/2 (@LLC2=27 MHz) or times 5/4 (@LLC2=32 MHz).

1) Adjustment of POFS2:
The clamping pulse for analog inserted RGB can be adjusted to the pedestal of the input signal with POFS2 or AVSTRT/AVSTOP of VPC.

2) Adjustment of POFS3:
The horizontal raster position of the analog inserted RGB signals can be set to the desired line position with POFS3

Table 4–5: Vertical timing registers

Register Name	Address (hexadecimal)	Bit Slice
VBST	1A4	8:0
VBSO	1A0	8:0
PFGVB	1AC	8:0
PFGVE	1A8	8:0

All registers, which refer to the number of lines between each Vsync, must be smaller then two times NLPF of VPC.

Due to the fact of different horizontal frequencies in different VGA mode all deflection related parameters like picture width and vertical amplitude have to be adjusted depending on your application.

Table 4–6: Vertical geometry registers

Register Name	Address (hexadecimal)	Bit Slice
AMPL	14D	15:8
VPOS	14F	15:8
LIN	150	15:8
SCORR	151	15:8

Table 4–7: Horizontal geometry registers

Register Name	Address (hexadecimal)	Bit Slice
WIDTH	157	15:7
TCORR	158	15:8
CUSH	159	15:8
CRNU	15A	15:8
CRNL	15B	15:8
ANGLE	14A	15:6
BOW	14B	15:6

5. Clamping and Horizontal Phase Adjustment

1. Adjust POFS2 to zero for a good horizontal synchronisation.
2. Adjust POFS3 to zero for the measurement of the clamping phase.
3. Connect an oscilloscope with two probes, one at one of the RGB input signals, the other one at the horizontal flyback input of the DDP.
   The start of the clamping pulse corresponds to the rising edge of the horizontal flyback signal when FLYPOL= 0 and to the falling edge when FLYPOL= 1.
4. adjust the clamping phase with AVSTRT of the VPC when HSYPOL= 0 or with AVSTOP when HSYPOL= 1.
   The duration of the clamping pulse is approx. 1.6 µs. The start should be adjusted at approx. 2 µs after start of the clamping level in the RGB signal.
5. adjust POFS3 for centering the picture. You can use the oscilloscope and move the RGB signal between two flyback pulses. The exact adjustment can be dona at the TV screen.
6. adjust the horizontal blanking HBST and HBSO and finally the E/W parameters.

6. Application Circuit for VPC 321xA

The VPC 321xA generates a stable line-locked clock for the 100-Hz system, only. It is not possible to use the information of NLPF, to identify the number of lines in the VGA signal!
A video input (sync) signal must be delivered to a VPC input to generate a synchronous clock in relation to the VGA sync signals. The original 31-kHz horizontal sync signal of the VGA interface is not suited for the VPC.

To get the VPC 321xA working properly it is necessary to suppress every second horizontal sync. This can be implemented by using the HC output signal of the VPC to gate the VGA sync signal. It is possible to use a simple resistive adder circuit (see figure below). The horizontal sync signal that is produced by VGA graphics is usually not bandlimited. In order to be sampled by the VPC, the H-signal must be bandlimited by a simple RC low-pass filter.

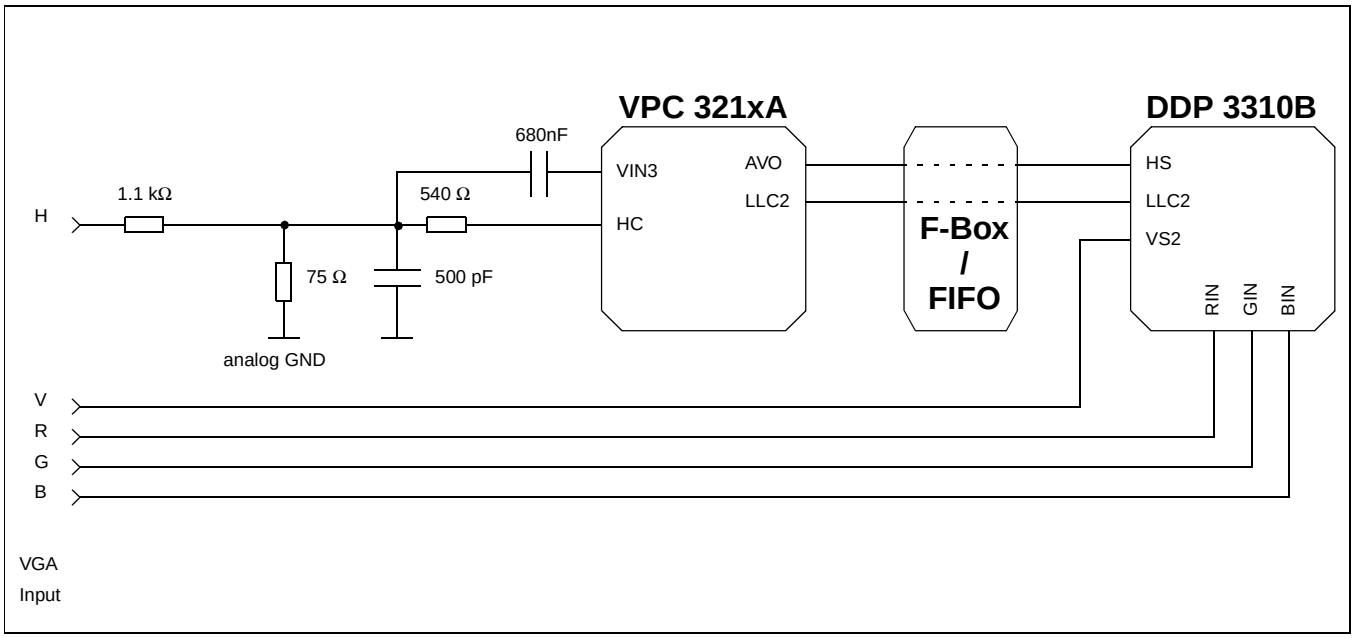

Fig. 6–1: Application circuit: VGA signals processing by means of VPC 321xA and DDP 3310B

7. Application Note History

1. Application Note IC: “DDP 3310B Displaying VGA Signals with VPC 32xxA/C/D, Jan. 11, 2001, 6251-464-2AN. First release of the application note IC.

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