Advance Information Supplement

Subject:	Version Change
Data Sheet Concerned:	DDP 3310B 6251-464-1AI, Edition July 9, 1999
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DDP 3310B-PT-E4 **27.08.99**

The DDP 3310B-PT-E4 is hardware and software compatible to DDP 3310B-PT-D3*. All known problems from Version DDP 3310B-PT-D3* have been solved.

Note: Changes from DDP 3310B-PT-D3* to DDP 3310B-PT-E4:

– In respect to problem No. 32, the recommended workaround No. 1 must be removed for DDP 3310B-PT-E4 to guarantee a working white-drive control loop.

– In respect to problem No. 33, pin 11 (VPROT) must be driven with the correct signal if the vertical protection is enabled (VPROT_DIS = 0).

Problem list for DDP 3310B-PT-E4:

No.	Problem	Description	Comment	Status
16	Crosstalk between SVM signal and analog main picture	Even if the analog SVM output signal is blanked, e.g. when analog RGB is inserted, there is a crosstalk of the SVM signal to the analog RGB output.		reduced by –40 dB
36	Reading PFG color	It is not possible to read the upper 8 bits of register PFC (I^2C-addr. h'11).		

The following table depicts the new features of DDP 3310B-PT-E4 and their related **additional XDFP Registers** or **additional bit slices**:

XDFP Control and Status Registers						
Subaddr.	**Mode**	**Function**			**Default**	**Name**
h'165	16-r/w	bit[14:6]	0..511	analog contrast for external RGB	360	EXT_CONTR
		bit[0]	0 1	beam current limitation reduces ext. RGB BCL does not reduce ext. RGB	0	NOOSDBCL
h'17C	16-r	bit[14:3]	0..4095	minimum beam current (reset every field)	–	BC_MIN
h'17D	16-r	bit[14:3]	0..4095	maximum beam current (reset every field)	–	BC_MAX
h'1EA	16-r/w	bit[0]	0/1	disable/enable soft stop if h-safety protection is active	0	HPROT_SS
h'17A	16-r/w	Fast-Blank interface mode				FBLMODE
		bit[11]	0 1	clamp RGBIN1 to black (if CLAMP =1) clamp RGBIN1 to bias (if CLAMP =1)	0	C1_B
		bit[12]	0 1	clamp RGBIN2 to black (if CLAMP =1) clamp RGBIN2 to bias (if CLAMP =1)	0	C2_B

The following **XDFP Register** has been removed in DDP 3310B-PT-E4:

XDFP Control and Status Registers						
Subaddr.	**Mode**	**Function**			**Default**	**Name**
h'17B	16-r/w	bit [15:4]	–128...127	delay from horizontal flyback to rising edge of HOUT (e.g. negative) in steps of 0.25 µs	0	SEC_POFS

DDP 3310B-PT-D3* 07.05.99

The DDP 3310B-PT-D3* is hardware and software compatible to DDP 3310B-PT-D3. Problem No. 31 has been solved in this version.

DDP 3310B-PT-D3 16.12.98

The DDP 3310B-PT-D3 is hardware and software compatible to DDP 3310B-PT-C2. Problems No. 23, 24, 27, and 30 have been solved in this version.

DDP 3310B-PT-D2 16.12.98

The DDP 3310B-PT-D2 is hardware and software-compatible to DDP 3310B-PT-C2.

DDP 3310B-PT-C2 25.11.98

The DDP 3310B-PT-C2 is hardware, but not software compatible to DDP 3310B-PT-B1.

Problem list for DDP 3310B-PT-C2:

No.	Problem	Description	Comment	Status
16	Crosstalk between SVM signal and analog main picture	Even if the analog SVM output signal is blanked, e.g. when analog RGB is inserted, there is a crosstalk of the SVM signal to the analog RGB output.	Workaround: Set SVG to zero if analog RGB is inserted.	Improved in E4
23	White-Drive measurement lines in FIFO-Application	Not all measurement lines for white-drive RGB appear in a correct order. Sometimes the measurement-line for white-drive blue is not available.		OK in D2
24	Center Brightness	The center brightness value ’0’ for INT_BRT and EXT_BRT is influenced by the white-drive control loop.		OK in D3
25	Contrast of analog inserted RGB	Up to 30 seconds after reset, the contrast is incorrect.	Workaround: Directly after reset, set 0x1e5 to 0x0001 and 0x0d6 to 0x5a00.	OK in E4
26	Measurement active after reset	Measurement lines appear at the analog RGB outputs.	Workaround: Directly after reset, set 0x1e5 to 0x0001 and 0x07d to 0x1800.	OK in E4
27	SAFETY function is always active.	Regardless of HPROT_DIS = 1, the RGB outputs will be blanked if SAFETY is connected to GNDD.	Workaround: 2.5 V DC at SAFETY Pin.	OK in D3
28	LLC1 connected to GNDD if not used	Automatic VSYNC polarity detection does not work.	Workaround: Connect LLC1 to VSUPD if not used.	See Adv. Info.
29	Doubled FIFORRD output	Regardless of DFDSW, the FIFORRD signal is always the doubled VS/VS2 input signal.	The FIFORD is also blanked during each VSYNC.	OK in E4
30	Matrix Coefficient MR1M	MR1M is always zero.	Using old matrix coefficients of B1 version	OK in D3
31	Progressive Scan	Problems with VBST, TML, and PFGVB in fields with more than 511 lines.	Set VBST to 511. Cutoff & WDR control loop does not work.	OK in D3*
32	BCL influences White-Drive measurement	If the BCL reduces the picture, the WDR measurement lines are also reduced!	See workaround No. 1.	OK in E4
33	Vertical protection does not work	Regardless of VPROT_DIS = 0, the picture will not be blanked if pin 11 (VPROT) detects an error.	See workaround No. 2.	OK in E4
34	3.3 V Pad supply	It is not possible to connect less than 4.75 V to VSUPP (supply voltage for the FIFO control signals).	Concerns only applications which use the FIFO control signals of the DDPB.	OK in E4

No.	Problem	Description	Comment	Status
35	Vertical sawtooth	Horizontal noise in vertical sawtooth		OK in E4
36	Reading PFG color	It is not possible to read the upper 8 bits of register PFC (I^2C-addr. h'11).		

The following three tables depict the firmware changes from the Version DDP 3310B-PT-B1 to DDP 3310B-PT-C2.

Addresses changed from *DDP 3310B-PT-B1* **to DDP 3310B-PT-C2**

XDFP Control and Status Registers						
B1 XDFP Subaddr.	***C2 XDFP Subaddr.***	**Function**			**Default**	**Name**
h'065	**h'17A**	Fast-Blank interface mode				FBLMODE
		bit [0]	0 1	Fast-Blank from FBLIN1 pin force internal Fast-Blank signal to high	0	FBFOH1
		bit [1]	0/1	Fast-Blank active high/low at FBLIN pin	0	FBPOL
		bit [2]	0 1	Fast-Blank from FBLIN1 pin force internal Fast-Blank signal to low	0	FBFOL1
		bit[3]	 0 1	Fast-Blank priority FBLIN1>FBLIN2 FBLIN1<FBLIN2	0	FBPRIO
		bit [4]	0 1	Fast-Blank from FBLIN2 pin force internal Fast-Blank signal to low	0	FBFOL2
		bit [5]	0 1	Fast-Blank from FBLIN2 pin force internal Fast-Blank signal to high	0	FBFOH2
		bit[6]	0/1	Fast-Blank monitor input select FBLIN1/2	0	FBMON
		bit[7]	0/1	disable/enable clamping for RGBIN1&2	0	CLAMP
		bit[8]	0/1	half contrast signal active high/low at HCS pin	0	HCSPOL
		bit[9]	0/1	disable/enable half contrast switching	0	HCSEN
		bit[10]	0 1	half contrast signal from HCS pin force internal half contrast signal to high	0	HCSFOH
h'1D7	**h'15F**	bit[10:0]	0... 1295	Latch timing of madc data **relative to the beginning of horiz. blanking HBST**	128	MADCLAT
		picture matrix coefficient R-Y = MR1M/64*C_B + MR2M/64*C_R				
h'1AD	**h'1B9**	**bit [15:7]**	–256 ... 255		0	MR1M
h'1A5	**h'1B8**	**bit [15:7]**	–256 ... 255		86	MR2M
		picture matrix coefficient G-Y = MG1M/64*C_B + MG2M/64*C_R				
h'19D	**h'1B7**	**bit [15:7]**	–256 ... 255		–22	MG1M
h'195	**h'1B6**	**bit [15:7]**	–256 ... 255		–44	MG2M
		picture matrix coefficient B-Y = MB1M/64*C_B + MB2M/64*C_R				
h'18D	**h'1B5**	**bit [15:7]**	–256 ... 255		113	MB1M
h'185	**h'1B4**	**bit [15:7]**	–256 ... 255		0	MB2M
h'1A2	**h'1B1**	bit [14:9]	0..63	picture contrast in steps of 1/32	32	CTM

Changed bit slices in DDP 3310B-PT-C2

XDFP Control and Status Registers							
Subaddr.	**Mode**	**Function**				**Default**	**Name**
h'140	16-r/w	horizontal deflection control register					HCTRL
		bit [0]	0	reserved, set to 0		0	
		bit [1]	0/1	enable/disable vertical protection		0	VPROT_DIS
		bit [2]	0/1	enable/disable H-safety protection		0	HPROT_DIS
		bit [3]	0/1	disable/enable drive high during flyback		0	EFLB
		bit [4]	1	start ramp up/down		0	RAMP_EN
		bit [7:5]	0..7	horizontal frequency		0	HFREQ
				H-Freq. in kHz	pixels per line @LLC 27 MHz / 32 MHz		
			000	31.25	864 / 1024		
			001	35.1	768 / 912		
			010	31.46	858 / 1024		
			100	33.8	800 / 944		
			101	37.5	720 / 852		
			110	37.9	712 / 844		
h'141	16-r/w	adjustable delay of PLL2, clamping, and blanking (relative to incoming hsync) adjust clamping pulse for analog RGB input				5	POFS2
		bit [15:1]	Range ±600, 1 step = 1 pixel clock				
h'144	16-r/w	adjustable delay of flyback, H/VSYNC and analog RGB (relative to PLL2) adjust horizontal drive or H/VSYNC				0	POFS3
		bit [15:1]	Range ±600, 1 step = 1 pixel clock				
h'160	16-r/w	bit[15:4]	0... 2047 0...–2048	BCL threshold current if SENSE input used BCL threshold current if RSW1 input used (max. ADC output ~2047)		64	BCL_THRES
h'161	16-r/w	bit[8:0]	0...511	BCL time constant; 0 = off		0	BCL_TC
h'1B0	16-r/w	Input format					INFMT
		bit [0]	0/1	4:2:2 / 4:1:1 mode		1	M411
		bit [1]	0/1	binary offset / 2's complement		1	COB
		bit [2]	0/1	enable / disable blanking to black (for luma and chroma input when HS = 0)		1	BLNK
		bit [4:3]	0...3	select color multiplex		0	CMUX

XDFP Control and Status Registers						
Subaddr.	**Mode**	**Function**			**Default**	**Name**
h'176	16-r/w	display frequency doubling control word				DFDCTRL
		bit[1:0]	display raster mode (A' = field A in raster B) 0 = A A' B' B 1 = A A B B 2 = A A B' B' 3=not used		0	DFDMODE
		bit[3:2]	minimum field length filter 0 = off 1 = 2 fields 2 = 3 fields 3 = 4 fields		0	DFDFILT
		bit[5:4]	input sync doubling switch 0 = leave H and V sync unchanged 1 = double VSYNC and leave HSYNC unchanged 2 = double HSYNC and leave VSYNC unchanged 3 = double H and V sync		0	DFDSW
		bit[6]	clock switch 0 = Clock from LLC2 pin divided by 2 1 = Clock from LLC1 pin		0	DFDCLK
		bit[7]	test bit, set to 0		0	
		bit[8]	0 1	automatic VS/VS2 polarity detection Low-active VS/VS2 input	0	VSYPOL
		bit[9]	0 / 1	High/Low-active HS input	0	HSYPOL
		bit[10]	0 / 1	VS / VS2 Pin is source of VSYNC	0	VSYSRC
		bit[11]	0 / 1	dis-/enable still picture (only available if display frequency doubling is enabled)	0	STILL
		bit[12]	0 / 1	High / Low-active FIFO control signals	0	FIFOPOL

New addresses in DDP 3310B-PT-C2

XDFP Control and Status Registers						
Subaddr.	**Mode**	**Function**			**Default**	**Name**
h'1B2	16-r/w	bit [15:9]	0...63 –1	picture saturation in steps of 1/32; reserved mode to use old MATRIX coefficients and CTM addresses from B1	–1	SATM
h'1B3	16-r/w	bit [14:8]	0...127	limit for picture contrast × saturation in steps of 1/32	80	SATLIM
h'17B	16-r/w	bit [15:4]	–128...127	delay from horizontal flyback to rising edge of HOUT (e.g. negative) in steps of 0.25 µs	0	SEC_POFS
h'18B	16-r/w	bit [8:0]	0...511	start point of active video relative to incoming HS signal in steps of 2 LLC2 clocks; can be used e.g. for panning	0	SFIF
h'198	16-r/w	bit [7:0]	0/1:	disable/enable analog FastBlank input1/2 if bit[x] is set to 1, then the function is active for the respective signal priority	0	PBFB1
h'194	16-r/w	bit [2:0]	0...7	picture frame generator priority id	7	PFGID
		bit [8]	0/1	enable prio id for picture frame generator	1	PFGEN

DDP 3310B-PT-B1 **23.09.98**

The DDP 3310B-PT-B1 is hardware, but not software compatible to version DDP 3310B-PT-A0

Problem list for DDP 3310B-PT-B1:

No.	Problem	Description	Comment	Status
12	HOUT after reset	If Flyback is available, the HOUT will go high after 82 ms (first two periods with 50% duty cycle, rest with 2 µs low and 16 µs high).		OK in C2
13	Horizontal free running after soft start	After soft start, HOUT is not locked to incoming HSYNC when HDRV > h'31.	Workaround: Set POFS3 to delay of HOUT vs. HFLB in clock periods times 4 and HDRV to h'30.	OK in C2
14	White-Drive measurement lines	Not all measurement lines for white-drive RGB appear in a correct order. Sometimes the measurement line for white-drive blue is not available.	Workaround: setting WDR_GAIN to zero to use WDR_RGB as drive values.	OK in D2
3	Scaler	SCMODE register h'1C1: When read, always '0'.	Firmware resets this register after scaler update.	OK in C2
15	Asynchronous vertical blanking in free running mode	In vertical free running mode, the incoming VSYNC causes a vertical blanking.		OK in C2
16	Crosstalk between SVM signal and analog main picture	Even if the analog SVM output signal is blanked, e.g. when analog RGB is inserted, there is a crosstalk of the SVM signal to the analog RGB output	Workaround: Set SVG to zero if analog RGB is inserted.	
17	The attenuation of the beam current limiter is too small and works incorrectly for BCL_TC > 200.	An attenuation of approximately max. 75% is available. If BCL_TC is greater than 240, every second line flickers.	Workaround: Switching off BCL function with BCL_GAIN = 0. A similar function can be achieved by manipulating drive measurement reference-values depending on the measured beam current.	OK in C2
18	Cutoff and white-drive measurement lines are blanked if FBFOL1 or FBFOL2 is set to '1'.	If the cutoff or white-drive control loop is active, the brightness or contrast is extremely increased.	Make sure that FBFOL1 and FBFOL2 are always cleared (= 0). If necessary, forcing can be done by setting FBFOH1 or FBFOH2 and inverting polarity by FBPOL = 1.	OK in C2

No.	Problem	Description	Comment	Status
19	EHT compensation does not work.	Vertical amplitude correction is unstable. Horizontal amplitude correction does not work.		OK in C2
20	Cutoff and white-drive measurement lines are blanked if BLANK_DIS = 0 (video mute).	If the cutoff or white-drive control loop is active, the brightness or contrast is extremely increased, after BLANK_DIS is set to ’1’.	Before setting BLANK_DIS = 0, be sure to disable the cutoff and white-drive control loop (CUT_DIS = 1, WDR_DIS = 1).	OK in C2
21	White-Drive measurement line has a too small amplitude if HCS is active during vertical blanking.	The white-drive measurement line is reduced to 50% of its normal amplitude.	Make sure that there is no active HCS during vertical blanking.	OK in C2
22	After about 1 minute, the external contrast will be increased.	The external contrast changes significantly.		OK in D3

DDP 3310B-PS-A0 (TC 0101) **24.04.1998**

Problem list for DDP 3310B-PT-A0:

No.	Problem	Description	Comment	Status
1	Picture Frame Generator	pfghb full frame = $7ff has no function		OK in B1
2	Cutoff / White-Drive Control loop	CUT_DIS, WDR_DIS has no function. White-Drive and Cutoff measurements do not work.	No measurement lines.	OK in B1
3	Scaler	SCMODE register h'1C1: When read, always '0'.	Firmware resets this register after scaler update.	OK in C2
4	Vertical Protection	If activated, HOUT will be switched to free running 50%, RGB is not blanked.	Firmware change.	OK in B1
5	Vertical DAC	The flyback booster (VBI recharge) does not work if the internal load resistances are switched off.		OK in B1
6	adjustments for vertical and East/West	Gain for East/West is too small.	Firmware change.	OK in B1
7	Vertical Modes	Non-interlaced modes do not work correctly.	Firmware change.	OK in B1
8	RGB Outputs	Adjustments of drive, cutoff, and analog brightness do not work correctly.	Fix settings for: INT_BRT = –256	OK in B1
9	H-Drive	Horizontal jitter on H-Drive signal	Firmware problem.	OK in B1
10	H-Drive	Soft Start/Stop function of HOUT does not work.	Firmware problem.	OK in B1
11	H-SYNC input	For correct scaler operation, active video is required; this causes incorrect vertical raster modes.	Vertical blanked active video signal.	OK in B1

List of Workarounds

1. BCL Influences White-Drive Measurement (Problem No. 32) **05.05.99**

The BCL reduces the gain of the RGB drive multipliers. Also, the measurement lines for the white-drive control loop are reduced (by mistake). Therefore, the WDR control increases the gain more and more. To overcome this problem, software can be used to compensate this effect.

General description of the White-Drive Control Loop

One complete white-drive measurement cycle takes three fields (one field for each R, G, and B). Therefore, the white-drive control loop is updated every third field. If only small errors of the RGB cathodes must be compensated, 4 control loop cycles should be sufficient to keep the remaining error small.

A. White-Drive Control Loop active only during blanked picture (e.g. channel switching)

If the picture is blanked or shown with small contrast and brightness for 12 fields during channel switching, the white-drive control loop can be activated, because the BCL does not reduce the contrast due to small beam current. When the picture is stable after channel switching the white-drive loop can be stopped and the normal picture settings can be restored. The calculated new white-drive values will be fix until the next channel switch procedure.

Description of procedure:

1. BLANK_DIS = 0 (blank complete picture or reduced contrast/brightness)
2. WDR_DIS = 0 (start white-drive control loop)
3. all necessary commands for channel switching
4. WDR_DIS = 1 (stop white-drive control loop)
5. BLANK_DIS = 1 (show complete picture or restore contrast/brightness)

B. White-Drive Control Loop active only during modified beam current limiter (BCL)

It is possible to modify the behavior of the BCL so that the contrast is reduced down to a certain limit (BCL_MIN_C in DDP 3310B) if the beam current is too high. If this limit is reached and the remaining beam current is still too high, the brightness will then be reduced. If this minimum contrast is about 94% (BCL_MIN_C = 480), the white-drive control loop can work properly.

This high limit for contrast reduction for the BCL may not be the desired value for the customer. So this limit should only be set during a certain period of time (about 12 fields), to turn on the white-drive control loop. If the difference of the modified BCL settings to the usual settings is not visible, this workaround could have a faster update rate of the white-drive loop than suggestion No. 1.

Description of procedure:

1. BCL_MIN_C = 480 (increase minimum contrast of BCL to 94%)
2. WDR_DIS = 0 (activate white-drive control loop)
3. wait for 12 fields or channel switching
4. WDR_DIS = 1 (disable white-drive control loop)
5. BCL_MIN_C = old value (switch to old minimum contrast of BCL)

External control loop to compensate reduction of measurement lines (WDRM):

The start value of WDRM should be around 256, then you have enough space to increase it up to 511.

Description of procedure:

1. Read register BCL_C (BCL_C: XDFP Addr.: h’E8, Bit[14:6])
2. coeff = (BCL_C * 2^-7) AND h’FF (calculate reduction factor of BCL)
3. NEWWDRM = WDRMSTART / coeff (compensate reduction)
4. IF(NEWWDRM > h’1FF) THEN NEWWDRM = h’1FF (limit to maximum 511)
5. Write NEWWDRM to WDRM register

2. Vertical Protection does not Work (Problem No. 33) 05.05.99

Regardless of VPROT_DIS = 0, the picture will not be blanked if pin 11 (VPROT) detects an error.

As a workaround, the actual status of the vertical protection can be read out from the XDFP-Register address h’11D bit[6]. This information can be used, for example, to blank the entire picture (BLANK_DIS = 0).