SONY

CXP81952M/81960M

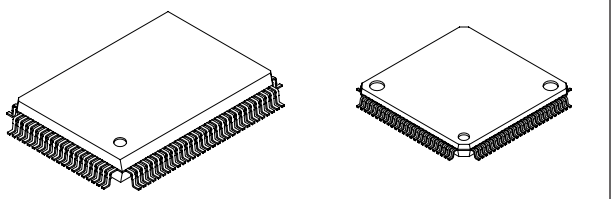
CMOS 8-bit Single Chip Microcomputer

Description

The CXP81952M/81960M is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, PWM for tuner, 32kHz timer/event counter, remote control reception circuit, and FRC capture unit, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also the CXP81952M/81960M provides sleep/stop functions which enable to lower power consumption and ultra-low speed instruction mode in 32kHz operation.

100 pin QFP (Plastic) 100 pin LQFP (Plastic)



Structure

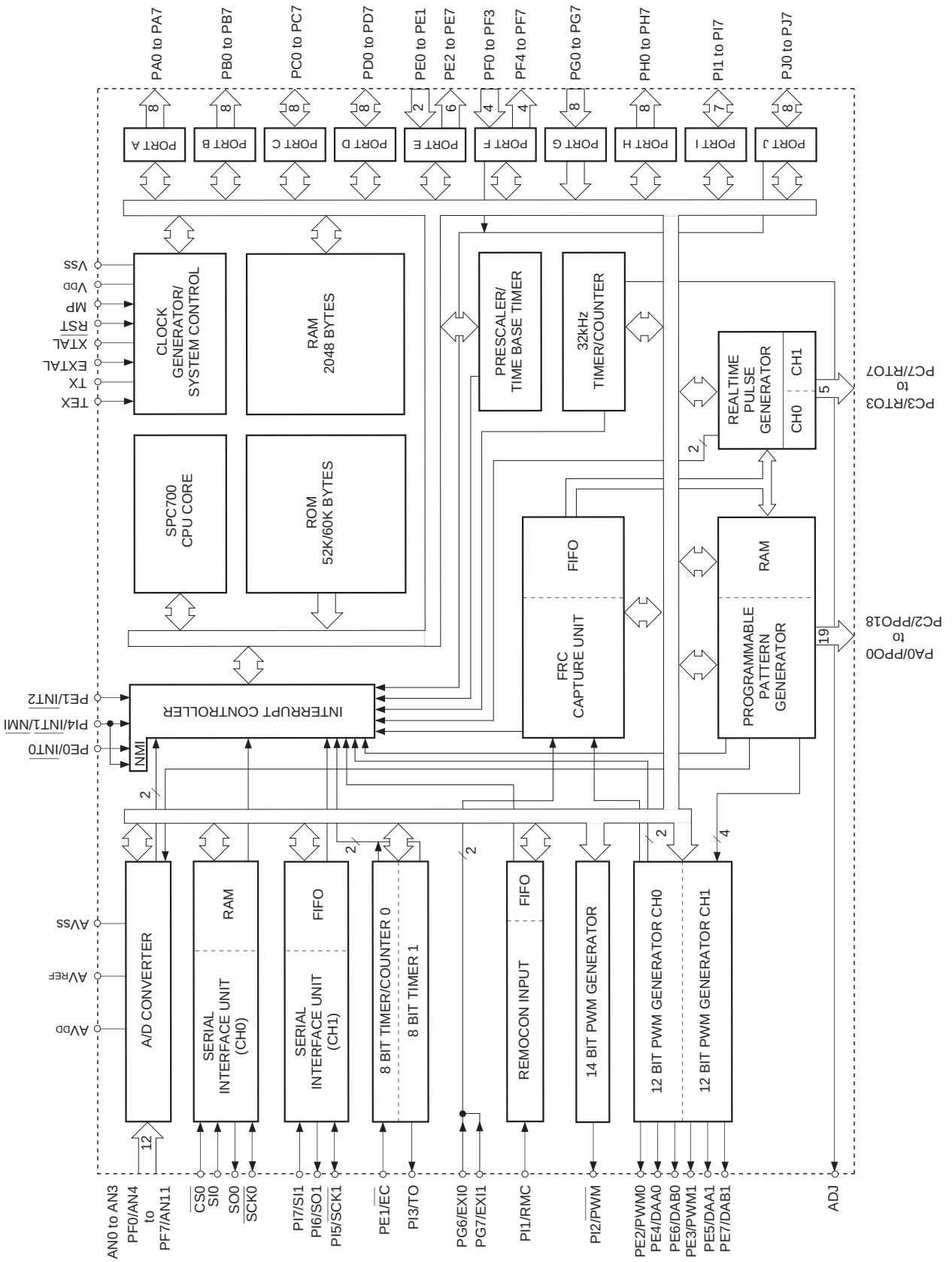
Silicon gate CMOS IC

Features

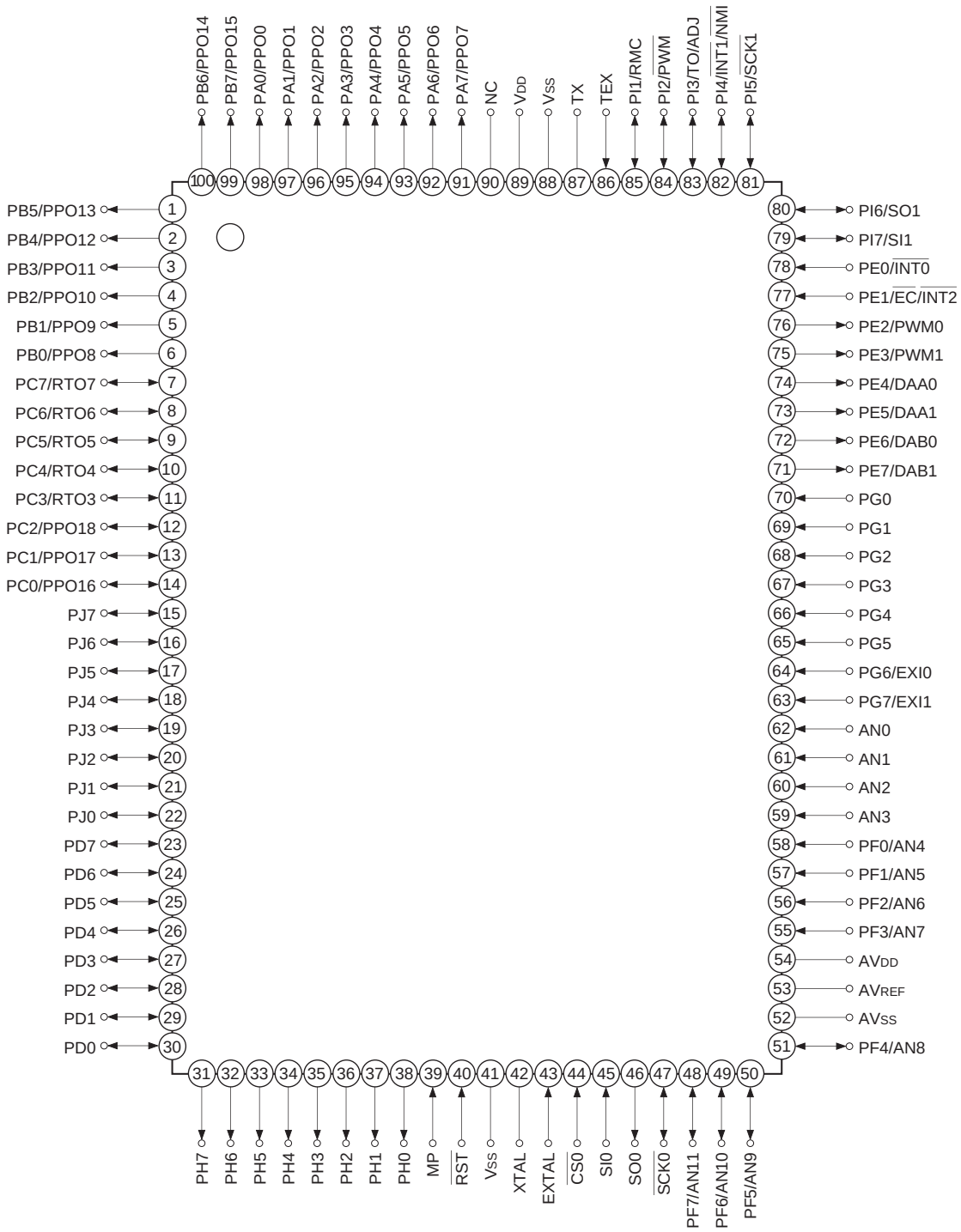
- A wide instruction set (213 instructions) which covers various types of data
  — 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle 200ns at 20MHz operation (4.5 to 5.5V)
  333ns at 12MHz operation (2.7 to 5.5V)
  122µs at 32kHz operation
- Incorporated ROM capacity 52K bytes (CXP81952M), 60K bytes (CXP81960M)
- Incorporated RAM capacity 2048 bytes
- Peripheral functions
  - — A/D converter: 8 bits, 12 channels, successive approximation system (Conversion time of 16µs at 20MHz)
  - — Serial Interface: Incorporated buffer RAM (1 to 32 bytes auto transfer), 1 channel
    Incorporated 8-bit and 8-stage FIFO (1 to 8 bytes auto transfer), 1 channel
  - — Timer: 8-bit timer, 8-bit timer/counter, 19-bit time base timer, 32kHz timer/counter
  - — High precision timing pattern generator: PPG: maximum of 19 pins, 32 stages programmable
    RTG: 5 pins, 2 channels
  - — PWM/DA gate output: PWM: 12 bits, 2 channels (Repetitive frequency of 78kHz at 20MHz)
    DA gate pulse output: 13 bits, 4 channels
  - — FRC capture unit: Incorporated 26-bit and 8-stage FIFO
  - — PWM output: 14 bits, 1 channel
  - — Remote control reception circuit: 8-bit pulse measurement counter with on-chip 6-stage FIFO
- Interruption 20 factors, 15 vectors, multi-interruption possible
- Standby mode Sleep/stop
- Package 100-pin plastic QFP/LQFP
- Piggyback/evaluator CXP81900M

E95511A69-PS

Block Diagram

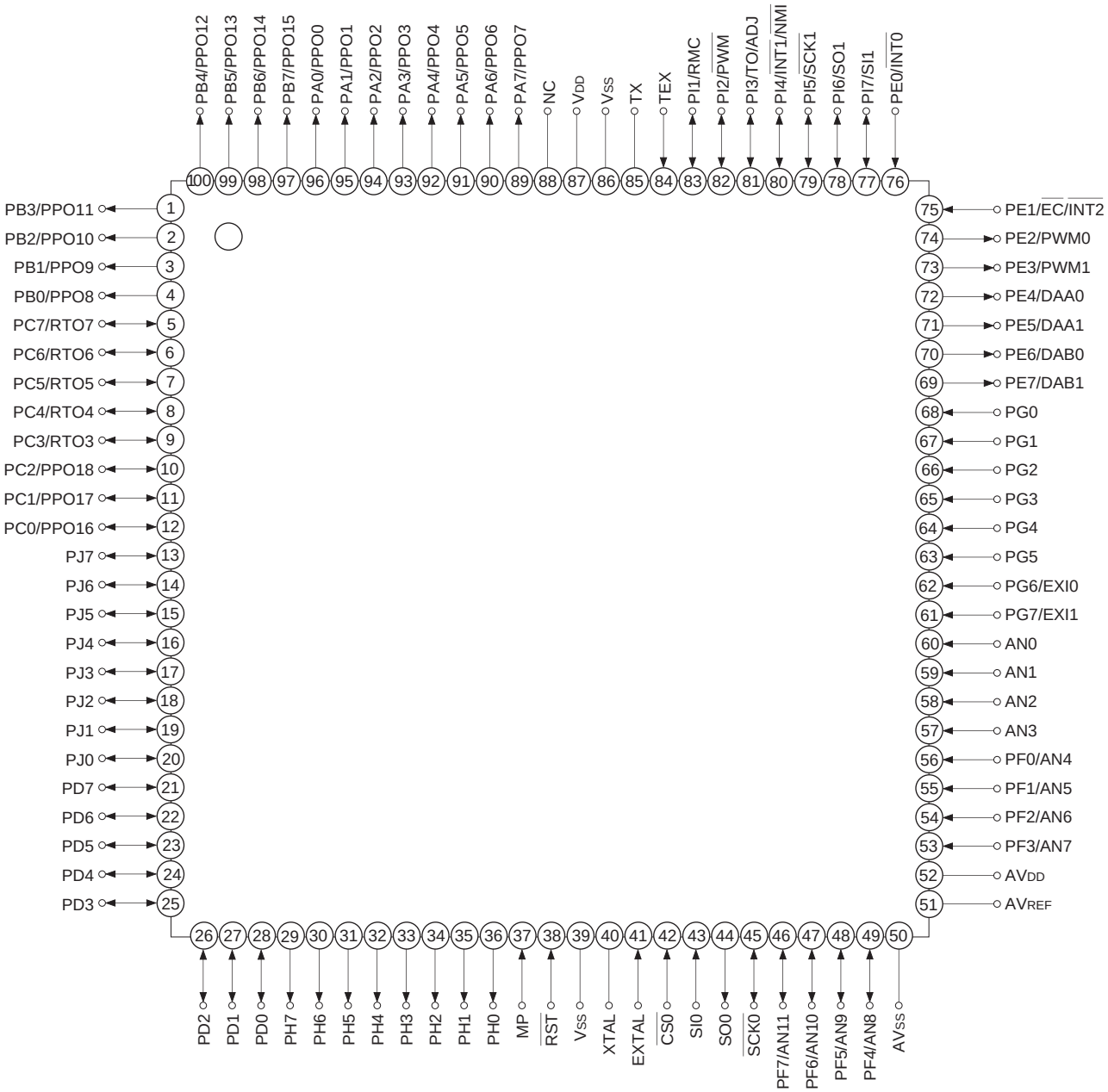


Pin Assignment 1 (Top View) 100-pin QFP package



Note) 1. NC (Pin 90) is always connected to V_{DD}.
2. Vss (Pins 41 and 88) are both connected to GND.
3. MP (Pin 39) is always connected to GND.

Pin Assignment 2 (Top View) 100-pin LQFP package



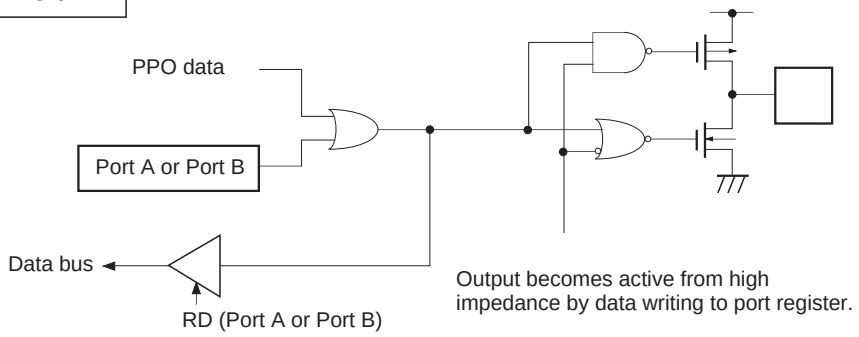
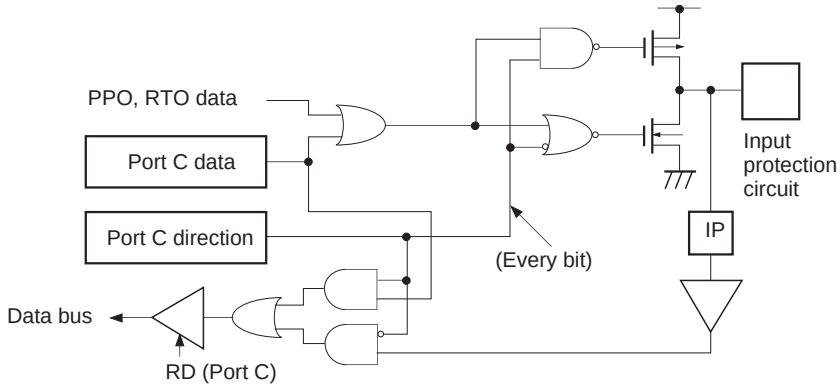
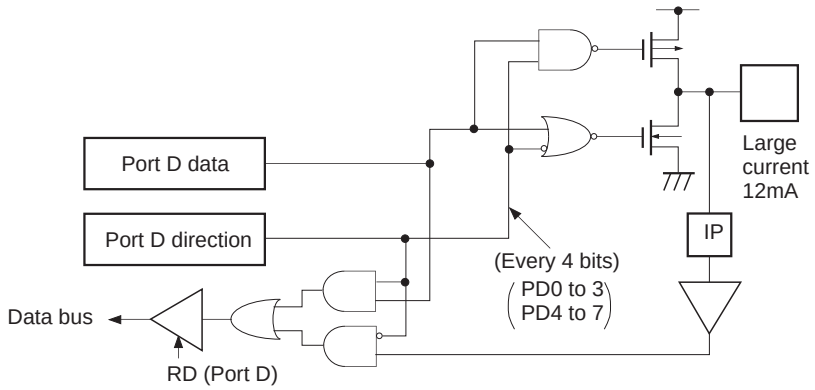
Note) 1. NC (Pin 88) is always connected to V_{DD}.
2. Vss (Pins 39 and 86) are both connected to GND.
3. MP (Pin 37) is always connected to GND.

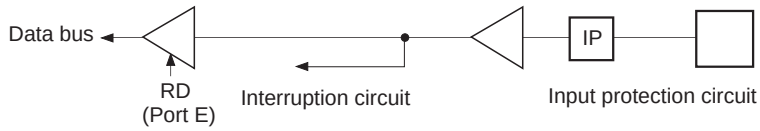
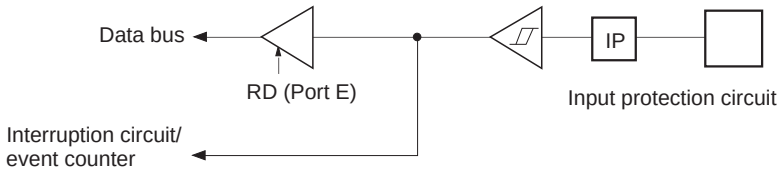
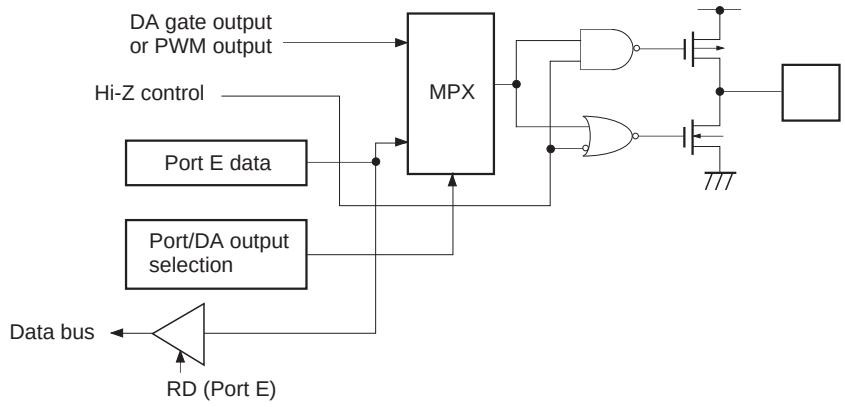
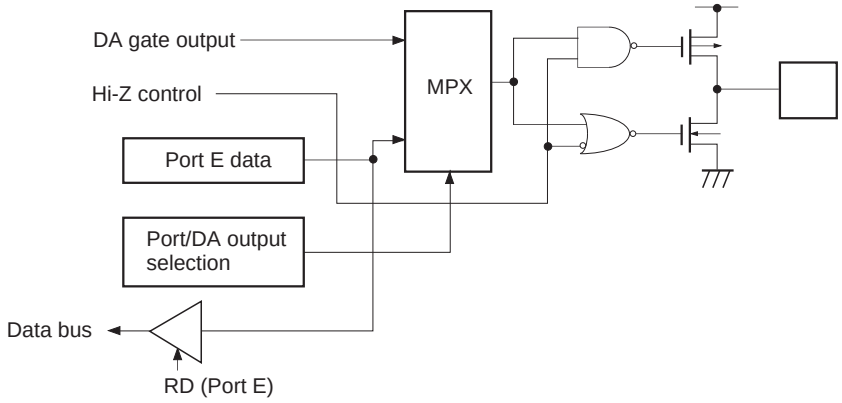
Pin Description

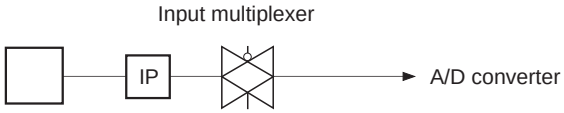
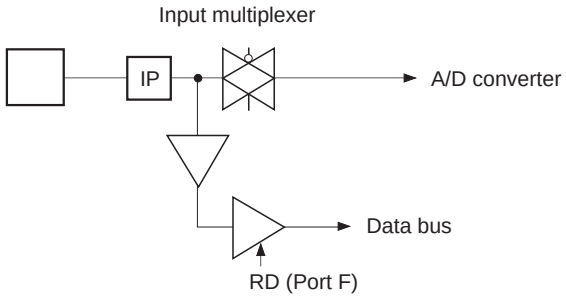
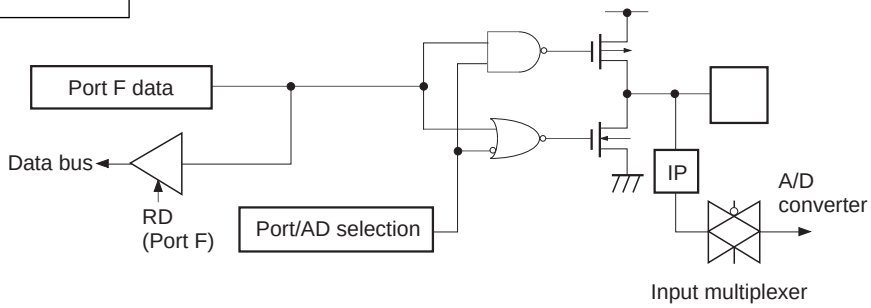
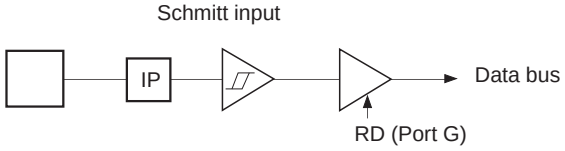
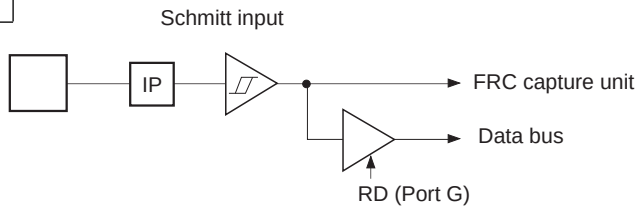
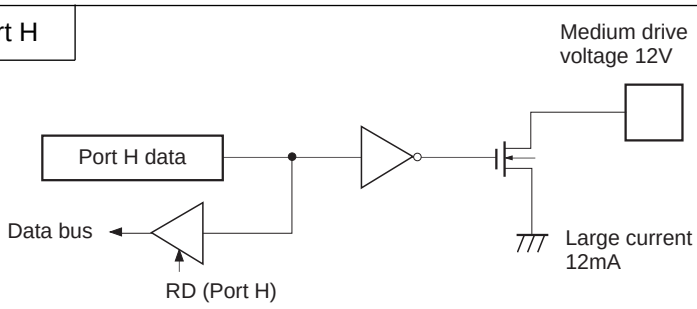
<table>
<tr><th>Symbol</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td>PA0/PPO0
to
PA7/PPO7</td><td>Output/
Real-time output</td><td>(Port A)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
(8 pins)</td><td colspan="2" rowspan="3">Programmable pattern generator (PPG) output.
Functions as high precision real-time pulse output port.
(19 pins)</td></tr>
<tr><td>PB0/PPO8
to
PB7/PPO15</td><td>Output/
Real-time output</td><td>(Port B)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
(8 pins)</td></tr>
<tr><td>PC0/PPO16
to
PC2/PPO18</td><td>I/O/
Real-time output</td><td rowspan="2">(Port C)
8-bit I/O port. I/O can be set in a unit of single bits.
Data is gated with PPO or RTO contents by OR-gate and they are output.
(8 pins)</td></tr>
<tr><td>PC3/RTO3
to
PC7/RTO7</td><td>I/O/
Real-time output</td><td colspan="2">Real-time pulse generator (RTG) output.
Functions as high precision real-time pulse output port. (5 pins)</td></tr>
<tr><td>PD0 to PD7</td><td>I/O</td><td colspan="3">(Port D)
8-bit I/O port. I/O can be set in a unit of 4bits.
Can drive 12mA sink current.
(8 pins)</td></tr>
<tr><td>PE0/$\overline{\text{INT0}}$</td><td>Input/Input</td><td rowspan="8">(Port E)
8-bit port.
Lower 2 bits are for input; upper 6 bits are for output.
(8 pins)</td><td colspan="2">Input pin to request external interruption.
Active at the falling edge.</td></tr>
<tr><td>PE1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$</td><td>Input/Input/Input</td><td>External event input pin for timer/counter.</td><td>Input pin to request external interruption.
Active at the falling edge.</td></tr>
<tr><td>PE2/PWM0</td><td>Output/Output</td><td colspan="2" rowspan="2">PWM output pins.
(2 pins)</td></tr>
<tr><td>PE3/PWM1</td><td>Output/Output</td></tr>
<tr><td>PE4/DAA0</td><td>Output/Output</td><td colspan="2" rowspan="4">DA gate pulse output pins.
(4 pins)</td></tr>
<tr><td>PE5/DAA1</td><td>Output/Output</td></tr>
<tr><td>PE6/DAB0</td><td>Output/Output</td></tr>
<tr><td>PE7/DAB1</td><td>Output/Output</td></tr>
<tr><td>AN0 to AN3</td><td>Input</td><td colspan="3">Analog input pins to A/D converter. (12 pins)</td></tr>
<tr><td>PF0/AN4
to
PF3/AN7</td><td>Input/Input</td><td colspan="3" rowspan="2">(Port F)
8-bit port. Lower 4 bits are for input; upper 4 bits are for output.
Lower 4 bits also serve as standby release input pin.
(8 pins)</td></tr>
<tr><td>PF4/AN8
to
PF7/AN11</td><td>Output/Input</td></tr>
<tr><td>$\overline{\text{SCK0}}$</td><td>I/O</td><td colspan="3">Serial clock (CH0) I/O pin.</td></tr>
<tr><td>SO0</td><td>Ouput</td><td colspan="3">Serial data (CH0) output pin.</td></tr>
<tr><td>SI0</td><td>Input</td><td colspan="3">Serial data (CH0) input pin.</td></tr>
<tr><td>$\overline{\text{CS0}}$</td><td>Input</td><td colspan="3">Serial chip select (CH0) input pin.</td></tr>
</table>

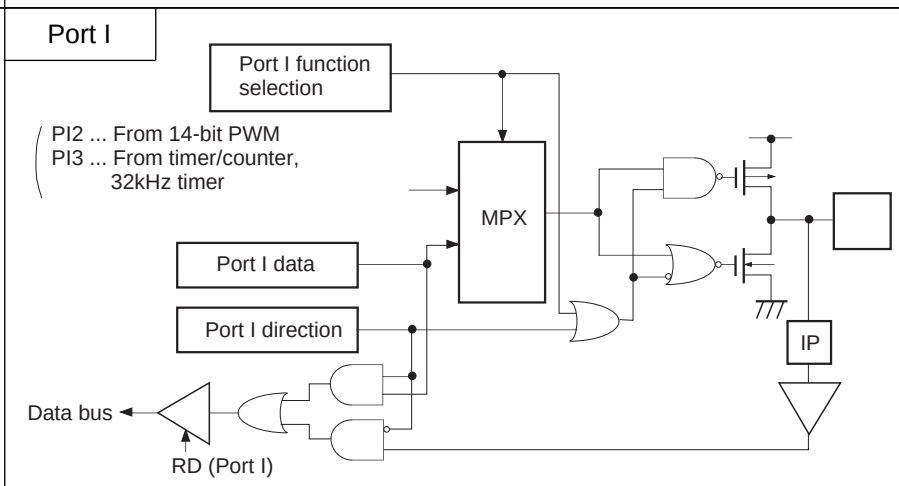
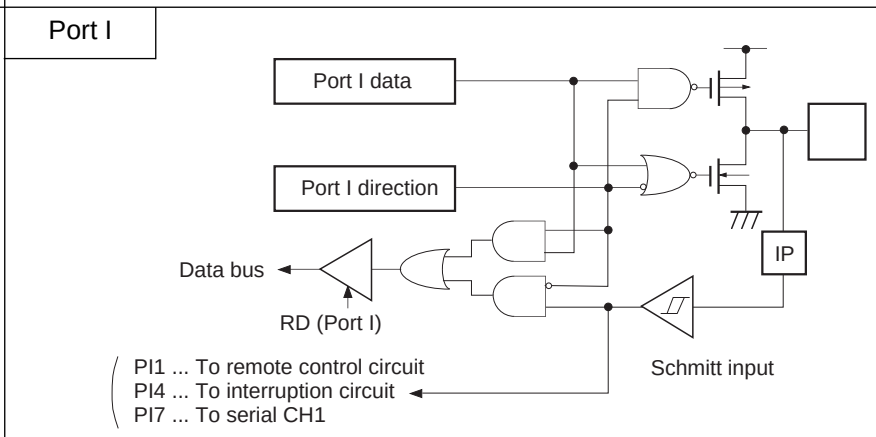
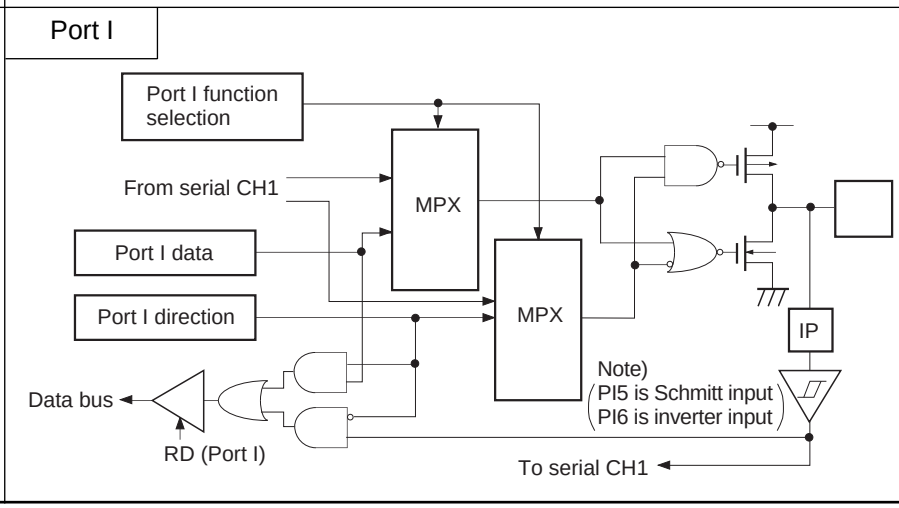
Symbol	I/O	Description	
PG0 to PG4	Input	(Port G) 8-bit input port. (8 pins)	
PG5			
PG6/EXI0			External input pin to FRC capture unit.
PG7/EXI1			
PH0 to PH7	Output	(Port H) 8-bit output port; N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O port can be set in a unit of single bits. (7 pins)	Remote control reception circuit input pin.
PI2/$\overline{\text{PWM}}$	I/O/Output		14-bit PWM output pin.
PI3/TO/ADJ	I/O/Output/Output		Timer/counter, 32kHz oscillation adjustment output pin.
PI4/$\overline{\text{INT1}}$/$\overline{\text{NMI}}$	I/O/Input/Input		Input pin to request external interruption and non-maskable interruption. Active at the falling edge.
PI5/$\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O pin.
PI6/SO1	I/O/Output		Serial data (CH1) output pin.
PI7/SI1	I/O/Input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. I/O and standby release input can be set in a unit of single bits.	
EXTAL	Input	Connects a crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connects a crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)	
TX	Output		
$\overline{\text{RST}}$	Input	System reset pin; active at Low level.	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AV_{DD}		Positive power supply pin of A/D converter.	
AV_{REF}	Input	Reference voltage input pin of A/D converter.	
AVss		GND pin of A/D converter.	
V_{DD}		Positive power supply pin.	
Vss		GND pin. Connect both Vss pins to GND.	

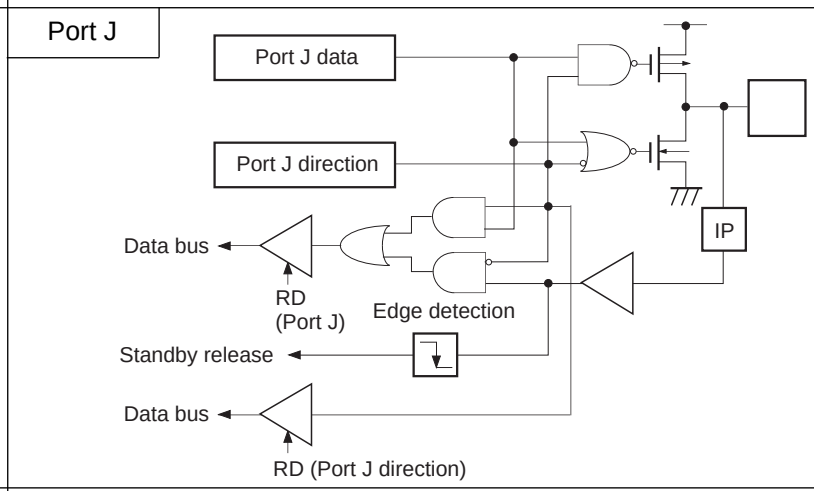
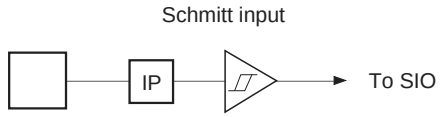
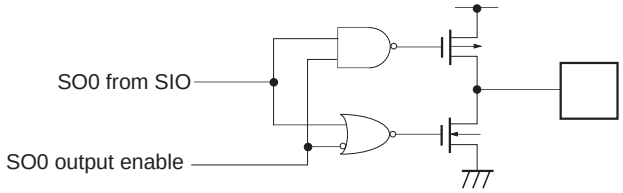
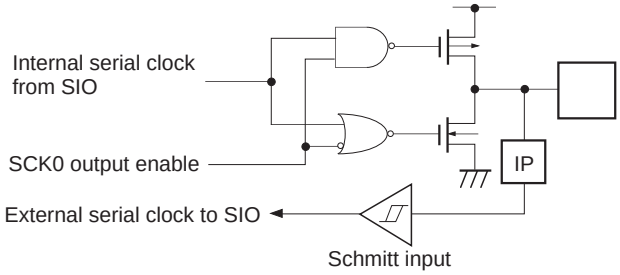
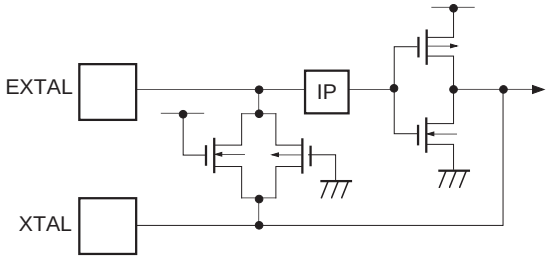
Input/Output Circuit Formats for Pins

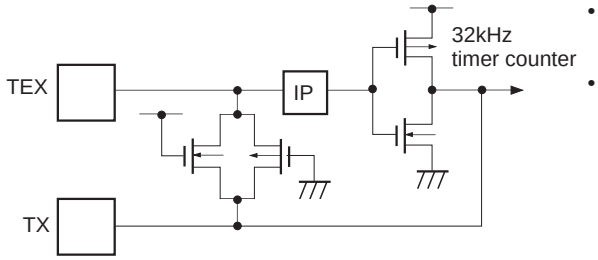
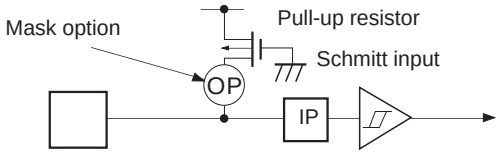
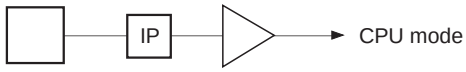
Pin	Circuit format	When reset
PA0/PPO0 to PA7/PPO7 PB0/PPO8 to PB7/PPO15 16 pins	Port A Port B 	Hi-Z
PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7 8 pins	Port C 	Hi-Z
PD0 to PD7 8 pins	Port D 	Hi-Z

Pin	Circuit format	When reset
PE0/$\overline{\text{INT0}}$ 1 pin	Port E 	Hi-Z
PE1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$ 1 pin	Port E 	Hi-Z
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E 	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E 	High level

Pin	Circuit format	When reset
AN0 to AN3 4 pins		Hi-Z
PF0/AN4 to PF3/AN7 4 pins	Port F 	Hi-Z
PF4/AN8 to PF7/AN11 4 pins	Port F 	Hi-Z
PG0 to PG5 6 pins	Port G 	Hi-Z
PG6/EXI0 PG7/EXI1 2 pins	Port G 	Hi-Z
PH0 to PH7 8 pins	Port H 	Hi-Z

Pin	Circuit format	When reset
PI2/$\overline{\text{PWM}}$ PI3/TO/ADJ 2 pins		Hi-Z
PI1/RMC PI4/$\overline{\text{INT1}}$/$\overline{\text{NMI}}$ PI7/SI1 3 pins		Hi-Z
PI5/$\overline{\text{SCK1}}$ PI6/SO1 2 pins		Hi-Z

Pin	Circuit format	When reset
PJ0 to PJ7 8 pins	Port J 	Hi-Z
$\overline{CS0}$ SI0 2 pins		Hi-Z
SO0 1 pin		Hi-Z
$\overline{SCK0}$ 1 pin		Hi-Z
EXTAL XTAL 2 pins	 • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop mode.	Oscillation

Pin	Circuit format	When reset
TEX TX 2 pins	 • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs Low level and TX pin outputs High level.	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level
MP 1 pin		Hi-Z

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	AV_{DD}	AVss to +7.0*1	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*2	V	
Output voltage	V_{OUT}	–0.3 to +7.0*2	V	
Medium drive output voltage	V_{OUTP}	–0.3 to +15.0	V	PH pin
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Pins excluding large current outputs (value per pin)
	I_{OLC}	20	mA	Large current output pin (value per pin*3)
Low level total output current	$\sum I_{OL}$	130	mA	Total of output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP
		380		LQFP

*1 AV_{DD} and V_{DD} should be set to the same voltage.

*2 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*3 The large current operation transistors are the N-CH transistors of the PD and PH ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks	
Supply voltage	V_{DD}	4.5	5.5	V	fc = 20MHz or less	Guaranteed operation range for high-speed mode (1/2 frequency dividing clock)
		2.7	5.5	V	fc = 12MHz or less	
		2.7	5.5	V	Guaranteed operation range for low-speed mode (1/16 frequency dividing clock)	
		2.5	5.5	V	Guaranteed operation range by TEX clock	
		2.0	5.5	V	Guaranteed data hold range for stop mode	
Analog supply voltage	AV_{DD}	2.7	5.5	V	*1	
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2	
	V_{IHS}	0.8V_{DD}	V_{DD}	V	CMOS Schmitt input*3 and PE0/$\overline{INT0}$	
			5.5	V	CMOS Schmitt input*6	
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL*4, *7 and TEX*5, *7	
		V_{DD} – 0.2	V_{DD} + 0.2	V	EXTAL*4, *8 and TEX*5, *8	
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2, *7	
		0	0.2V_{DD}	V	*2, *8	
	V_{ILS}	0	0.2V_{DD}	V	CMOS Schmitt input*3 and PE0/$\overline{INT0}$	
	V_{ILEX}	–0.3	0.4	V	EXTAL*4, *7 and TEX*5, *7	
		–0.3	0.2	V	EXTAL*4, *8 and TEX*5, *8	
Operating temperature	Topr	–20	+75	°C		

*1 AV_{DD} and V_{DD} should be set to the same voltage.

*2 Normal input ports (PC, PD, PF0 to PF3, PG, PI and PJ), MP

*3 $\overline{SCK0}$, $\overline{RST}$, PE1/$\overline{EC}$/$\overline{INT2}$, PI1/RMC, PI4/$\overline{INT1}$/$\overline{NMI}$, PI5/$\overline{SCK1}$ and PI7/SI1

*4 Specifies only when the external clock is input.

*5 Specifies only when the external event count clock is input.

*6 $\overline{CS0}$, SI0 and PG

*7 In case of 4.5 to 5.5V supply voltage (V_{DD}).

*8 In case of 2.7 to 3.3V supply voltage (V_{DD}).

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V) (Ta = –20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V_{OL} only) PI1 to PI7 PJ, SO0, $\overline{SCK0}$	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PH	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*1		–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP AN0 to AN3, $\overline{CS0}$, SI0, SO0 $\overline{SCK0}$, $\overline{RST}$*1	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Open drain output leakage current (in N-CH Tr OFF state)	I_{LOH}	PH	V_{DD} = 5.5V V_{OH} = 12V			50	µA
Supply current*2	I_{DD1}	V_{DD}	High speed mode (1/2 frequency dividing clock) operation				
			V_{DD} = 5.5V, 20MHz crystal oscillation (C_1 = C_2 = 15pF)		39	60	mA
	I_{DDS1}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		39	100	µA
	I_{DD2}		Sleep mode				
			V_{DD} = 5.5V, 20MHz crystal oscillation (C_1 = C_2 = 15pF)		2.1	10	mA
	I_{DDS2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		7	30	µA
	I_{DDS3}		Stop mode				
			V_{DD} = 5.5V, termination of 20MHz and 32kHz oscillation			10	µA
Input capacity	C_{IN}	Other than V_{DD}, Vss, AV_{DD}, and AVss	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 For $\overline{RST}$ pin, specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

*2 When all output pins are open.

DC Characteristics (V_{DD} = 2.7 to 3.3V) (Ta = –20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V_{OL} only) PI1 to PI7 PJ, SO0, $\overline{SCK0}$	V_{DD} = 2.7V, I_{OH} = –0.12mA	2.5			V
			V_{DD} = 2.7V, I_{OH} = –0.45mA	2.1			V
Low level output voltage	V_{OL}		V_{DD} = 2.7V, I_{OL} = 1.0mA			0.25	V
			V_{DD} = 2.7V, I_{OL} = 1.4mA			0.4	V
		PD, PH	V_{DD} = 2.7V, I_{OL} = 4.5mA			0.9	V
Input current	I_{IHE}	EXTAL	V_{DD} = 3.3V, V_{IH} = 3.3V	0.3		20	µA
	I_{ILE}		V_{DD} = 3.3V, V_{IL} = 0.3V	–0.3		–20	µA
	I_{IHT}	TEX	V_{DD} = 3.3V, V_{IH} = 3.3V	0.1		10	µA
	I_{ILT}		V_{DD} = 3.3V, V_{IL} = 0.3V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*1		–0.9		–200	µA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP AN0 to AN3, $\overline{CS0}$, SI0, SO0 $\overline{SCK0}$, $\overline{RST}$*1	V_{DD} = 3.3V, V_I = 0, 3.3V			±10	µA
Open drain output leakage current	I_{LOH}	PH	V_{DD} = 3.3V, V_{OH} = 12V			50	µA
Supply current*2	I_{DD1}	V_{DD}	12MHz crystal oscillation (C_1 = C_2 = 15pF) V_{DD} = 3.0V ± 0.3V*3		13	25	mA
	I_{DDS1}		Sleep mode V_{DD} = 3.0V ± 0.3V		0.7	2.0	mA
	I_{DDS3}		Stop mode (EXTAL and TEX pins oscillation stop) V_{DD} = 3.0V ± 0.3V			10	µA
Input capacity	C_{IN}	Other than V_{DD}, Vss, AV_{DD}, and AVss	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 For $\overline{RST}$ pin, specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

*2 When all output pins are open.

*3 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FE$_H$) to "00" and operating in high-speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta = –20 to +75°C, V_{DD} = 2.7 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, V_{DD} = 4.5 to 5.5V	1	20	MHz
			Fig. 2	1	12	
System clock input pulse width	t_{XL}, t_{XH}	XTAL EXTAL	Fig. 1, V_{DD} = 4.5 to 5.5V	23		ns
			Fig. 2 (External clock drive)	37.5		
System clock input rise and fall times	t_{CR}, t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns
Event count clock input pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	$t_{sys} \times 4$*1		ns
Event count clock input rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3		20	ns
System clock frequency	f_C	TEX TX	Fig. 2 V_{DD} = 2.5 to 5.5V (32kHz clock applied condition)	32.768		kHz
Event count clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10		µs
Event count clock input rise and fall times	t_{TR}, t_{TF}	TEX	Fig. 3		20	ms

*1 tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)

Fig. 1. Clock timing

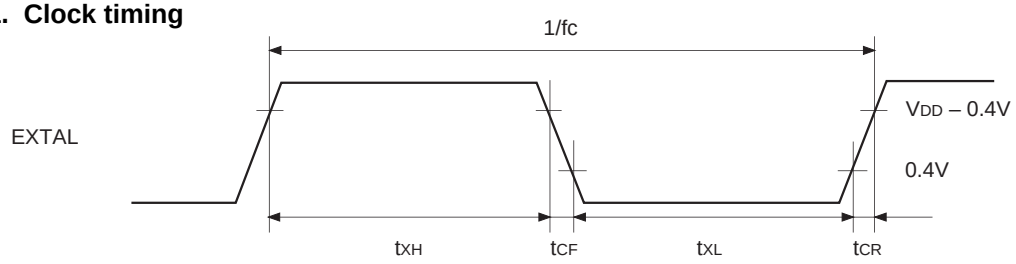


Fig. 2. Clock applied condition

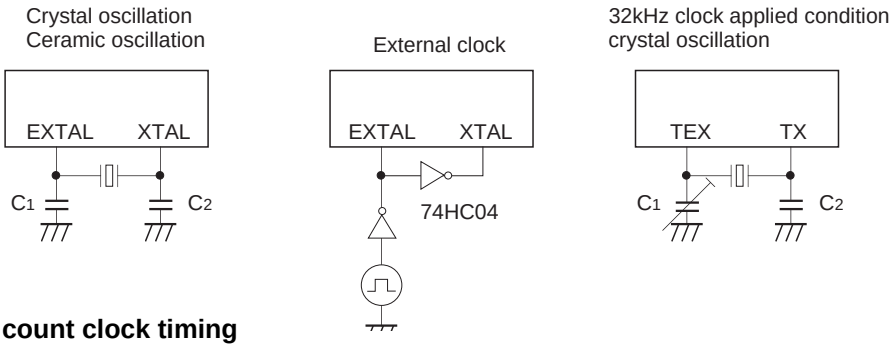
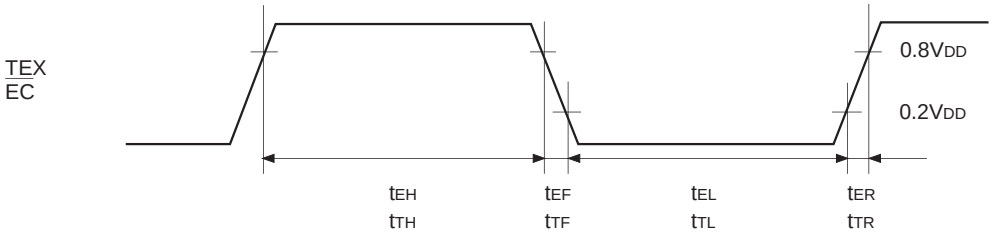


Fig. 3. Event count clock timing



(2) Serial transfer (CH0) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS} \downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS} \downarrow \rightarrow$ SO floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 100		ns
SI input setup time (for $\overline{SCK} \uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK} \uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	2tsys + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow$ SO delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		2tsys + 200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; $00FE_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO represents $\overline{CS0}$, SCK0, SI0 and SO0, respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

Serial transfer (CH0) (Ta = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V reference)

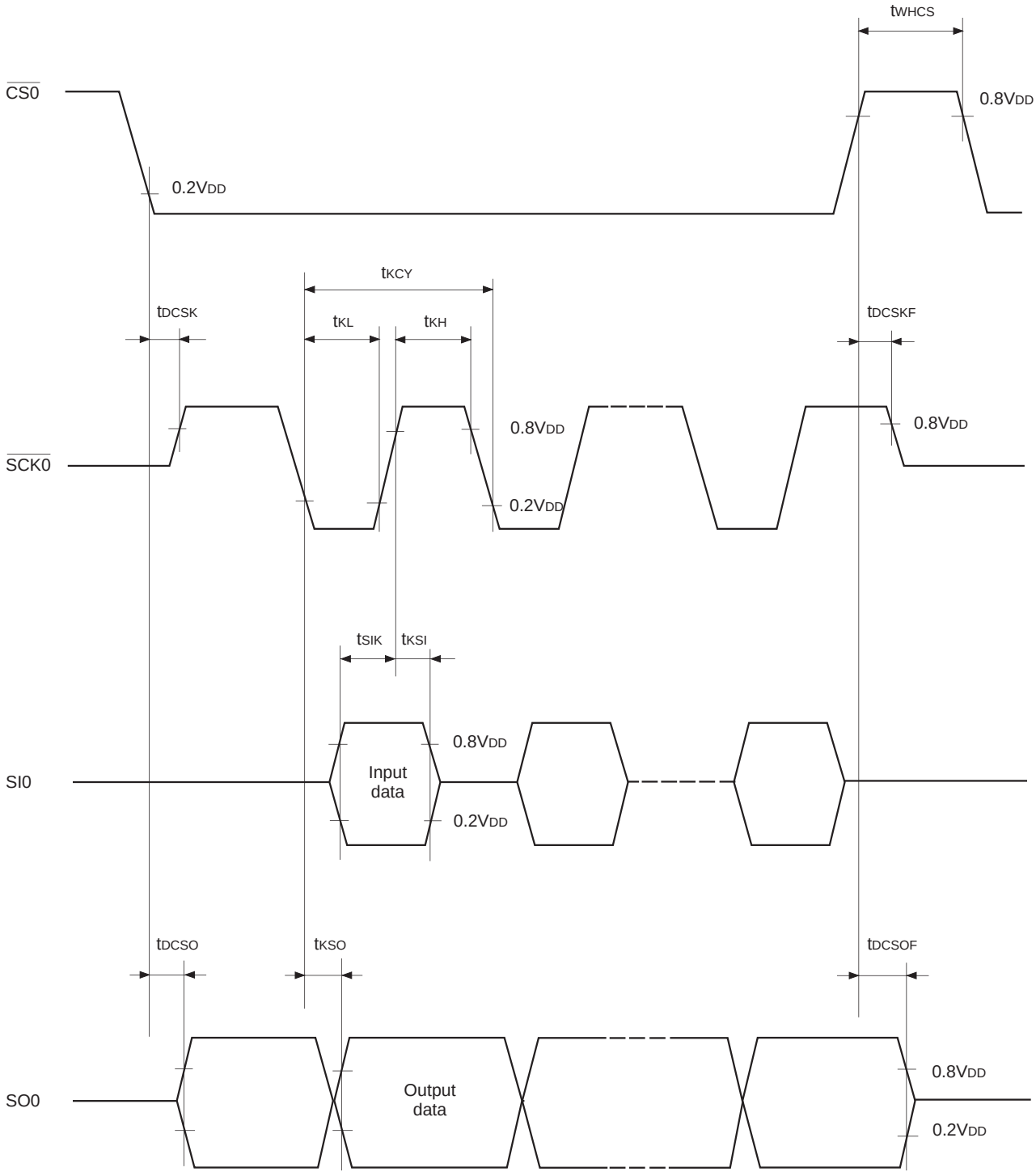
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 250	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS} \downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 250	ns
$\overline{CS} \downarrow \rightarrow$ SO floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 150		ns
SI input setup time (for $\overline{SCK} \uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK} \uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	2tsys + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow$ SO delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		2tsys + 250	ns
			$\overline{SCK}$ output mode		125	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO represents $\overline{CS0}$, SCK0, SI0 and SO0, respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer timing (CH0)



Serial transfer (CH1) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	2tsys + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK1}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	tsys + 100		ns
			Output mode	4000/fc – 100		ns
SI1 input setup time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	tsys + 200		ns
			$\overline{SCK1}$ output mode	100		ns
SCK1 ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		tsys + 200	ns
			$\overline{SCK1}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)

Note 2) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF + 1TTL.

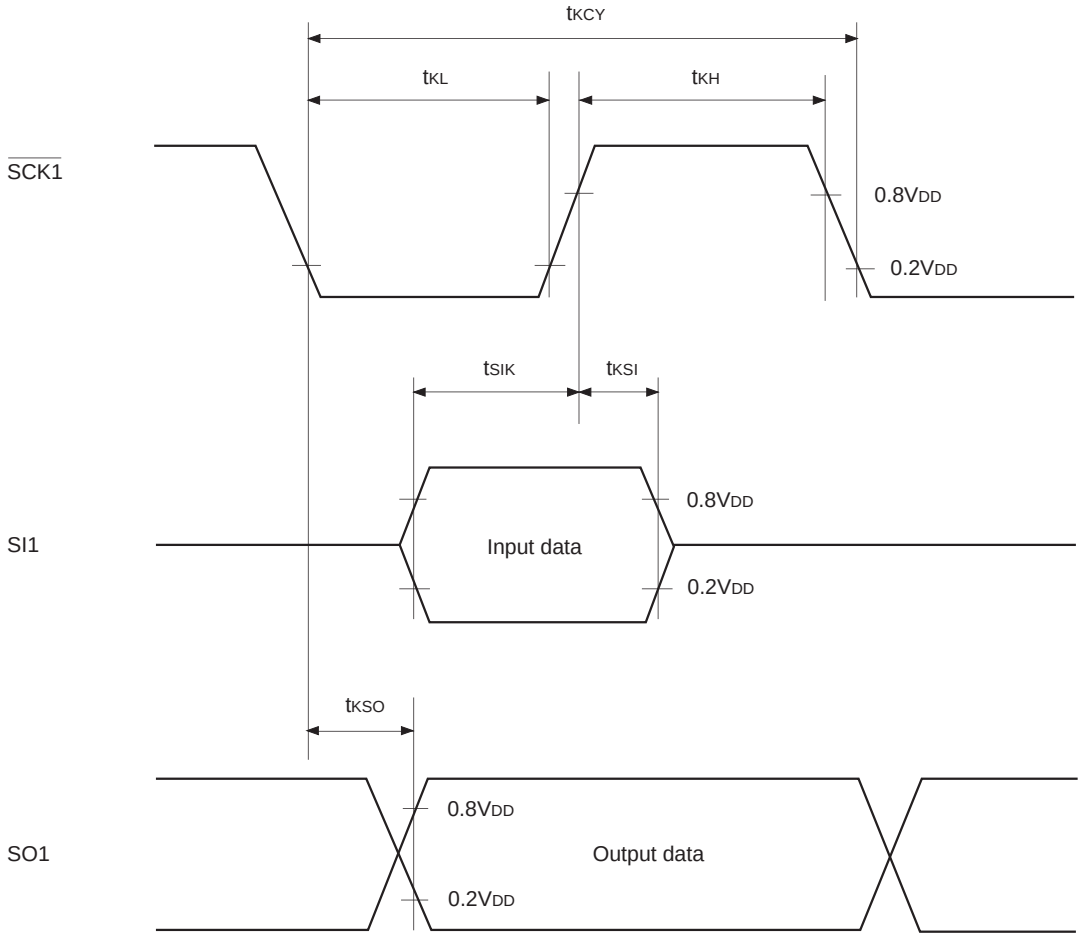
Serial transfer (CH1) (Ta = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	2tsys + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK1}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	tsys + 100		ns
			Output mode	4000/fc – 150		ns
SI1 input setup time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	tsys + 200		ns
			$\overline{SCK1}$ output mode	100		ns
SCK1 ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		tsys + 250	ns
			$\overline{SCK1}$ output mode		125	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)

Note 2) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing



(4) A/D converter characteristics

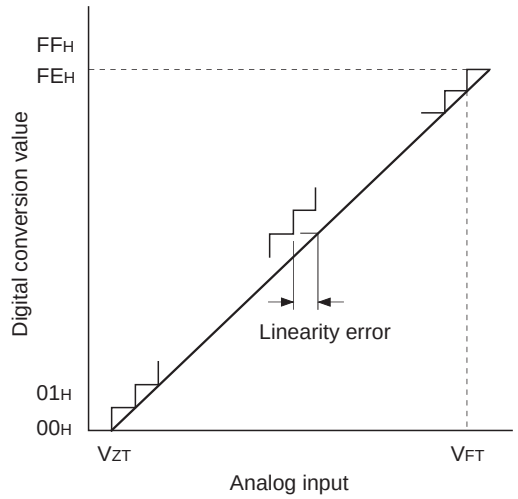
(Ta = –20 to +75°C, V_{DD} = AV_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC}*1			µs
Sampling time	t_{SAMP}			12/f_{ADC}*1			µs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD} = AV_{DD} = 4.5 to 5.5V	AV_{DD} – 0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		Sleep mode Stop mode 32kHz operating mode			10	µA

(Ta = –20 to +75°C, V_{DD} = AV_{DD} = 2.7 to 3.3V, AV_{REF} = 2.7 to AV_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 3.0V V_{SS} = AV_{SS} = 0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC}*1			µs
Sampling time	t_{SAMP}			12/f_{ADC}*1			µs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD} = AV_{DD} = 2.7 to 3.3V	AV_{DD} – 0.3		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.3	0.7	mA
	I_{REFS}		Sleep mode Stop mode 32kHz operating mode			10	µA

Fig. 6. Definitions of A/D converter terms



*1 The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).

When PS2 is selected, f_{ADC} = fc/2

When PS1 is selected, f_{ADC} = fc

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 2.7 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High and Low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{NMI}$ PJ0 to PJ7		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 7. Interruption input timing

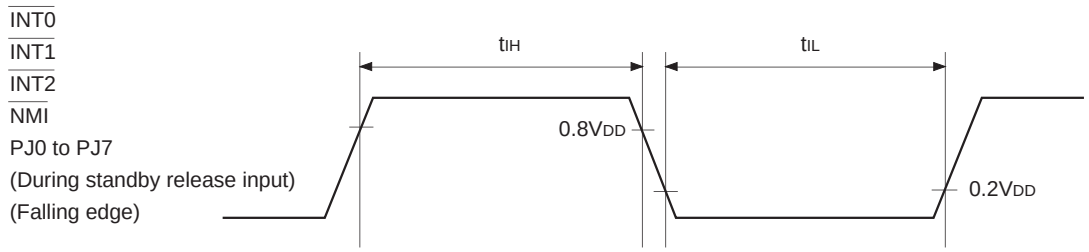
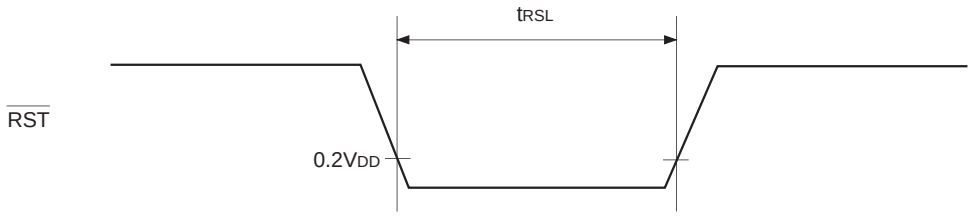


Fig. 8. Reset input timing

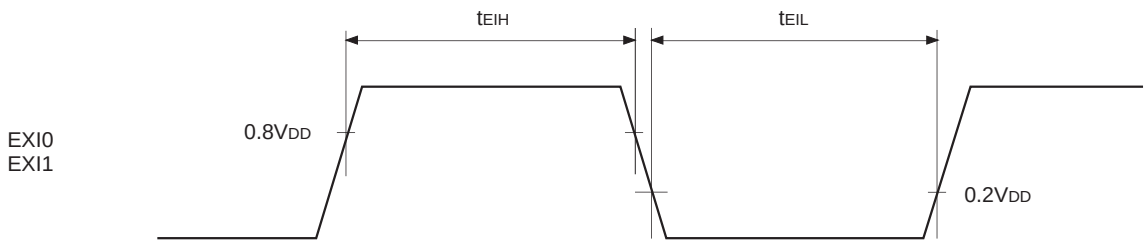


(5) Others (Ta = –20 to +75°C, V_{DD} = 2.7 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
EXI input High and Low level widths	t_{EIH} t_{EIL}	EXI0 EXI1	tsys = 2000/fc	$t_{FRC} \times 8 + 200 + t_{SYS}$		ns

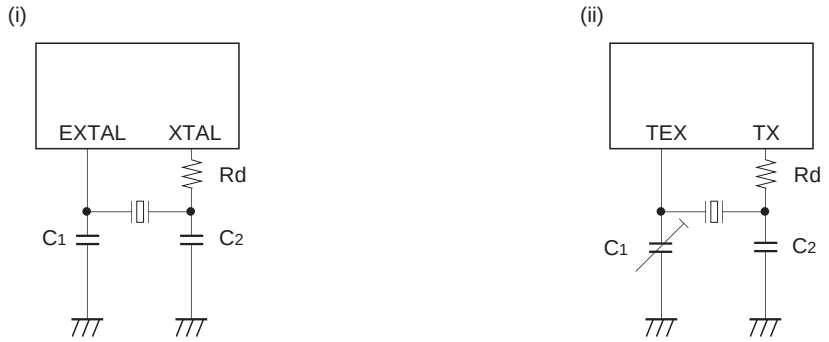
Note) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)
t_{FRC} = 1000/fc [ns]

Fig. 9. Other timings



Appendix

Fig. 10. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470K	(ii)
NIHON DENPA KOGYO CO., LTD	AT-51	20.00	2*1	2*1	0*1	(i)

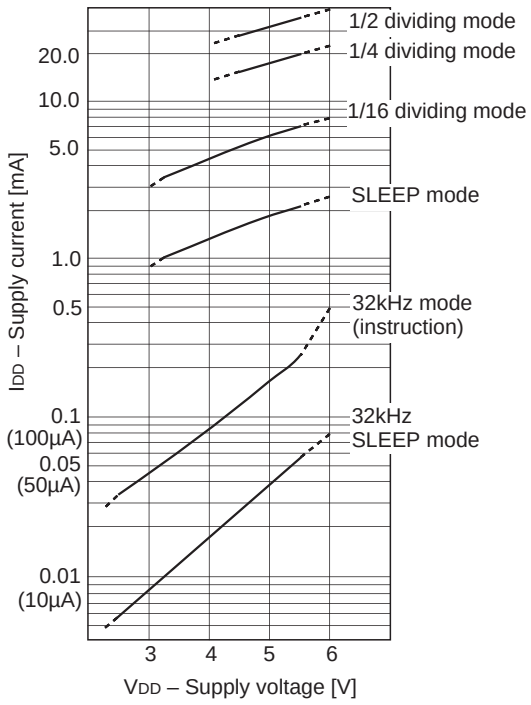
*1 Typical

Mask option table

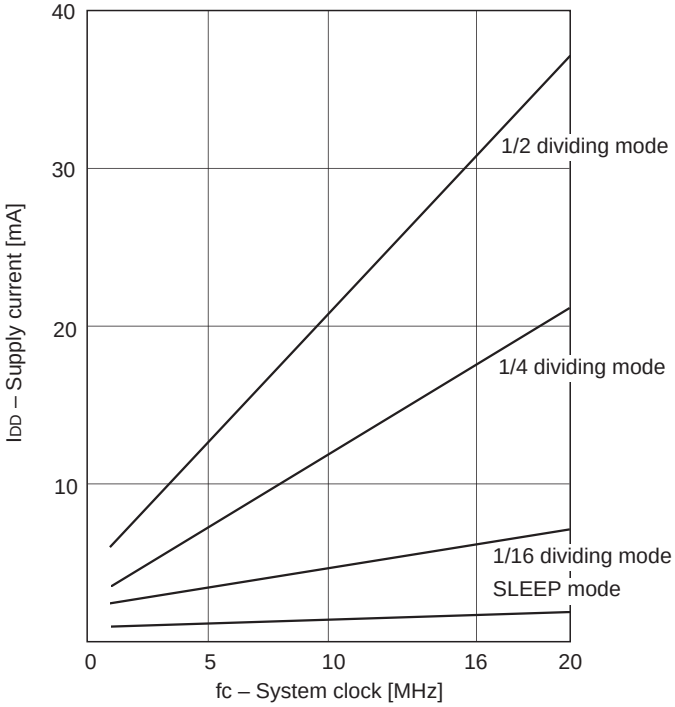
Item	Content	
Reset pin pull-up resistor	Non-existent	Existent

Characteristics Curve

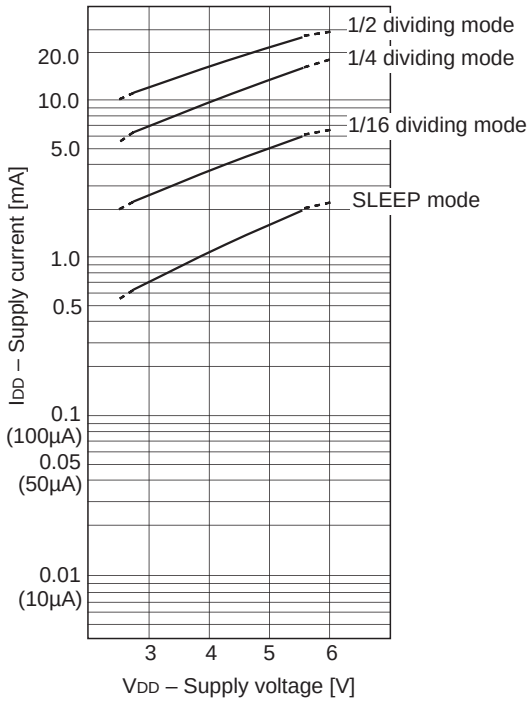
IDD vs. VDD
(fc = 16MHz, Ta = 25°C, Typical)



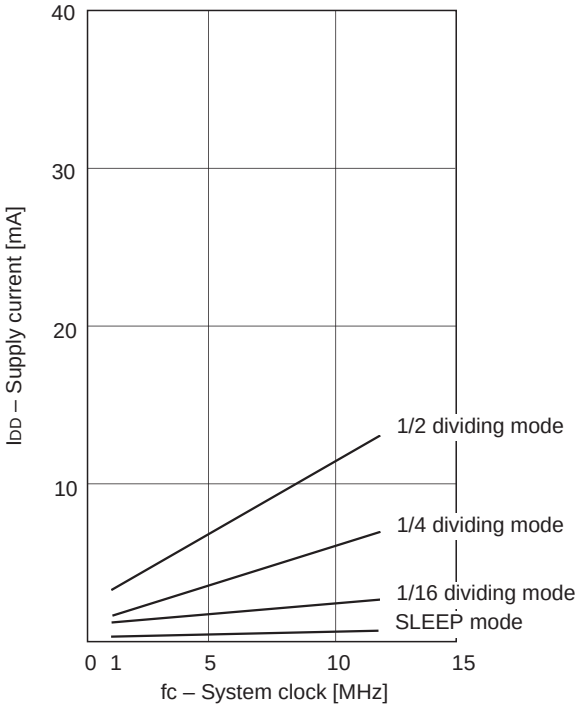
IDD vs. fc
(VDD = 5V, Ta = 25°C, Typical)



IDD vs. VDD
(fc = 12MHz, Ta = 25°C, Typical)

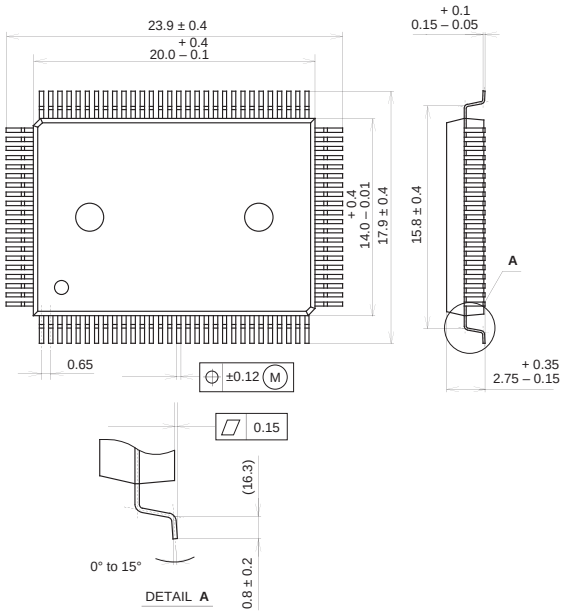


IDD vs. fc
(VDD = 3.0V, Ta = 25°C, Typical)



Package Outline Unit: mm

100PIN QFP (PLASTIC)

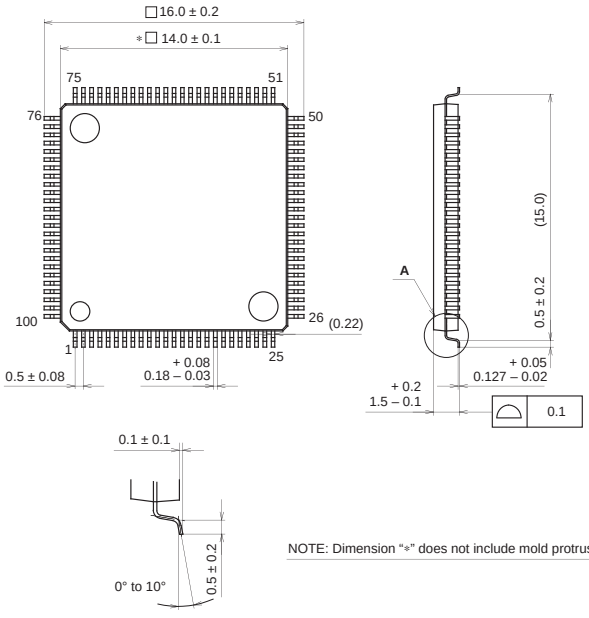


SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g

100PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	*QFP100-P-1414-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	————