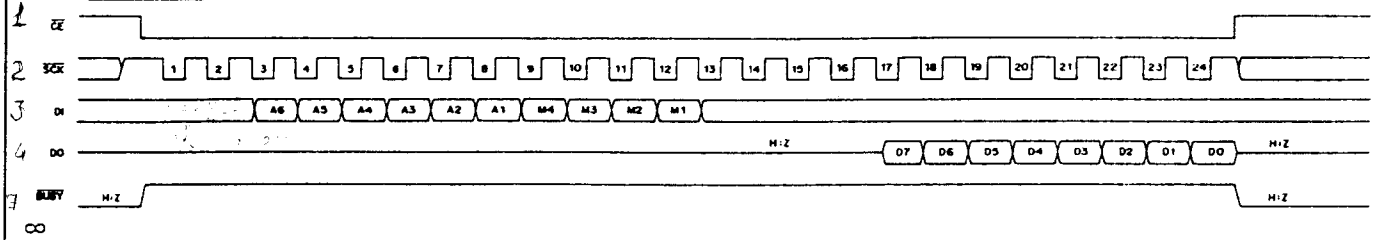
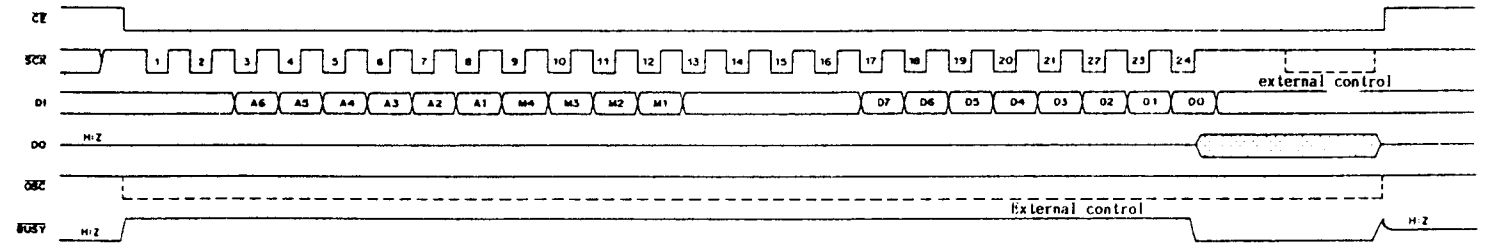
DR(DATA READ)



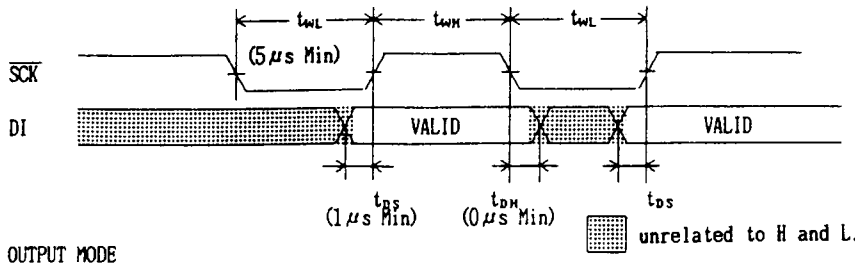
DW(DATA WRITE), ALDW(ALL BYTE DATA WRITE)



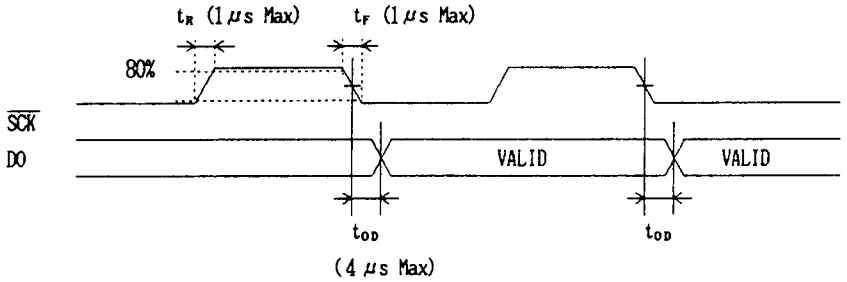
Undefined

Input/Output Timing Chart

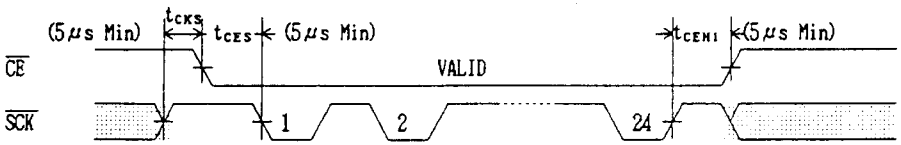
INPUT MODE



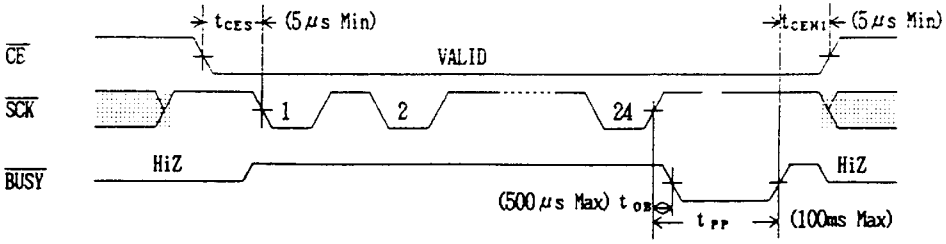
OUTPUT MODE



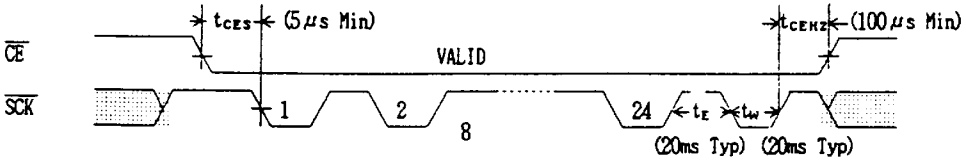
$\overline{CE}$ TIMING 1 (DR MODE)

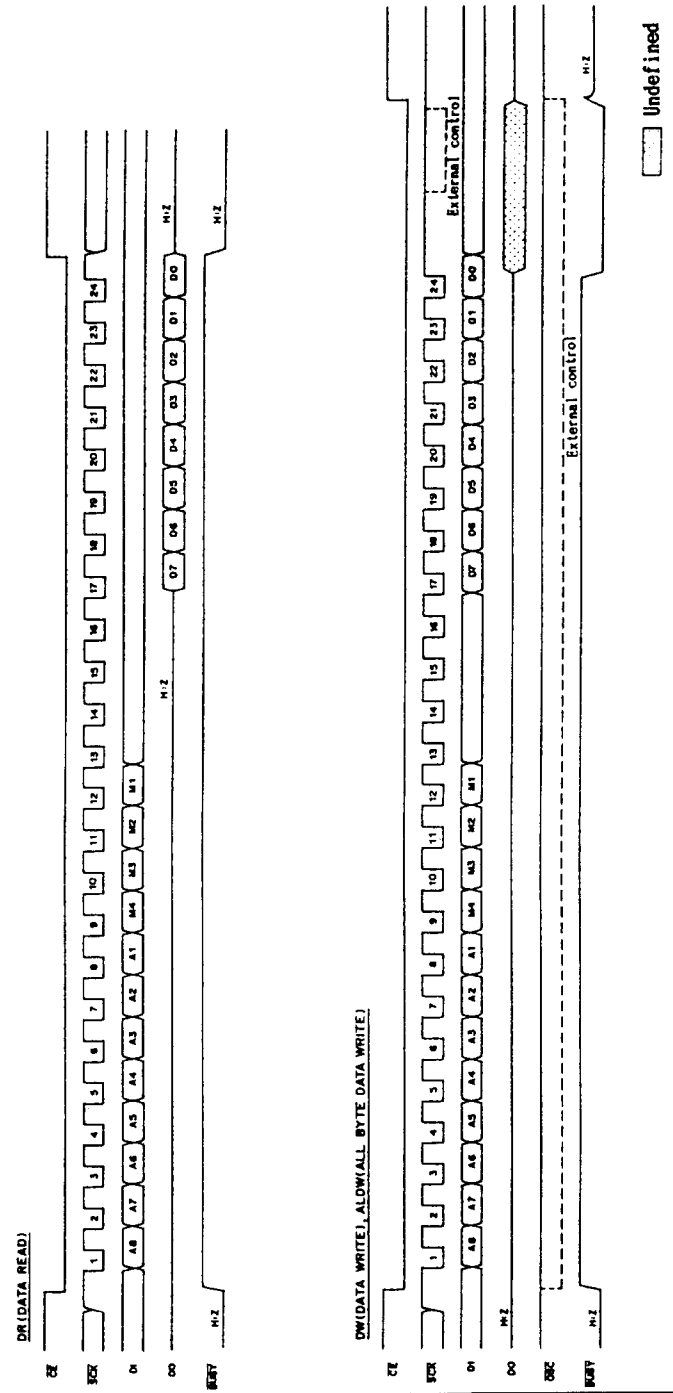


$\overline{CE}$ TIMING 2 (DW, ALDW MODE, INTERNAL TIMER)



$\overline{CE}$ TIMING 3 (DW, ALDW MODE, EXTERNAL CONTROL)





Electrical Characteristics 2.

(Ta=-40to+85℃, V_{CC} =5V±10%, GND=0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse width	t_{WH}		5			μs
Clock pulse width	t_{WL}		5			μs
Data input setup time	t_{DS}		1			μs
Data input hold time	t_{DH}		0			μs
Rise/Fall time	$t_{r,tf}$				1	μs
Chip enable setup time	t_{CES}		5			μs
Chip enable hold time 1	t_{CEH1}		5			μs
Chip enable hold time 2	t_{CEH2}		100			μs
Clock setup time	t_{CKS}		5			μs
Data delay time	t_{OD}	CL=100pF			4	μs
$\overline{BUSY}$ output delay time*3	t_{BD}	$\overline{BUSY}$, R=10kΩ			500	μs
Number of Read	N_R	Refresh period	10^7	10^9		time
Program time	t_{PP}	During internal timer usage *1		40	100	ms
Erasure time	t_E	During external control *2	16	20	100	ms
Write time	t_W	During external control *2	16	20	100	ms
Memory retention time 1	t_{MH1}	After rewritng 10^4times Store at Ta=85℃	10			year
Memory retention time 1	t_{MH2}	After rewritng 10^5times Store at Ta=85℃	1			year

*1. Indicates the value when Ta=25 ℃.

*2. Usage of ranges t_E to t_W (16mS to 100mS) presents no problems for Erasure ans Write in functions.

*3. See Fig.2.

Command Table

M4	M3	M2	M1	Operational Command
0	0	0	0	No operation
0	0	1	0	DW:Memory Write
0	1	0	0	ALDW:All byte write
0	1	1	0	Test mode ,Usage forbidden
1	0	0	0	No operation
1	0	1	0	DR:Memory Read
1	1	0	0	Test mode ,Usage forbidden
1	1	1	0	Test mode ,Usage forbidden
X	X	X	1	Test mode ,Usage forbidden

Description of Circuit Operations

1) Timing

At the rise time of Sync clock ($\overline{SCK}$),data is taken in from DL and with the fall time,data is output from DO. Input data should be stabilized,from $\overline{SCK}$ rise time and before 1μs.

2) DR:Data Read (Memory Read)

$\overline{CE}$ is set to L and then the first clock is input after 5μs.

By entering address data (A8 to A1) and mode data (M4 M3 M2 M1=1010),from the 17th clock and in syncronization with the fall time,D7 D6 through D0 are output in the respective order. When the rise time of the 24th clock has taken place,set $\overline{CE}$ to H after 5μs.

3) DW:Data Write (Memory Write)

$\overline{CE}$ is set to L and then the first clock is input after 5μs.

By entering Address data (A8 to A1),mode data rise time of the 24th clock,Erasure and Write are performed automatically.

As $\overline{BUSY}$ pin outputs L during ERASURE and WRITE following H output and after 5μs.

When $\overline{BUSY}$ pin is not in use,set $\overline{CE}$ to H after 100ms(Typ.Max.)

4) ALDW:All Byte Data Write

By entering Mode Data (M4 M3 M2 M1=0100),Write operation of the same data (D7 to D0)is carried out simultaneously to all addresses. CE timing and $\overline{BUSY}$ output are the same as in above article 3).

5) External control of Erasure and Write

Erasure and Write pulses are generated by the built-in C and R.

However,external control is also possible.

By setting $\overline{OSC}$ pin to L in DW or ALDW modes, Erasure and Write control are possible through the usage of $\overline{SCK}$ pin.

Erasure is carried out during CE(20ms Typ.)and Write during t_W(20ms Typ.).

By setting $\overline{SCK}$ pin to H after the lapse of actual completion takes place about 50μs after the pulse generation. (50μs Typ., 100μs Max.)

At that time $\overline{BUSY}$ pin changes from L to H. Over 5μs after it has turned to H, set $\overline{CE}$ pin to H. When $\overline{BUSY}$ pin is not in use,after $\overline{SCK}$ pin has turned from L to H(t_W)by over 100μs set $\overline{CE}$ to H.