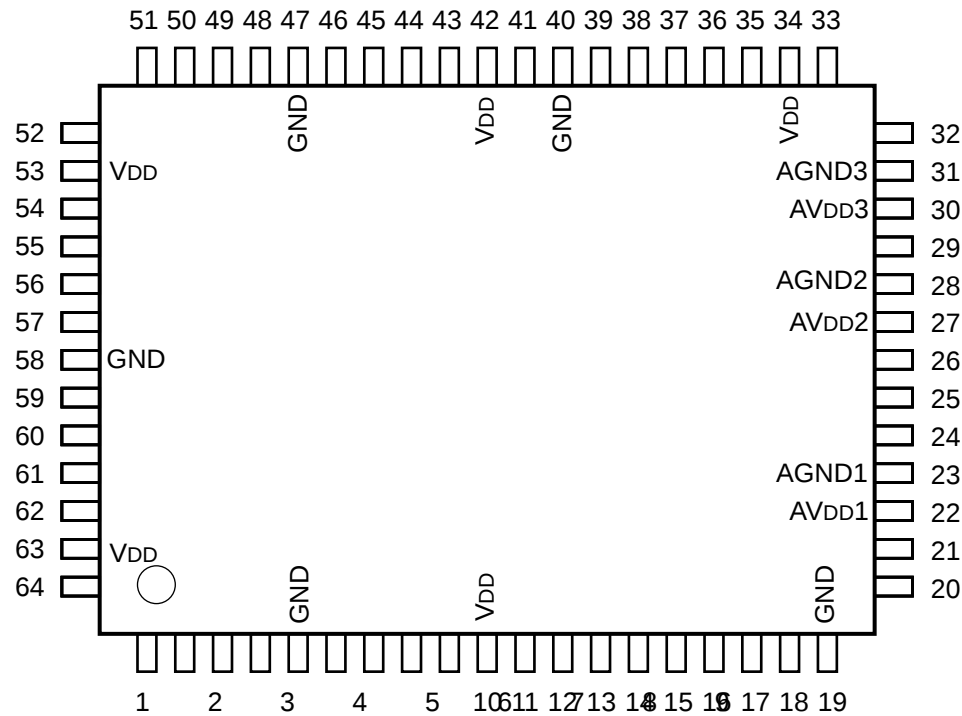

DIGITAL VIDEO ENCODER
-TOP VIEW-



(AVDD1 to 3 = +3.3 to 5V, VDD = +3.3 to 5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	PD7	17	I/O	PD9/TD1	33	I/O	TD10	49	I	SCK/SCL
2	I	PD6	18	I/O	PD8/TD0	34	-	VDD	50	I	XCS/SA
3	I	PD5	19	-	GND	35	I/O	TD9	51	I	XVRST
4	I	PD4	20	I	IREF	36	I/O	TD8	52	I	FI
5	-	GND	21	I	VREF	37	I	XTEST1	53	-	VDD
6	I	PD3	22	-	AVDD1	38	I	XTEST2	54	I	XTEST4
7	I	PD2	23	-	AGND1	39	I	XTEST3	55	I	XRST
8	I	PD1	24	O	COMP-O/V	40	-	GND	56	I	SYSCLK
9	I	PD0	25	O	VB	41	I	TRST	57	O	PDCLK
10	-	VDD	26	O	VG	42	-	VDD	58	-	GND
11	I/O	PD15/TD7	27	-	AVDD2	43	I	TDI	59	O	VSYN
12	I/O	PD14/TD6	28	-	AGND2	44	I	TMS	60	O	HSYN
13	I/O	PD13/TD5	29	O	Y-OUT/Y	45	I	TCK	61	O	SO
14	I/O	PD12/TD4	30	-	AVDD3	46	O	TDO	62	O	FID
15	I/O	PD11/TD3	31	-	AGND3	47	-	GND	63	-	VDD
16	I/O	PD10/TD2	32	O	C-OUT/U	48	I	SI/SDA	64	I	XIICEN

INPUT

FI ; FIELD ID INPUT
IREF ; REFERENCE CURRENT INPUT
PD0-15 ; PIXEL DATA INPUTS
SI/SDA ; SERIAL DATA INPUT
SCK/SCL ; SERIAL CLOCK INPUT
SYSCLK ; SYSTEM CLOCK INPUT
TCK ; CLOCK INPUT FOR JTAG
TDI ; SERIAL DATA INPUT FOR JTAG
TMS ; CONTROL SIGNAL INPUT FOR JTAG
TRST ; RESET SIGNAL INPUT FOR JTAG
VREF ; REFERENCE VOLTAGE INPUT
XCS/SA ; CHIP SELECT INPUT
XIICEN ; SERIAL INTERFACE MODE SELECT INPUT
XRST ; SYSTEM RESET INPUT
XTEST1-4 ; TEST MODE CONTROL INPUTS
XVRST ; V-SYNC RESET INPUT

OUTPUT

COMP-O/V ; COMPOSITE/V D/A CONVERTER OUTPUT
C-OUT/U ; CHROMA/U D/A CONVERTER OUTPUT
FID ; FIELD ID OUTPUT
HSYNC ; H SYNC OUTPUT
PDCLK ; PIXEL DATA CLOCK OUTPUT FOR 13.5MHz
SO ; SERIAL OUTPUT
TDO ; SERIAL DATA OUTPUT FOR JTAG
VB,VG ; EXTERNAL CAPACITOR TERMINAL
VSYNC ; V SYNC OUTPUT
Y-OUT/Y ; Y D/A CONVERTER OUTPUT

INPUT/OUTPUT

TD0-10 ; TEST DATA BUS

