SONY

CXA2064M

US Audio Multiplexing Decoder

Description

The CXA2064M is an IC designed as a decoder for the Zenith TV Multi-channel System. Functions include stereo demodulation, SAP (Separate Audio Program) demodulation, dbx noise reduction.

Features

- Adjustment free of VCO and filter.
- Audio multiplexing decoder and dbx noise reduction decoder are all included in a single chip. Almost any sort of signal processing is possible through this IC.
- Various built-in filter circuits greatly reduce external parts.
- This IC is near pin to pin compatible with the CXA2020M.

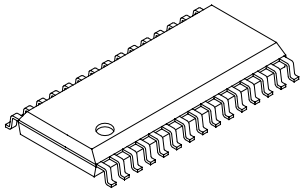
Applications

TV, VCR and other decoding systems for US audio multiplexing TV broadcasting

Structure

Bipolar silicon monolithic IC

30 pin SOP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	11	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1000	mW
• STID, SAPID drive current	I_O	2 (max.)	mA

Range of Operating Supply Voltage

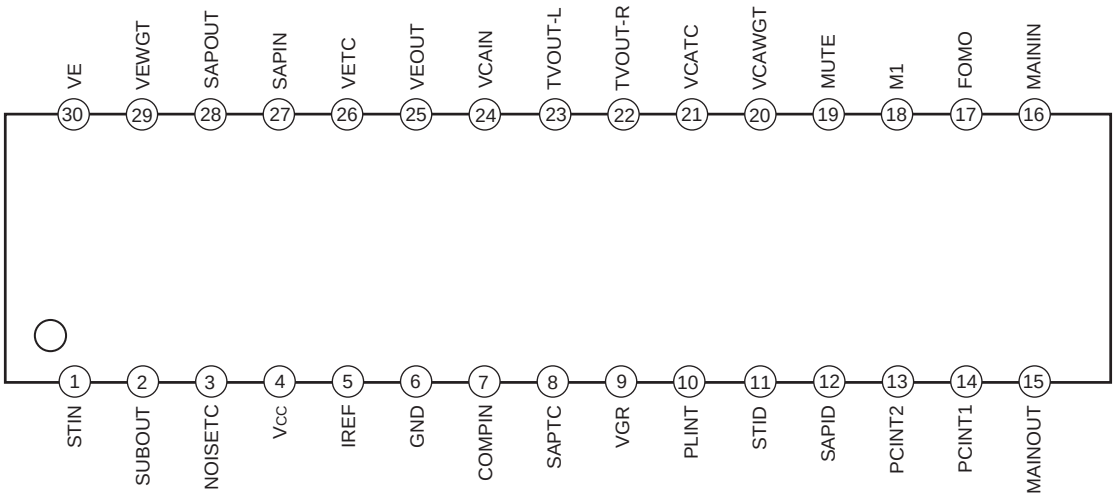
9 ± 0.5 V

* This device is available only to the licensees of the dbx-TV noise reduction system.

Standard I/O Level

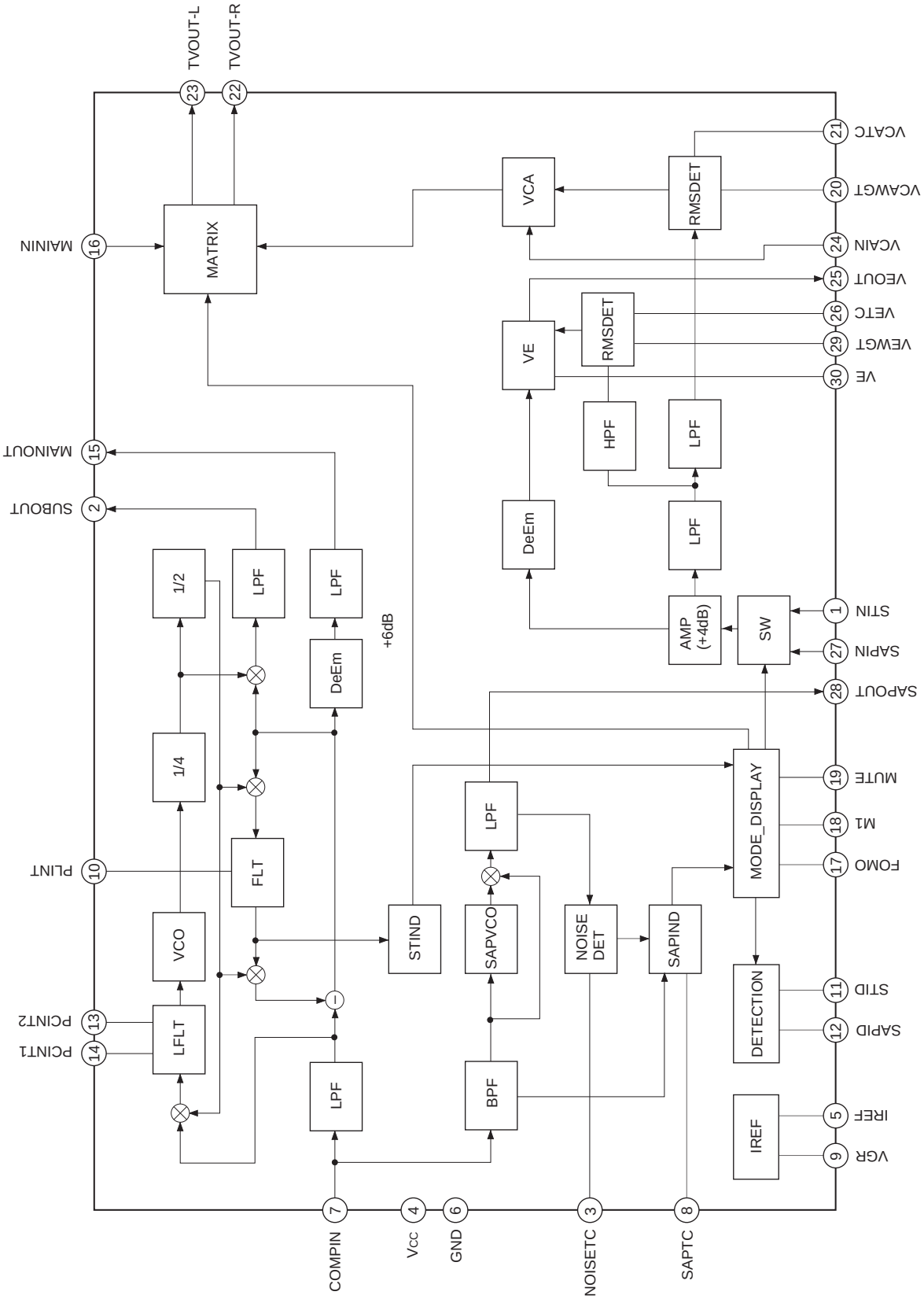
- Input level
  COMPIN (Pin 7) 100mVrms (MONO 100Hz 100% mod.)
- Output level
  TVOUT-L/R (Pins 23 and 22) 490mVrms (MONO 100Hz 100% mod.)

Pin Configuration (Top View)

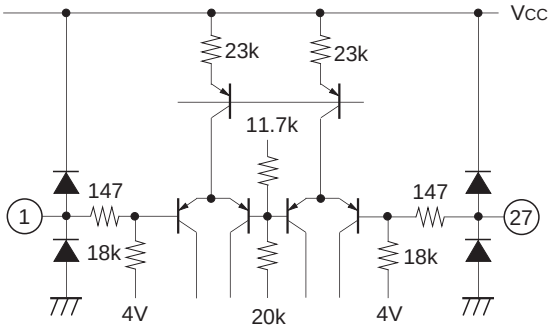
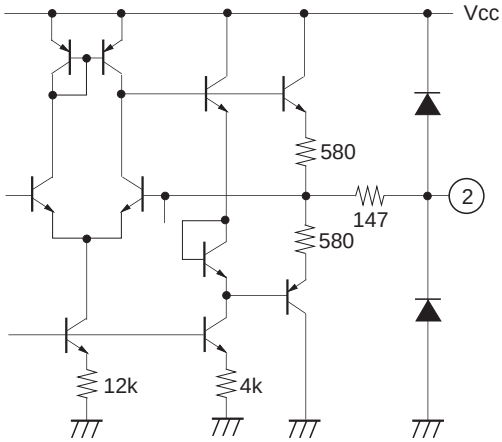
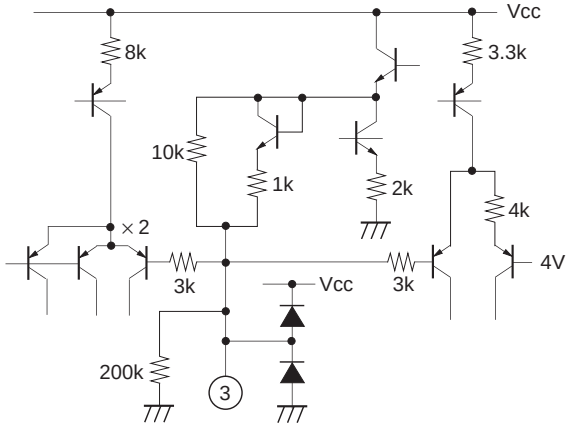
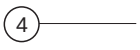


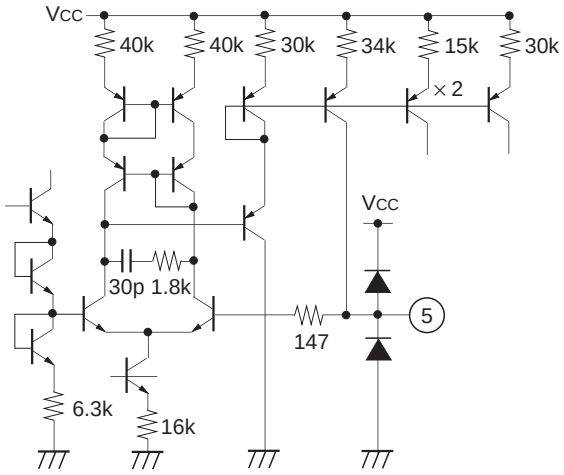
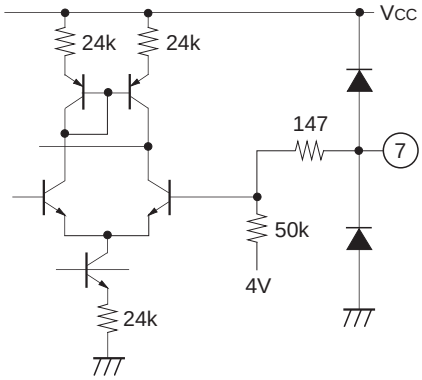
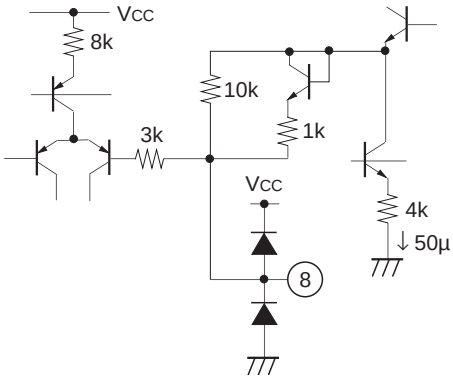
E98513-PS

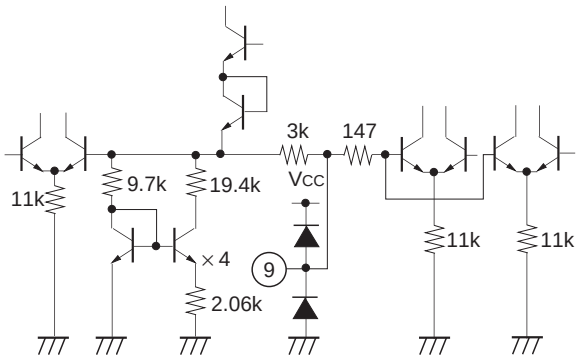
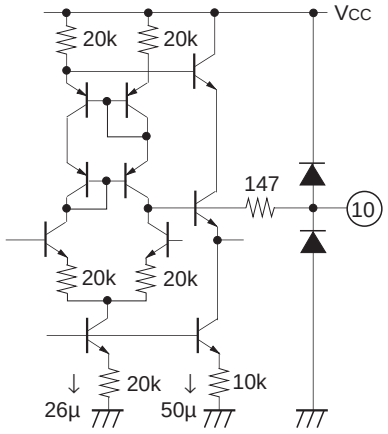
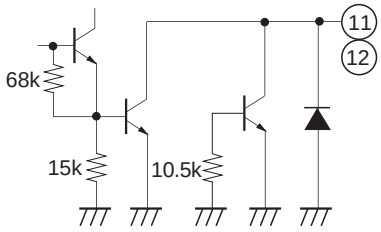
Block Diagram

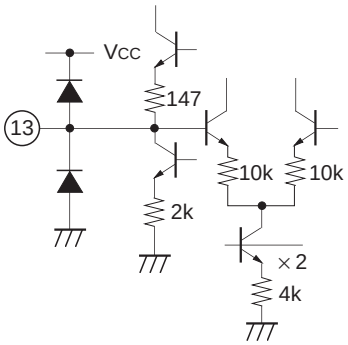
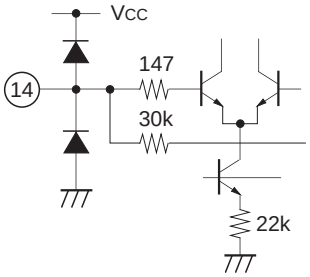
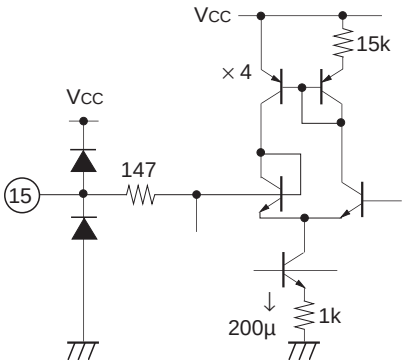
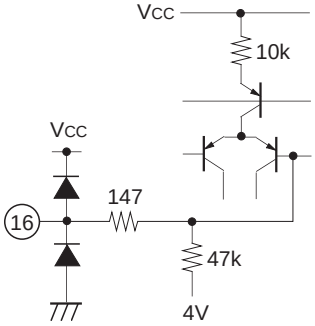
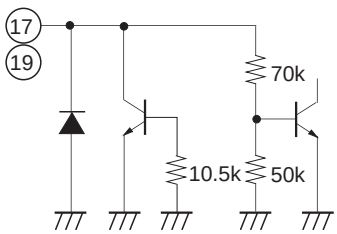


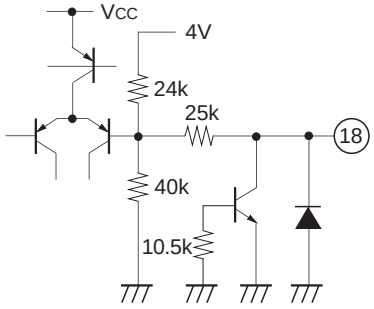
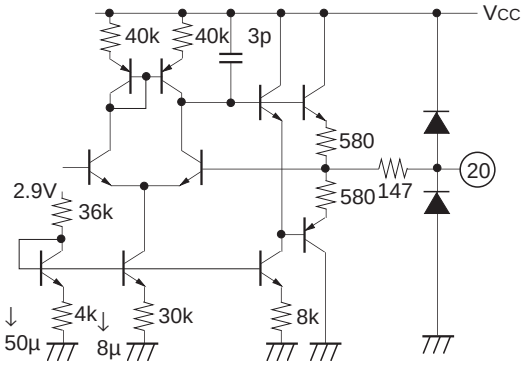
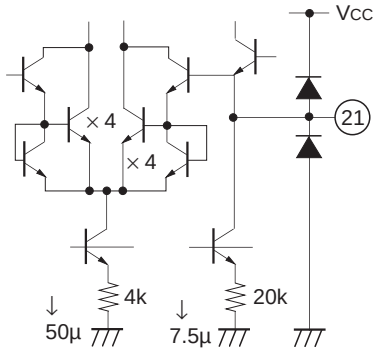
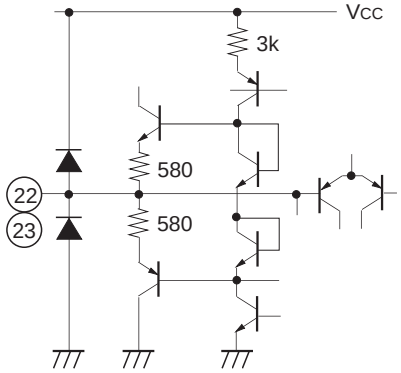
Pin Description (Ta = 25°C, Vcc = 9V)

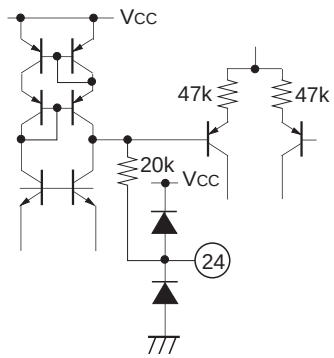
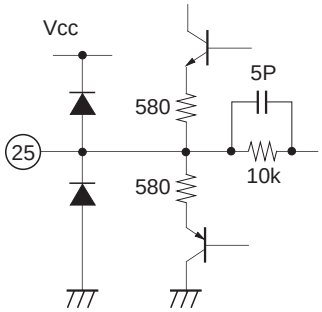
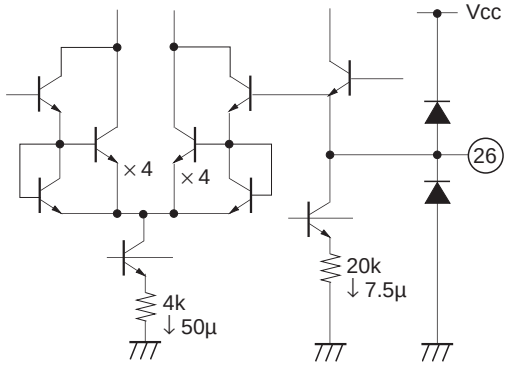
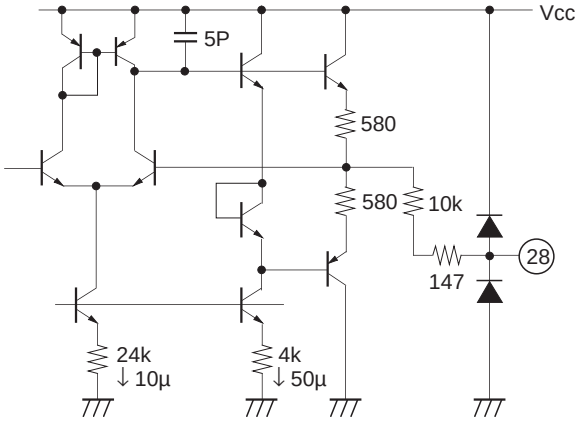
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	STIN	4.0V		Input the (L-R) signal from SUBOUT (Pin 2).
27	SAPIN	4.0V		Input the (SAP) signal from SAPOUT (Pin 28).
2	SUBOUT	4.0V		(L–R) signal output pin.
3	NOISETC	3.0V		Set the time constant for the noise detection circuit. (Connect a 4.7µF capacitor between this pin and GND.)
4	Vcc	—		Supply voltage pin.

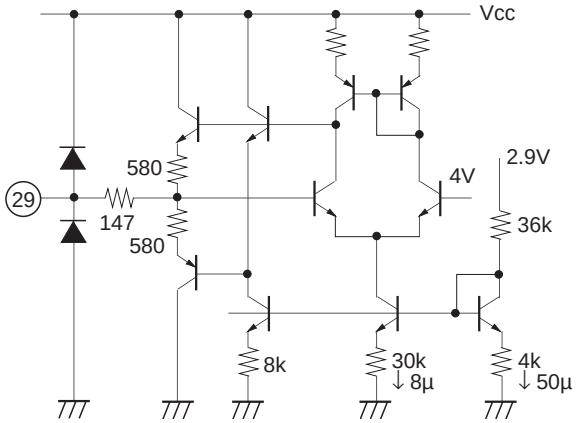
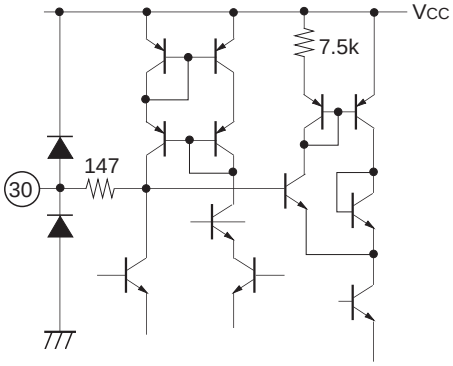
Pin No.	Symbol	Pin voltage	Eqivalent circuit	Description
5	IREF	1.3V		Set the filter and VCO reference current. (Connect a 68kΩ (±1%) resistor between this pin and GND.)
6	GND	—		Analog block GND.
7	COMPIN	4.0V		Audio multiplexing signal input pin.
8	SAPTC	4.5V		Set the time constant for the SAP carrier detection circuit. (Connect a 4.7µF capacitor between this pin and GND.)

Pin No.	Symbol	Pin voltage	Eqivalent circuit	Description
9	VGR	1.3V		Band gap reference output pin. (Connect a 10µF capacitor between this pin and GND.)
10	PLINT	5.1V		Pilot cancel circuit loop filter integrating pin. (Connect a 1µF capacitor between this pin and GND.)
11	STID	—		Stereo detection pin. Open collector output. Drive current is 2mA (Max.).
12	SAPID	—		SAP detection pin. Open collector output. Drive current is 2mA (Max.).

Pin No.	Symbol	Pin voltage	Eqivalent circuit	Description
13	PCINT2	4.0V		Stereo block PLL loop filter integrating pin.
14	PCINT1	4.0V		
15	MAINOUT	4.0V		(L + R) signal output pin.
16	MAININ	4.0V		Input the (L + R) signal from MAINOUT (Pin 15).
17	FOMO	—		Mode control switch pin. This pin has 3 ranges for input voltage. Sets forced monoral mode and also control ST.ID.
19	MUTE	—		Mode control switch pin. When this pin is set to H level, TVOUT output is muted.

Pin No.	Symbol	Pin voltage	Eqivalent circuit	Description
18	M1	—		Mode control switch pin. This pin has 3 ranges for input voltage. Stereo, BOTH, SAP selection are available.
20	VCAWGT	4.0V		Weight the VCA control effective value detection circuit. (Connect a 1µF capacitor and a 3.9kΩ resistor in series between this pin and GND.)
21	VCATC	1.7V		Determine the restoration time constant of the VCA control effective value detection circuit. (the specified restoration time constant can be obtained by connecting a 10µF capacitor between this pin and GND.)
22	TVOUT-R	4.0V		TVOUT right channel output pin.
23	TVOUT-L	4.0V		TVOUT left channel output pin.

Pin No.	Symbol	Pin voltage	Eqivalent circuit	Description
24	VCAIN	4.0V		VCA input pin. Input the variable de-emphasis output signal from Pin 25 via a coupling capacitor.
25	VEOUT	4.0V		Variable de-emphasis output pin. (Connect a 4.7µF non-polar capacitor between Pins 25 and 24.)
26	VETC	1.7V		Determine the restoration time constant of the variable de-rmphasis control effective value detection circuit. (the specified restoration time constant can be obtained by connecting a 3.3µF capacitor between this pin and GND.)
28	SAPOUT	4.0V		SAP FM detector output pin.

Pin No.	Symbol	Pin voltage	Eqivalent circuit	Description
29	VEWGT	4.0V		Weight the variable de-emphasis control effective value detection circuit. (Connect a 0.047µF capacitor and a 3kΩ resistor in series between this pin and GND.)
30	VE	4.0V		Variable de-emphasis integrating pin. (Connect a 2700pF capacitor and a 3.3kΩ resistor in series between this pin and GND.)

Electrical Characteristics

COMPIN input level
(100% modulation level)

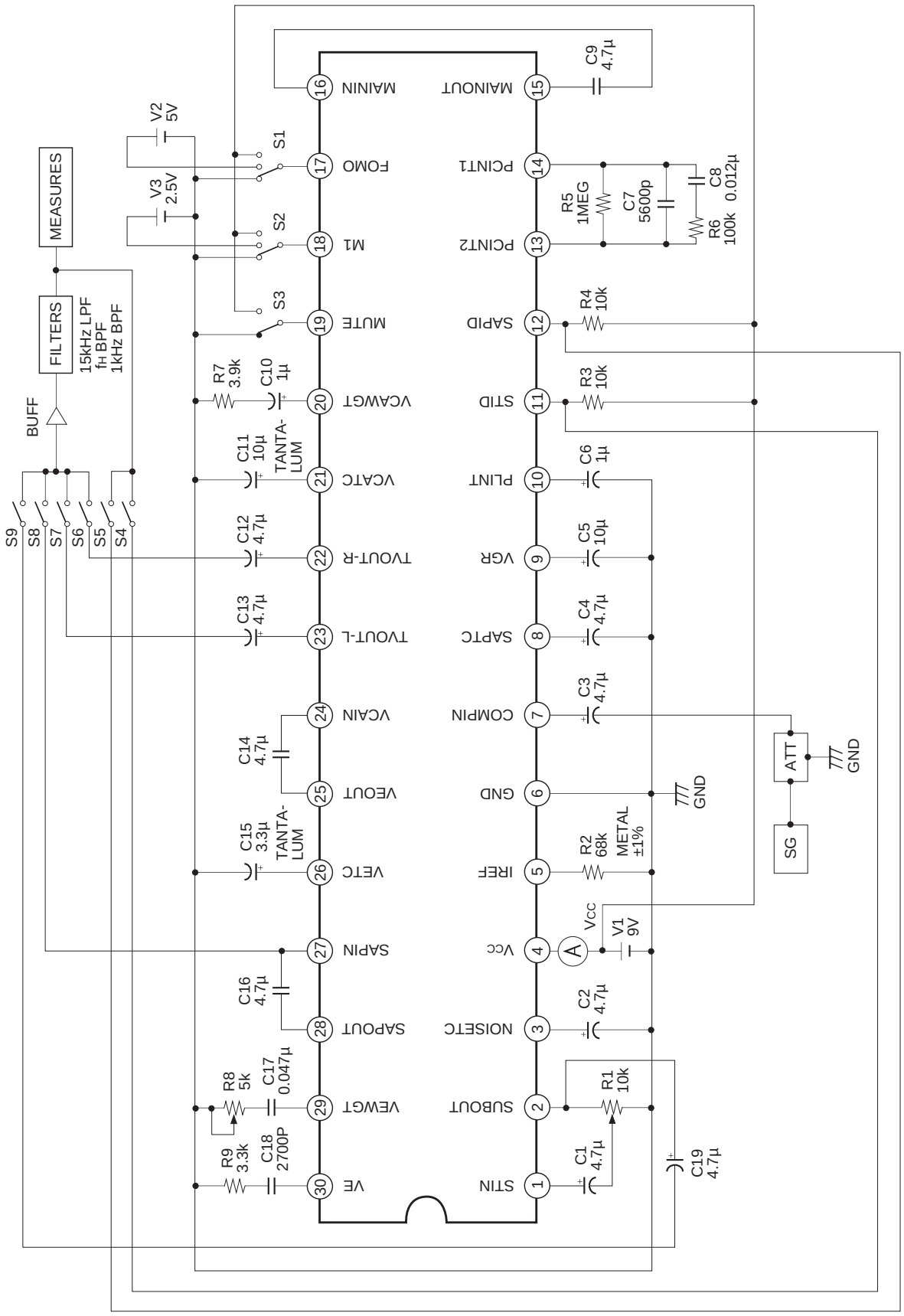
Main (L + R) (Pre-Emphasis: OFF) = 100mVrms
SUB (L – R) (dbx-TV: OFF) = 200mVrms
Pilot= 20mVrms
SAP Carrier= 60mVrms
f_H = 15.734kHz

(Ta = 25°C, V_{CC} = 9V)

No.	Item	Signal	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
1	Current consumption	Icc		—	No signal				15	23	31	mA
2	Main output level	Vmain	MONO	7	Mono 1kHz 100% mod. Pre-em. ON			22/23	440	490	540	mVrms
3	Main de-emphasis frequency characteristic	FCdeem	MONO	7	Mono 5kHz 30% mod. Pre-em. ON	20 log ('5k'/'1k')		22/23	–1.2	0	1.0	dB
4	Main LPF frequency characteristic	FCmain	MONO	7	Mono 12kHz 30% mod. Pre-em. ON	20 log ('12k'/'1k')		22/23	–3.0	–1.0	1.0	dB
5	Main distortion	THDm	MONO	7	Mono 1kHz 100% mod. Pre-em. ON		15kLPF	22/23	—	0.1	0.5	%
6	Main overload distortion	THDmmax	MONO	7	Mono 1kHz 200% mod. Pre-em. ON		15kLPF	22/23	—	0.15	0.5	%
7	Main S/N	SNmain	MONO	7	Mono 1kHz, Pre-em. ON	20 log ('100%'/'0%')	15kLPF	22/23	61	69	—	dB
8	Sub output level	Vsub	ST	7	SUB (L-R) 1kHz, 100% mod., NR OFF			2	225	275	325	mVrms
9	Sub LPF frequency characteristic	FCsub	ST	7	SUB (L-R) 12kHz, 30% mod., NR OFF	20 log ('12k'/'1k')		2	–3.0	–0.5	1.0	dB
10	Sub distortion	THDsub	ST	7	SUB (L-R) 1kHz, 100% mod., NR OFF		15kLPF	2	—	0.1	1.0	%
11	Sub overload distortion	THDsmax	ST	7	SUB (L-R) 1kHz, 200% mod., NR OFF		15kLPF	2	—	0.2	2.0	%
12	Sub S/N	SNsub	ST	7	SUB (L-R) 1kHz, NR OFF	20 log ('100%'/'0%')	15kLPF	2	56	64	—	dB
13	ST → SAP Crosstalk	CTst	SAP	7	SUB (L-R) 1kHz, 100% mod., NR ON, SAP Carrier (5f_H)	20 log ('M1 = L'/ 'M1 = H')	1kBPF	23	60	70	—	dB
14	Sub pilot leak	PCsub	ST	7	PILOT (f_H) 0dB	0dB = 20mVrms	f_H BPF	2	—	–27	–16	dB

No.	Item	Signal	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
15	Stereo ON level	THst	ST	7	Change PILOT (f_H) Level	0dB = 20mVrms		11	–9.0	–6.0	–3.0	dB
16	Stereo ON/OFF hysteresis	HYst				20 log (‘on level'/'off level')		11	2.0	6.0	10.0	dB
17	SAP output level	Vsap	SAP	7	SAP 1kHz 100% mod. NR OFF			28	130	170	210	mVrms
18	SAP LPF frequency characteristic	FCsap	SAP	7	SAP 10kHz 30% mod. NR OFF	20 log ('10k'/'1k')		28	–3.0	0	2.5	dB
19	SAP distortion	THDsap	SAP	7	SAP 1kHz 100% mod. NR OFF		15kLPF	28	—	2.5	6.0	%
20	SAP S/N	SNsap	SAP	7	SAP 1kHz, NR OFF	20 log ('100%'/'0%')	15kLPF	28	46	55	—	dB
21	SAP → ST Cross talk	CTsap	ST	7	SAP 1kHz 100% mod. NR ON, Pilot (f_H)	20 log ('M1 = H'/ 'M1 = L')	1kBPF	23	60	70	—	dB
22	SAP ON level	THsap	SAP	7	Change SAP Carrier ($5f_H$) Level	0dB = 60mVrms		12	–12.0	–9.0	–6.5	dB
23	SAP ON/OFF hysteresis	HYsap				20 log (‘on level’/’off level’)		12	2.0	4.0	6.0	dB
24	ST separation 1 L → R	STLsep1	ST	7	ST-L 300Hz 30% mod. NR ON	20 log ('Lch'/'Rch')	15kLPF	22/23	23	35	—	dB
25	ST separation 1 R → L	STRsep1	ST	7	ST-R 300Hz 30% mod. NR ON	20 log ('Rch'/'Lch')	15kLPF	22/23	23	35	—	dB
26	ST separation 2 L → R	STLsep2	ST	7	ST-L 3kHz 30% mod. NR ON	20 log ('Lch'/'Rch')	15kLPF	22/23	23	35	—	dB
27	ST separation 2 R → L	STRsep2	ST	7	ST-R 3kHz 30% mod. NR ON	20 log ('Rch'/'Lch')	15kLPF	22/23	23	35	—	dB

Electrical Characteristics Measurement Circuit



Adjustment Method

1. Input level adjustment
   1) Connect components as shown in Fig. 1.
   2) Set the US MPX encoder output to MONO 100Hz 100% modulation.
   3) Adjust the "ATT" so that COMPIN (Pin 7) level goes to 100mVrms (±0.5dB).

2. Separation adjustment
   1) Mode control pin are set to FOMO (Pin 17): L, M1 (Pin 18): L, MUTE (Pin 19): L.
   2) Set the US MPX encoder ouput to Stereo Lch-only 300Hz 30% modulation, NR-ON.
      Then, adjust the variable resistor of SUBOUT (Pin 2) to reduce the TVOUT-R output to the minimum.
   3) Next, set the frequency only of the input signal to 3kHz and adjust the variable resistor of VEWGT (Pin 29) to reduce the TVOUT-R output to the minimum.
   4) The adjustments in 2 and 3 above are performed to optimize the separation.

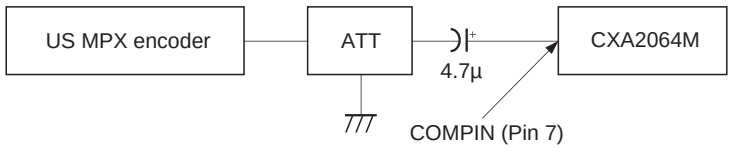


Fig. 1. Adjustment setup

* Adjust this IC through Tuner and IF when this IC is mounted on the set.

Description of Operation

The US audio multiplexing system possesses the base band spectrum shown in Fig. 2.

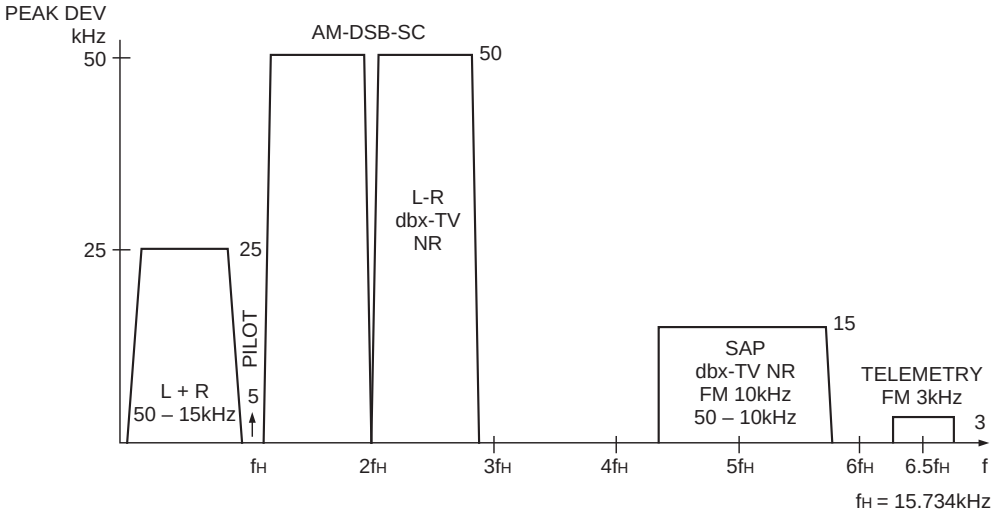


Fig. 2. Base band spectrum

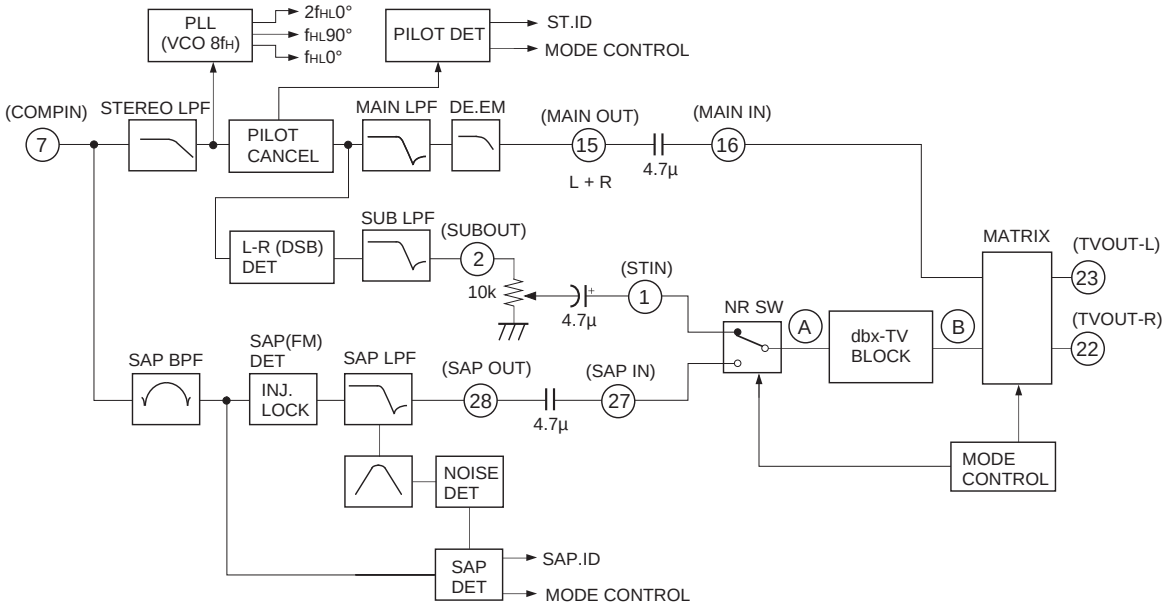


Fig. 3. Overall block diagram (See Fig. 4 for the dbx-TV block)

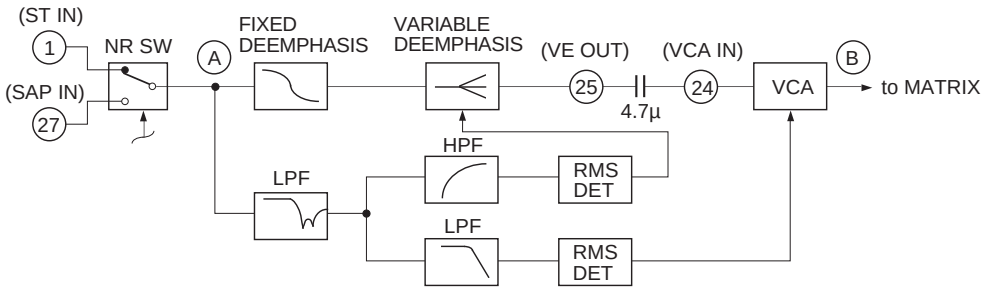


Fig 4. dbx-TV block

(1) L + R (MAIN)

When the audio multiplexing signal is inputted to COMPIN (Pin 7), the SAP signal and telemetry signal are suppressed by STEREO LPF. Next, the pilot signals are canceled. Finally, the L – R signal and SAP signal are removed by MAIN LPF, and frequency characteristics are flattened (de-emphasized) and input to the matrix.

(2) L – R (SUB)

The L – R signal follows the same course as L + R before the pilot signal is canceled. L – R has no carrier signal, as it is a suppressed-carrier double-sideband amplitude modulated signal (DSB-AM modulated). For this reason, the pilot signal is used to regenerate the carrier signal (quasi-sine wave) to be used for the demodulation of the L – R signal. In the last stage, the residual high frequency components are removed by SUB LPF and the L – R signal is input to the dbx-TV block via the NRSW circuit.

(3) SAP

SAP is an FM signal using $5f_H$ as a carrier as shown in the Fig. 2. First, the SAP signal only is extracted using SAP BPF. Then, this is subjected to FM detection. Finally, residual high frequency components are removed and frequency characteristics flattened using SAP LPF, and the SAP signal is input to the dbx-TV block via the NRSW circuit.

(4) Mode discrimination

Stereo discrimination is performed by detecting the pilot signal amplitude. SAP discrimination is performed by detecting the $5f_H$ carrier amplitude. NOISE discrimination is performed by detecting the noise near 25kHz after FM detection of SAP signal.

(5) dbx-TV block

Either the L – R signal or SAP signal input respectively from STIN (Pin 1) or SAPIN (Pin 27) is selected by the mode control and input to the dbx-TV block.

The input signal then passes through the fixed de-emphasis circuit and is applied to the variable de-emphasis circuit. The signal output from the variable de-emphasis circuit passes through an external capacitor and is applied to VCA (voltage control amplifier). Finally, the VCA output is converted from a current to a voltage using an operational amplifier and then input to the matrix.

The variable de-emphasis circuit transmittance and VCA gain are respectively controlled by Each of effective value detection circuits. Each of the effective value detection circuits passes the input signal through a predetermined filter for weighting before the effective value of the weighted signal is detected to provide the control signal.

(6) Matrix

The signals (L + R, L – R, SAP) input to “MATRIX” become the outputs for the ST-L, ST-R, MONO and SAP signals according to the mode control and whether there is ST / SAP discrimination.

(7) Others

“Bias” supplies the reference voltage and reference current to the other blocks. The current flowing to the resistor connecting IREF (Pin 5) with GND become the reference current.

Decoder Output and Mode Control Table

Input signal mode	ID		Pin		dbx input	Output	
	ST	SAP	M1	FOMO		Lch	Rch
MONO	H	H	L	*	MUTE	L + R	L + R
	H	H	M	*	MUTE	L + R	L + R
	H	H	H	*	MUTE	L + R	L + R
STEREO	L	H	L	L	L – R	L	R
	L	H	L	M	MUTE	L + R	L + R
	H	H	L	H	MUTE	L + R	L + R
	L	H	M	L	MUTE	L + R	L + R
	L	H	M	M	MUTE	L + R	L + R
	H	H	M	H	MUTE	L + R	L + R
	L	H	H	L	L – R	L	R
	L	H	H	M	MUTE	L + R	L + R
	H	H	H	H	MUTE	L + R	L + R
MONO & SAP	H	L	L	*	MUTE	L + R	L + R
	H	L	M	*	SAP	L + R	SAP
	H	L	H	L	SAP	SAP	SAP
	H	L	H	M	SAP	L + R	SAP
	H	L	H	H	SAP	L + R	SAP
STEREO & SAP	L	L	L	L	L – R	L	R
	L	L	L	M	MUTE	L + R	L + R
	H	L	L	H	MUTE	L + R	L + R
	L	L	M	L	SAP	L + R	SAP
	L	L	M	M	SAP	L + R	SAP
	H	L	M	H	SAP	L + R	SAP
	L	L	H	L	SAP	SAP	SAP
	L	L	H	M	SAP	L + R	SAP
	H	L	H	H	SAP	L + R	SAP

*: Don’t care

Regarding ST, SAP, ID

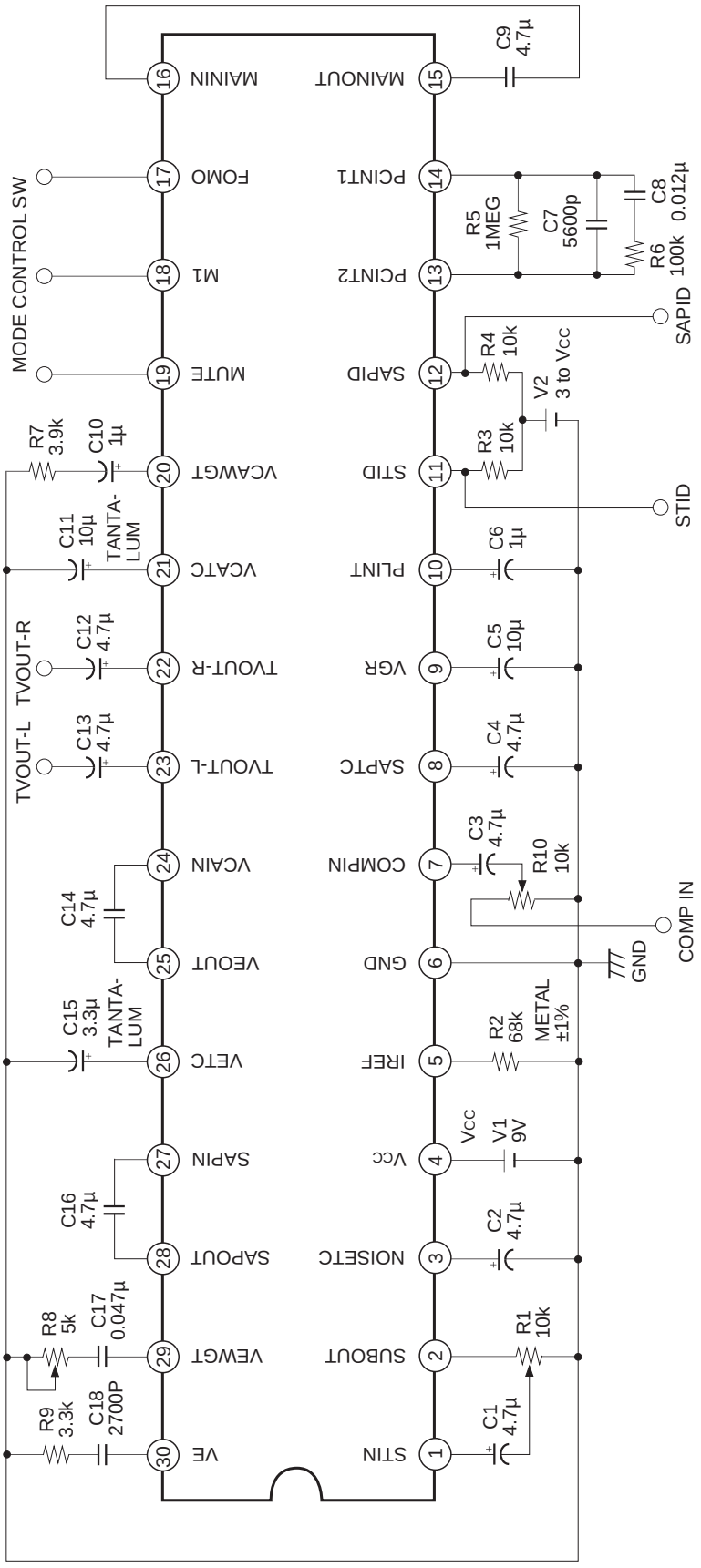
L shows that drive current runs through load register and pin voltage is low.

H shows that drive current doesn't run through load resistor and pin voltage is high.

Limits of Control Voltage

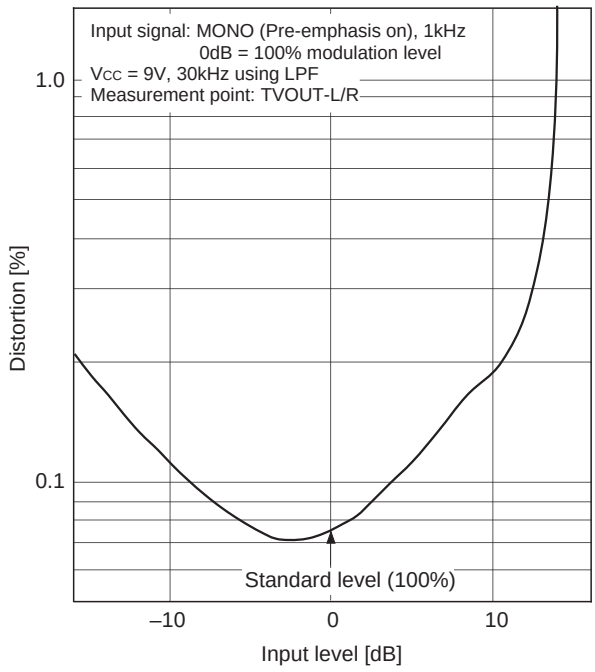
M1	H	SAP	4.5V to V_{CC}
	M	BOTH	2 to 3V (or OPEN)
	L	STEREO	0 to 0.5V
FOMO	H	STID-H	8.5V to V_{CC}
	M	STID-L	3 to 7V
	L	STID-L	0 to 0.5V (or OPEN)
MUTE	H	ON	3V to V_{CC}
	L	OFF	0 to 0.5V (or OPEN)

Application Circuit

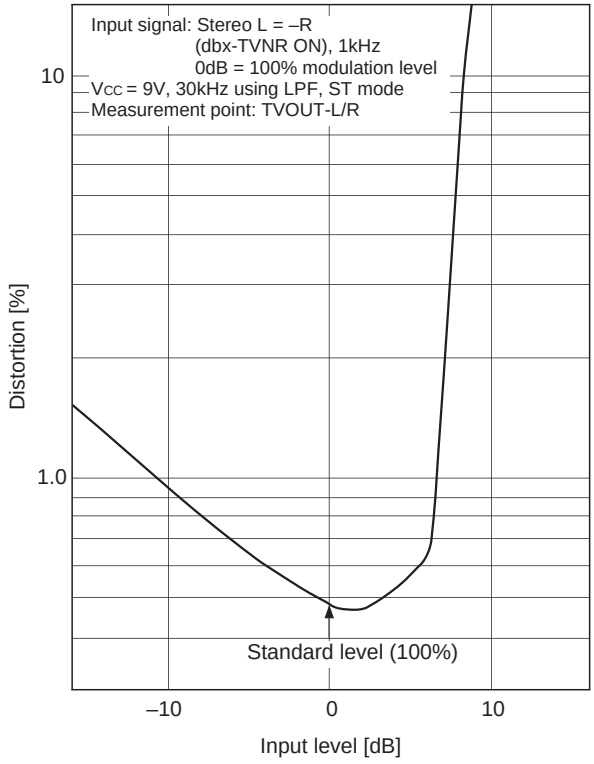


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

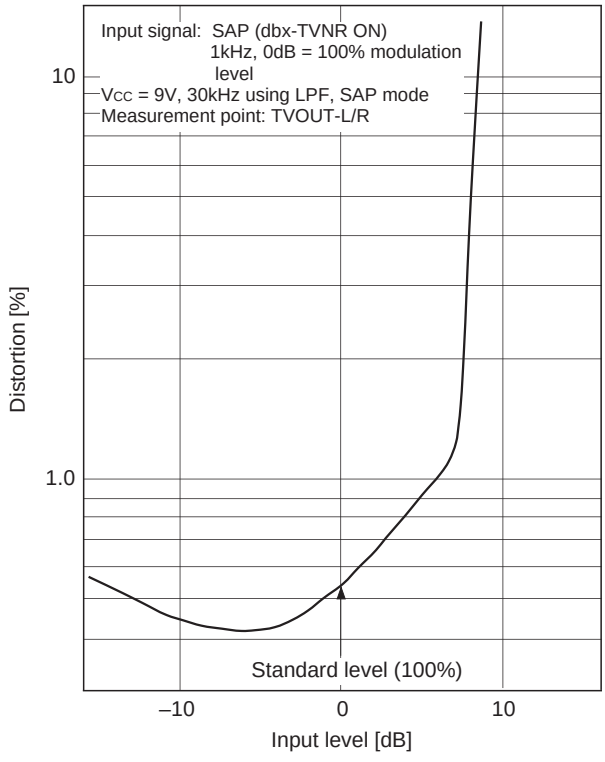
Input level vs. Distortion characteristics 1 (MONO)



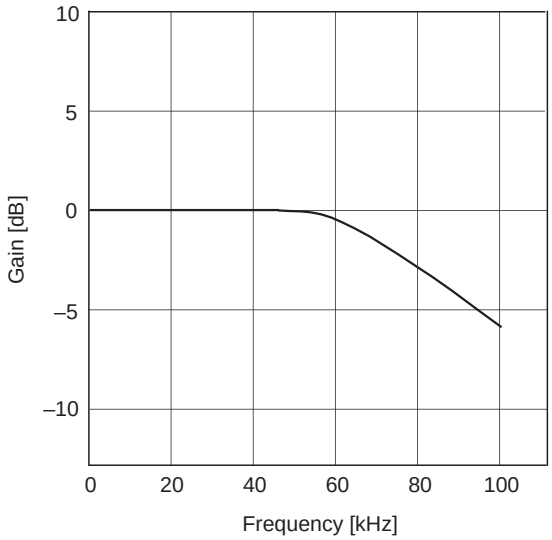
Input level vs. Distortion characteristics 2 (Stereo)



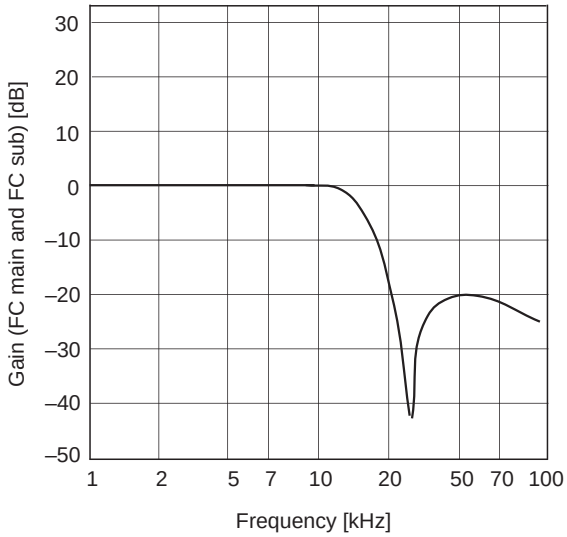
Input level vs. Distortion characteristics 3 (SAP)



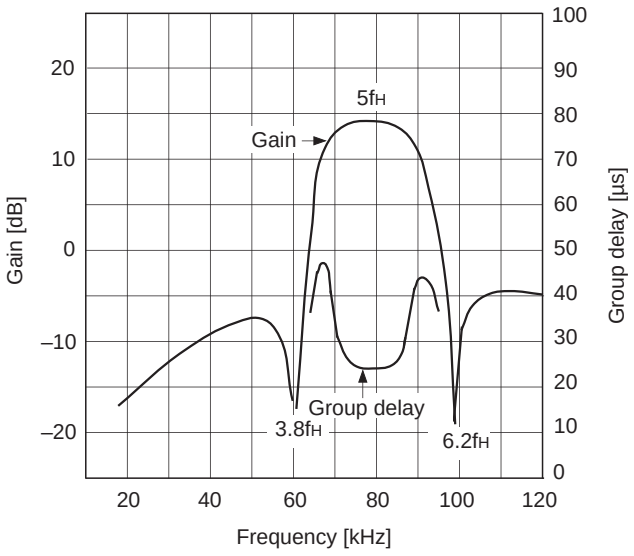
Stereo LPF frequency characteristics



Main LPF and Sub LPF frequency characteristics

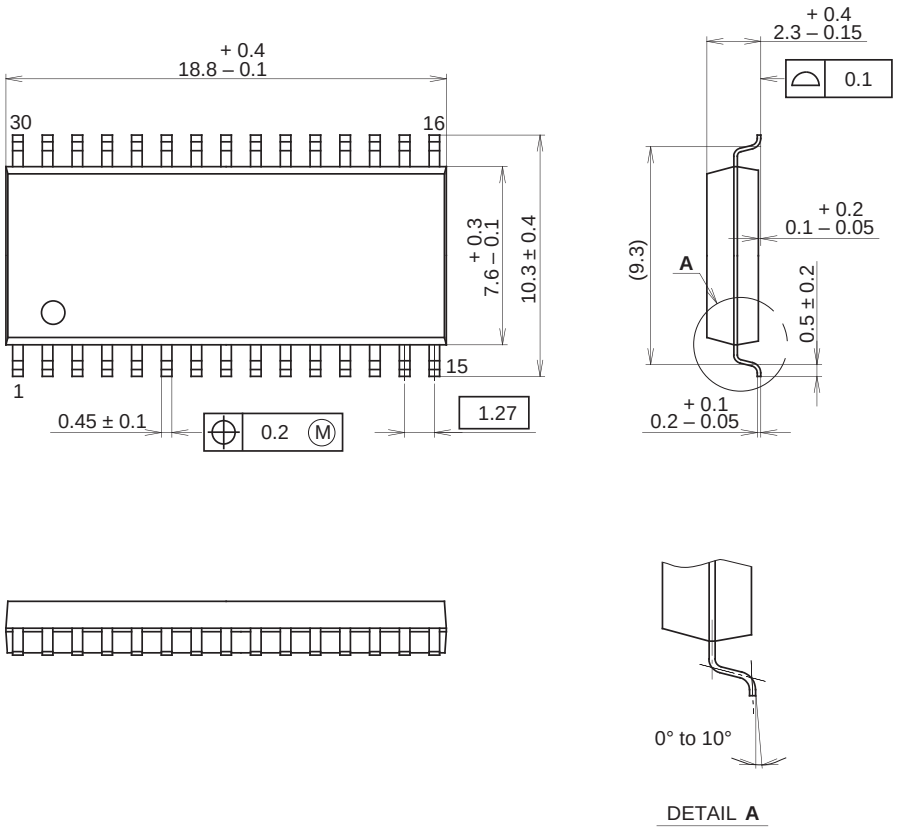


SAP frequency characteristics and group delay



Package Outline Unit: mm

30PIN SOP(PLASTIC)



SONY CODE	SOP-30P-L03
EIAJ CODE	SOP030-P-0375
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).