CL-PS7500FE

Product Bulletin

FEATURES

- **Massively integrated system-on-a-chip**
  - — High-speed CPU and all major system peripherals incorporated
  - — Minimized need for external components
  - — Maximum design simplicity
- **CRT/LCD controller**
  - — Unified Memory Architecture (UMA)
  - — Resolutions up to 1024 × 768 (XGA)
  - — 256-entry 28-bit video palette
  - — Up to 16 million colors
  - — Up to 120-MHz pixel clock rates for flicker-free screen refresh
  - — Supports single- and dual-scan LCD panels
  - — 16-level grayscaler
  - — Hardware cursor for all display modes
- **Performance matching 100-MHz Intel® ’486-based PC**
- **32-bit ARM710A microprocessor**
  - — ARM7 CPU

High-Performance System-on-a-Chip with CRT/LCD Controller

OVERVIEW

The CL-PS7500FE is a massively integrated general-purpose ‘system-on-a-chip’ designed for a wide range of control and communications applications. Based on a low-power, high-speed ARM® RISC CPU core, the CL-PS7500FE integrates a powerful 50-MIPS processor, hardware floating point unit, memory interfaces, and a full complement of system peripherals onto a single chip. This integrated chip greatly simplifies system design for complex applications such as network computers, set-top boxes, screen phones, process control systems, and instrumentation control.

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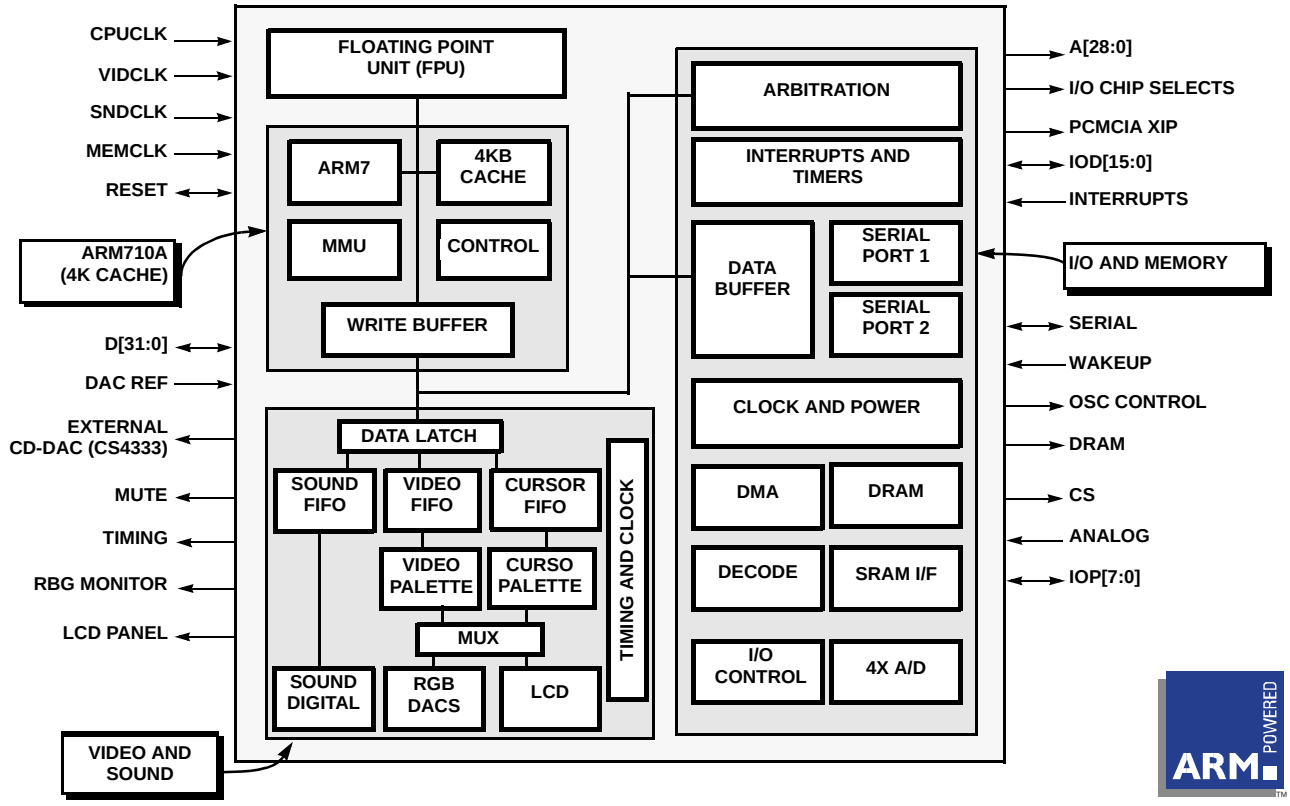
FUNCTIONAL BLOCK DIAGRAM



FEATURES (cont.)

- 4 Kbytes of unified cache
- MMU with 64-entry TLB (transition look-aside buffer)
- 8-words-deep write buffer

■ **Hardware FPU**
- Implements ANSI/IEEE Std. 754-1985
- Single, double, and extended precision
- Up to 12 Mflops, double-precision FP
- Ideal for Java™

■ **DRAM controller**
- Supports EDO and Fast Page Mode DRAMs
- Up to 132 Mbps (peak) throughput using 64-MHz memory clock and 32-bit-wide DRAMs
- Programmable 16- or 32-bit-wide memory system
- Pipelined speed-critical paths

■ **ROM/FLASH memory control**
- Supports two 16-Mbyte banks
- Individual read timings
- Burst mode reads
- Allows for writes under register control for FLASH

■ **Two PS/2®-style serial ports**
- Keyboard
- Mouse

■ **16-bit ISA-style I/O bus**
- Allows for connection to industry-standard peripheral devices
- CS89XX Ethernet controller
- 56K Fax/modem chipset
- Can be expanded to 32 bits with external transceivers

■ **Serial CD-quality digital sound (32-bit) output**

■ **Three-state power management**

■ **Eight general-purpose I/O lines**

■ **Four analog comparators**
- Supports analog joystick

■ **Timer and counters**

■ **Available in 40- and 56-MHz speed grades**

■ **240-pin MQFP package**

■ **Evaluation kit available with BOM, schematics, and design database**

OVERVIEW (cont.)

In addition to the 32-bit processor with a hardware floating point unit, the CL-PS7500FE incorporates system cache, a MMU (memory management unit), a high-resolution color CRT/LCD graphics controller, a CD-quality audio controller, and various other peripheral interfaces.

Display Interface

The display controller section of the CL-PS7500FE features direct drive of an RGB color monitor or a color LCD. It supports up to a 120-MHz pixel clock rate for flicker-free screen refreshes at resolutions up to the XGA 1024 x 768. It also incorporates various sync signals; when combined with an external encoder device, these signals permit the use of interlaced television monitors for display. A hardware cursor is supported in all display modes to minimize system overhead during cursor updates.

The CL-PS7500FE makes use of an UMA (unified memory architecture) that allows for a design to share system memory between the display function and the program memory. This eliminates the need for separate memory blocks for display and program memory and reduces overall system costs. A dedicated high-speed DMA channel is used to control screen updates and minimize the overall system bandwidth devoted to display requirements.

I/O and Memory

In addition to the advanced peripherals incorporated into the CL-PS7500FE, a wide variety of Cirrus Logic and industry-standard third-party peripheral functions can be attached through the CL-PS7500FE's integrated 16-bit ISA-style I/O bus and eight general-purpose I/O signals. Peripherals such as modems, mass storage subsystems, CCD cameras, data acquisition subsystems, and bar code readers can easily be interfaced to the CL-PS7500FE through these connections. For example, the Cirrus Logic CS8900A Ethernet controller can be easily attached for high-speed network communications. The device also has direct connections for a PS/2-style keyboard and a mouse as well as a serial CD-quality stereo audio output.

For high performance, the built-in memory controller in the CL-PS7500FE supports EDO DRAMs. DRAMs can interface directly to the CL-PS7500FE in up to 4 separate banks for maximum design flexibility.

Speed Grades

The CL-PS7500FE is available in two speed grades:

- ARM CPU running at 40 MHz; memory clock running up to 64 MHz
- ARM CPU running at 56 MHz; memory clock running up to 64 MHz

Packaging

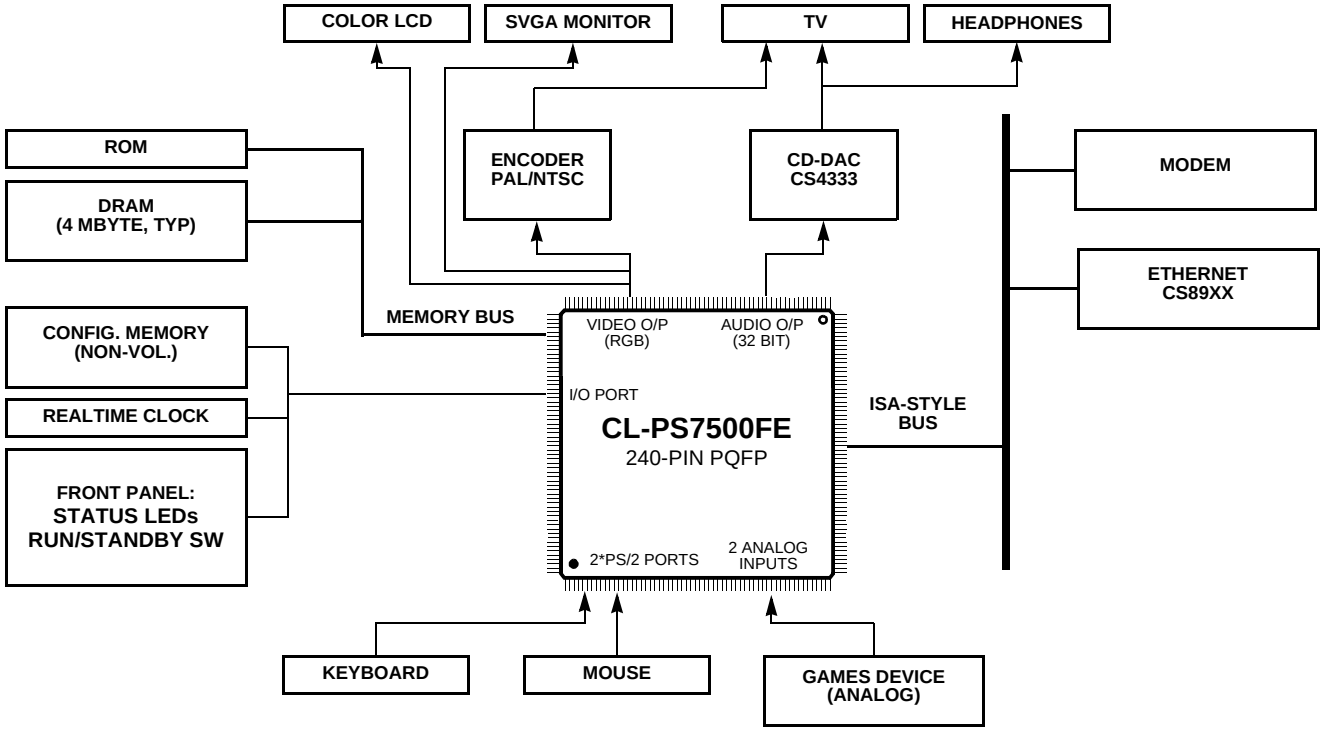
The CL-PS7500FE is available in a 240-pin MQFP package.

ARM® Compatibility

The ARM processor architecture is quickly becoming the industry's 32-bit standard. Investment protection in software and hardware designs is insured with over 30 companies building products based on this open, standard processor core. In addition, a wide range of realtime kernels, sophisticated operating systems, and state-of-the-art application development tools are available from third parties worldwide.

System Design

As shown in the system block diagram below, simply adding desired memory and peripherals to the highly integrated CL-PS7500FE completes a high-performance system board. All the interface logic is integrated on-chip.



A CL-PS7500FE–Based System

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