CS61581

Product Data Sheet

CIRRUS LOGIC

FEATURES

- **Provides T1 and E1, Long Haul and Short Haul Line Interface**

- **Provides a QRSS Test Signal and Error Detector**

- **Impedance Matching Line Driver Using a Single Transformer**

- **Greater than 14dB of Transmit Return Loss Without Using External Resistors**

- **No Crystal Needed for Jitter Attenuation**

- **Meets AT&T 62411 and CTR-12 Jitter Tolerance and Attenuation Requirements**

- **Meets ANSI T1.231B and ITU-T G.775 Requirements for LOS and AIS**

- **Meets the BS6450 Transmitter Short-Circuit Requirements for E1 Applications**

- **Compliant with:**
  - ITU-T Recommendations: G.703, G.732, G.775 and I.431
  - American National Standards (ANSI): T1.102, T1.105, T1.403, T1.408, and T1.231
  - FCC Rules and Regulations: Part 68 and Part 15
  - AT&T Publication 62411
 - ETSI ETS 300 011, 300 233, CTR 12, TBR 13
  - TR-NET-00499

CRYSTAL®

T1/E1 Universal Line Interface

DESCRIPTION

The CS61581 is a primary rate line interface unit capable of operation in both short haul (intraoffice) and long haul applications. The CS61581 combines the complete analog transmit and receive circuitry for a single, full-duplex interface at T1 and E1 rates. The device is pin and function compatible with the Level One LXT310 and LXT318 (the latter in the host mode only). Enhanced functionality is available through an extended register set allowing short haul operation, custom pulse shape generation, QRSS pattern generation, detection and error counting, and generation and detection of loop up and loop down codes. The CS61581 features Crystal® low-power impedance-matched line drivers and crystalless jitter attenuation.

ORDERING INFORMATION
CS61581-IL	28-pin PLCC
CS61581-IP	28-pin PDIP
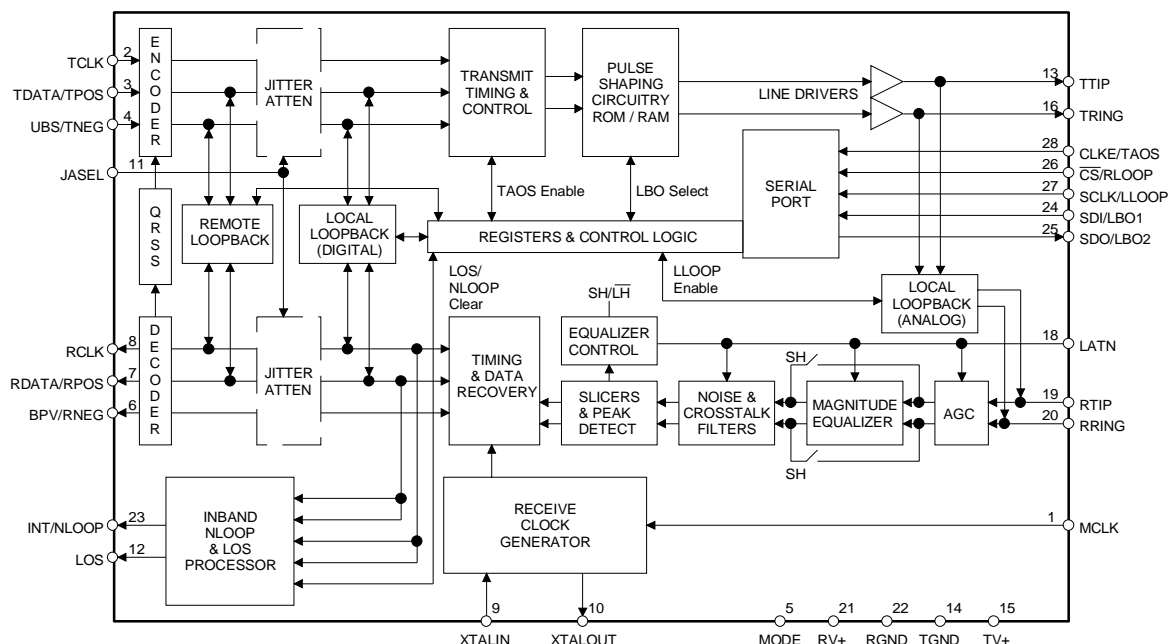
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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to RGND=TGND=0 V)	RV+	-	6.0	V
	TV+	-	(RV+) + 0.3	V
Input Voltage, Any Pin	V_{in}	RGND-0.3	(RV+) + 0.3	V
Input Current, Any Pin (Note 1)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes

Notes: 1 Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 1)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Power Consumption, Long Haul (Notes 2,3,4) Low Z	P_C	-	390	590	mW
Match Z		-	400	540	
Power Consumption, Short Haul (Notes 2,3,4) Low Z	P_C	-	480	640	mW
Match Z		-	430	600	

Notes: 1. TV+ must not exceed RV+ by more than 0.3 V.

2. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

3. Typical consumption corresponds to 50% ones density and medium line length at 5.0 V.

4. Maximum consumption corresponds to 100% ones density and maximum line length at 5.25 V.

DIGITAL CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0 V ±5%; GND = 0 V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 5) PINS 1-4, 24-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Note 5) PINS 1-4, 24-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Notes 5, 6) I_{OUT} = -40 µA PINS 6-8, 25	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Notes 5, 6) I_{OUT} = 1.6 mA PINS 6-8, 25	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	µA

Notes: 5. This specification guarantees TTL compatibility (V_{OH} = 2.4 V @ I_{OUT} = -40 µA).

6. Output drivers are TTL compatible and will drive CMOS logic levels into a CMOS load.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0 V ±5%; GND = 0 V)

Parameter		Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes	(Note 7)				
	E1, 75 Ω (Note 8)	2.14	2.37	2.6	V
	E1, 120 Ω (Note 9)	2.7	3.0	3.3	V
	T1, (FCC Part 68) (Note 10)	2.7	3.0	3.3	V
	T1, DSX-1 (Note 11)	2.4	3.0	3.6	V
External Equalizer Pulse Amplitude		4.8	5.6	6.4	V
Transmitter Output Impedance	(Note 9)				
Transformer turns ratio = 1:2	Low Z, Long Haul		1.5		Ω
Transformer turns ratio = 1:1.5	E1, 75 Ω		33		Ω
	E1, 120 Ω		53		Ω
	T1, FCC		44		Ω
	T1, DSX1		44		Ω
	T1, Ext. Equal		44		Ω
Jitter Added by the Transmitter	(Note 12)				
	10 Hz - 8 kHz	-	0.015	-	UI
	8k Hz - 40 kHz	-	0.015	-	UI
	10 Hz - 40 kHz	-	0.015	-	UI
	Broad Band	-	0.020	-	UI
Power in 2 kHz band about 772 kHz	(Notes 7, 13)	12.6	15	17.9	dBm
Power in 2 kHz band about 1.544 MHz (referenced to power in 2 kHz band at 772 kHz)	(Notes 7, 13)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Notes 7, 13)	-	0.2	0.5	dB
Transmitter Short Circuit Current	(Notes 7, 14)	-	-	50	mA RMS

Notes: 7. Using a 0.47 µF capacitor in series with the primary of a transformer recommended in the Applications Section.

8. Pulse amplitude measured at the output of the transformer across a 75 Ω load for line length settings LEN2/1/0 = 0/0/1 and 0/0/0.

9. Pulse amplitude measured at the output of the transformer across a 120 Ω load for line length setting LEN2/1/0 = 0/0/0.

10. Pulse amplitude measured at the output of the transformer across a 100 Ω load for line length setting LEN2/1/0 = 0/1/0.

11. Pulse amplitude measured at the DSX-1 Cross-Connect for all line length settings from LEN2/1/0 = 0/1/1 to LEN2/1/0 = 1/1/1.

12. Assuming that jitter free clock is input to TCLK.

13. Not production tested. Parameters guaranteed by design and characterization.

14. Measured broadband through a 0.5 Ω resistor across the secondary of the transmitter transformer during the transmission of an all ones data pattern with LEN2/1/0 = 0/0/0 or 0/0/1.

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ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0 V ±5%; GND = 0 V)

Parameter	Min	Typ	Max	Units
Receiver				
RTIP/RRING Input Impedance	-	20k	-	Ω
Sensitivity Below DSX (0 dB = 3.0 V) Long Haul, T1	-40	-	-	dB
	30	-	-	mV
Sensitivity Below DSX (0 dB = 3.0 V) Long Haul, E1	-36	-	-	dB
	48	-	-	mV
Sensitivity Below DSX (0 dB = 3.0 V) T1 - Short Haul	-21	-	-	dB
	270	-	-	mV
Sensitivity Below G.703 (0 dB = 2.4 V) E1 - Short Haul	-15	-	-	dB
	430	-	-	mV
Loss of Signal Threshold Long Haul, T1 & E1	-	-42	-	dB
T1 Short Haul	-	-22	-	dB
E1 Short Haul	-	-16	-	dB
Data Decision Threshold (Note 15)				
T1, DSX-1	45	50	55	% of peak
T1, (FCC Part 68) and E1	45	50	55	% of peak
Allowable Consecutive Zeros before LOS	160	175	190	bits
Receiver Input Jitter Tolerance - Short Haul (Note 16)				
E1: 10 kHz - 100 kHz	0.35	-	-	UI
T1: 10 kHz - 100 kHz	0.4	-	-	UI
(Note 18) 2 kHz	6.0	-	-	UI
(Note 18) 10 Hz and below	300	-	-	UI
Receiver Input Jitter Tolerance - Long Haul (Note 17)				
E1:10 kHz - 100 kHz	0.35	-	-	UI
T1:10 kHz - 100 kHz	0.4	-	-	UI
1 Hz	138			UI

Notes: 15. Data decision threshold established after the receiver equalizer filters pulse overshoot and undershoot.

16. Jitter tolerance for 0 dB input signal level. Jitter tolerance increases at lower frequencies. See Figure 8.

17. See Receiver Jitter Tolerance Plot, Figure 8.

18. Guaranteed by design.

T1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0 V ±5%;

GND = 0 V; Inputs: Logic 0 = 0 V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
MCLK Frequency	(Note 19)	f_{mclk}	-	1.544	-	MHz
RCLK Duty Cycle	(Note 20)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 21)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 21)	t_f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 22)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 23)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 22)	t_{h1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 23)	t_{h1}	150	274	-	ns

Notes: 19. MCLK provided by an external source or TCLK.

20. RCLK duty cycle will be 62.5% or 37.5% when jitter attenuator FIFO limits are reached.

21. At max load of 1.6 mA and 50 pF.

22. Host Mode (CLKE = 1).

23. Host Mode (CLKE = 0)

E1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0 V ±5%;

GND = 0 V; Inputs: Logic 0 = 0 V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency		f_{tclk}	-	2.048	-	MHz
MCLK Frequency	(Note 19)	f_{mclk}	-	2.048	-	MHz
RCLK Duty Cycle	(Note 20)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 21)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 21)	t_f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 22)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 23)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 22)	t_{h1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 23)	t_{h1}	100	194	-	ns

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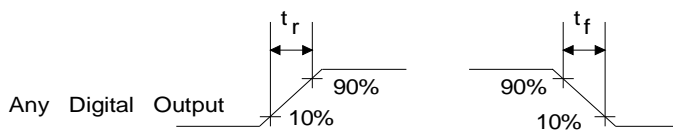
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Figure 1. Signal Rise and Fall Characteristics

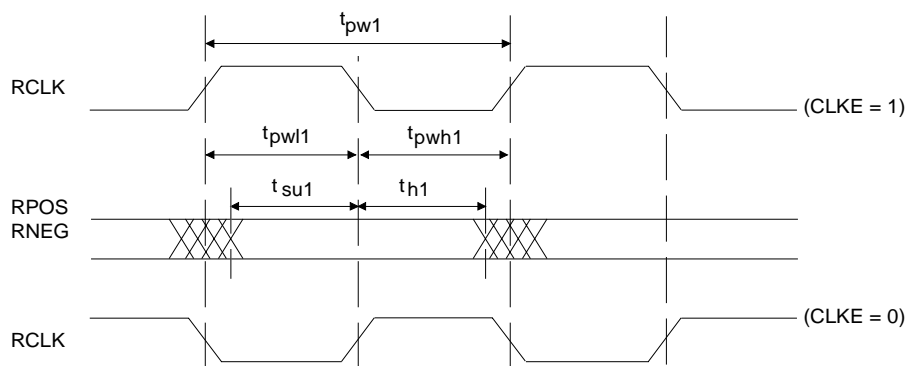**Figure 2. Recovered Clock and Data Switching Characteristics**
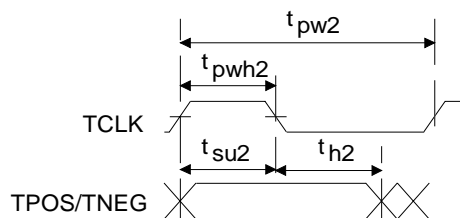
Figure 3. Transmit Clock and Data Switching Characteristics

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SWITCHING CHARACTERISTICS (TA = -40° to 85°C; TV+, RV+ = 5V ±5%;

Inputs: Logic 0 = 0 V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	240	-	-	ns
SCLK High Time	t_{ch}	240	-	-	ns
SCLK Rise and Fall Time	t_r, t_f	-	-	50	ns
CS to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to CS Hold Time	t_{cch}	50	-	-	ns
CS Inactive Time	t_{cwh}	250	-	-	ns
SCLK to SDO Valid (Note 24)	t_{cdv}	-	-	200	ns
CS to SDO High Z	t_{cdz}	-	100	-	ns

Notes: 24.   Output load capacitance = 50 pF
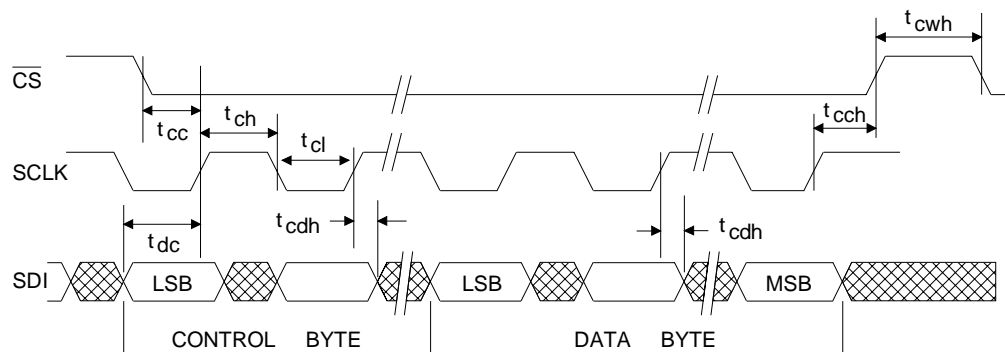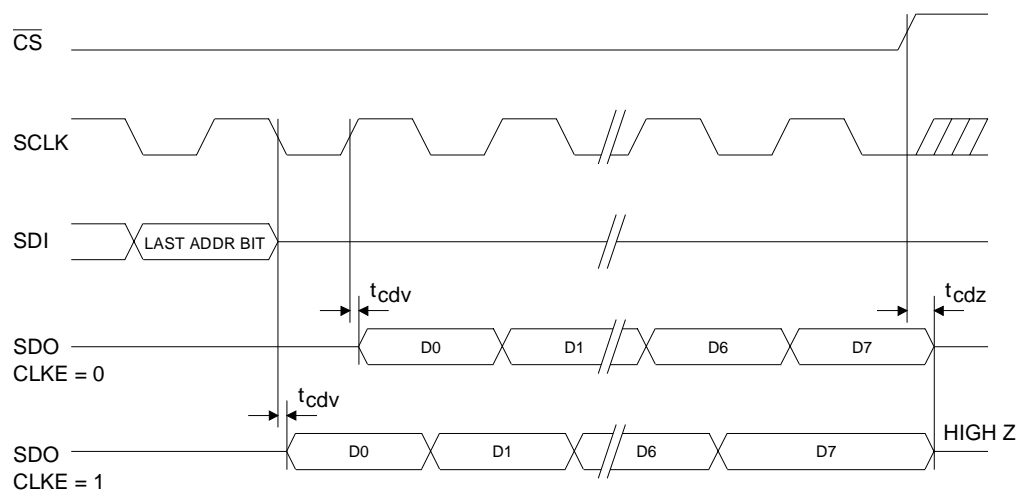

Figure 4. Serial Port Write Timing Diagram

Figure 5. Serial Port Read Timing Diagram

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THEORY OF OPERATION

The CS61581 Universal Line Interface supports T1 and E1 data rates for both short haul and long haul applications. The transmitter outputs all pulse shapes for T1 and E1 applications, and matches the standard line impedances with a single turns ratio transformer. When configured for long haul operation, the receiver uses gain and equalization to provide 40 dB of sensitivity. The receiver reconfigures for short haul operation, limiting the receive sensitivity to meet industry specifications.

Introduction to Operating Modes

The CS61581 can be operated in stand-alone hardware interface mode (MODE pin is low), or by a microcontroller in serial host mode (MODE pin is high). Additional functionality is available in the host mode including both short haul and long haul operational modes. The CS61581 defaults to the Long Haul configuration (LXT310/318 compatible). The T1 (DSX-1 and Network interface) and E1 (ITU-T G.703) are selectable via the serial port by writing to a control register.

Tying TNEG high for more than 16 TCLK cycles enables the coder mode, changing TPOS to TDATA, RPOS to RDATA, and RNEG to BPV. When configured for coder mode, the MODE pin can be tied to RCLK enabling the B8ZS encoders and decoders. Coder mode does NOT support LXT318 compatibility for E1 operation.

Master Clocks

The CS61581 requires a reference clock for the receiver and the jitter attenuator. Either a 1.544 MHz (or 2.048 MHz) external clock can be input to MCLK, or a 4x crystal can be connected to the on-chip oscillator. This frequency reference should be within 100 ppm of the nominal operating frequency. Jitter and wander on the reference clock will degrade jitter attenuation and receiver jitter tolerance. If MCLK is provided, the crystal oscillator is ignored.

Transmitter

The transmitter accepts digital T1 or E1 input data and drives appropriately shaped AMI (Alternate Mark Inversion) pulses onto a transmission line through a transformer. The transmit data (TPOS & TNEG or TDATA) is sampled on the falling edge of the input clock, TCLK.

Upon power up, the CS61581 defaults to Long Haul Mode with low-impedance drive. In this mode, a 1:2 transformer is required (See Table 1). The CS61581 will support both T1 and E1 operation as determined by the master clock frequency.

In host mode, T1 (DSX-1 or Network Interface), E1 (ITU-T or G.703) or T1 long-haul pulse shapes may be selected. Long-haul or short-haul operation is determined by the SH/$\overline{\text{LH}}$ bit (CR2.0). The SH/$\overline{\text{LH}}$ bit also establishes functionality of Control Registers 1 and 2.

In the matched impedance configuration, the line driver internally matches the impedance of the line load; 75 Ω or 120 Ω for E1, and 100 Ω for T1 using a 1:1.5 turns ratio transformer. Internal impedance matching reduces current consumption by about a factor of two compared to return loss achieved by external resistors.

The T1 long-haul pulse shapes comply with FCC Part 68 Option A (0 dB). Option B (-7.5 dB), Option C (-15 dB) or (-22.5 dB) (see Table 1). If desired, the T1 preequalization settings can be selected for E1 operation as well. In long-haul mode, pulse shaping and signal level are controlled by LBO1 and LBO2 pins or register bits.

Custom transmit pulse shapes may be implemented by writing pulse shape coefficients to the registers. Custom pulses may be used to correct for pulse shape degradation or distortion caused by improper termination, suboptimal interconnect wiring, or loading from external components such as high voltage protection devices.

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Long Haul

LB02	LB01	Output Pulse
0	0	0 dB
0	1	-7.5 dB
1	0	-15 dB
1	1	-22.5 dB

	Transformer Turns Ratio	
Mode	Transmit	Receive
HDW or MATCHZ* = 0	1:2	1:1
MATCHZ* = 1	1:1.5	1:1

* MATCHZ = CR2.5

Short Haul

LEN2	LEN1	LEN0	Output Pulse		Line Z
0	0	0	E1	2.37 V	75Ω
0	0	1	E1	3.0 V	120Ω
0	1	1	DSX-1	0'-133'	100Ω
1	0	0	DSX-1	133'-266'	100Ω
1	0	1	DSX-1	266'-399'	100Ω
1	1	0	DSX-1	399'-533'	100Ω
1	1	1	DSX-1	533'-655'	100Ω
0	1	1	ANSI	T1.403	100Ω
0	1	0	DSX-1	6.0 V	100Ω

Table 1. Pulse Shape Selection and Transformer Requirements

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the transmitter to the DSX-1 cross connect) may be selected. The five partition arrangement in Table 1 meets ANSI T1.102 pulse shape requirements when using #22 ABAM or AT&T 600 series cable. A typical output pulse is shown in Figure 6. These pulse settings can also be used to meet ITU-T pulse shape requirements for 1.544 MHz operation. Short haul pulse shapes for T1 and E1 are selected by the LEN2, LEN1, and LEN0 bits in Control Register 1.

Note that when the device is operated at E1 frequency in the hardware mode, it defaults to low impedance, long haul mode. The pulses driven by the transmitter in this mode are T1.403 (350ns) pulses with an overshoot and an undershoot. To drive pulses without overshoot and undershoot in E1 long haul mode, the E1_LH bit (CR3.6) must be set to 1, with the SH/$\overline{\text{LH}}$ bit (CR2.0) set to 0.
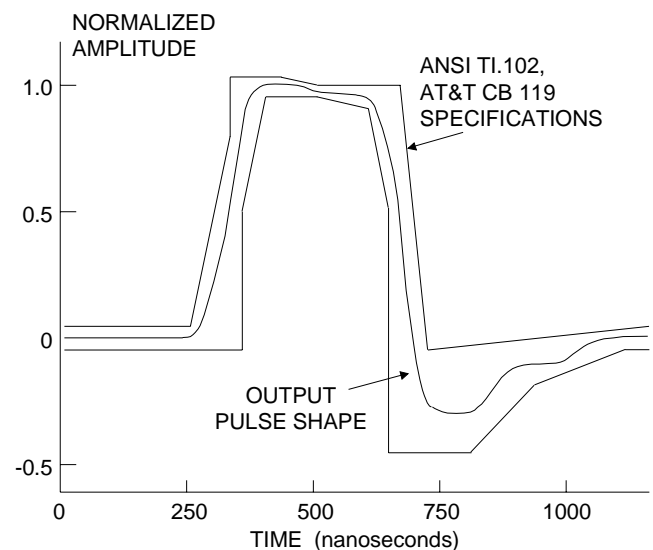

Figure 6. Typical Pulse Shape at DSX-1 Cross Connect

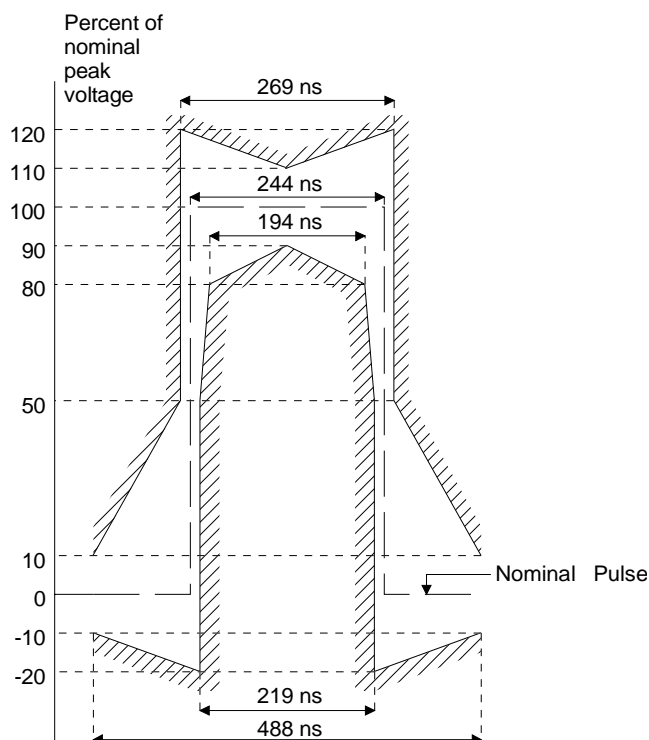**CIRRUS LOGIC PRODUCT DATA SHEET**

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Figure 7. Mask of the Pulse at the 2048 kbps Interface

The E1 G.703 pulse shape is supported with line length selections LEN2/1/0=0/0/0 for 2.37 V 75Ω applications or LEN2/1/0=0/0/1 for 3.0 V 120 Ω applications. The output pulse will meet the G.703 pulse shape template shown in Figure 7. The output impedance of the driver will adjust according to the pulse shape selected.

The CS61581 will detect the absence of TCLK, and will force TTIP and TRING to high impedance after 175 bit periods, preventing transmission when data input is not present. In host mode, the transmitter can be set to high impedance by setting the TxHIZ bit, CR2.1, to "1."

When any transmit control bit (TAOS, LEN0-2, LBO1-2, or LLOOP) is toggled, the transmitter outputs will require approximately 22 bit periods to stabilize. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

The CS61581 has the option to drive a 6 V$_{peak}$ pulse. The option is used for driving external equalizers used in some T1 DSX applications. The configuration is selected by setting the LEN2/1/0 control bits in register 16 to 0/1/0 in short haul configuration.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. If TCLK is absent, then MCLK is used (or the quartz crystal generated frequency in the absence of MCLK). Transmit all ones is selected when TAOS, pin 28, (CR1.7 = 1, in host mode) goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). When TAOS is active, the TPOS and TNEG (TDATA) inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

In Hardware mode, the receiver is configured for Long Haul operation. In host mode Short Haul operation can be selected by setting the SH/$\overline{LH}$ to "1," (CR2.0 = 1). When configured for short haul, the functions of registers 16 and 17 are redefined. In both receiver modes, a noise and cross-talk filter removes signal components that are coupled onto the line from other cables. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, AT&T 62411, TR-TSY-000170, ITU-T G.823 and ETSI CTR12. Jitter tolerance is shown in Figure 8. The RTIP and RRING inputs are biased to an intermediate DC level and treat the input signal differentially.

Short Haul

The Short Haul receiver extracts data and clock from an AMI coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of the recommended cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuit.
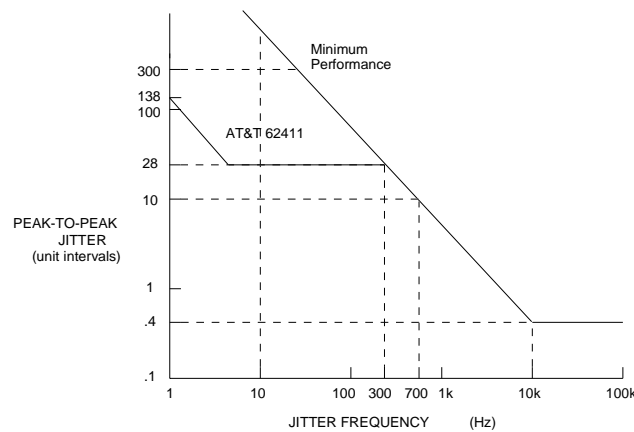
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Figure 8. Minimum Input Jitter Tolerance of Receiver

Receiver sensitivity is set to comply with ITU-T I.431 requirements, providing more than -6 dB of sensitivity for E1 and -18 dB of sensitivity for T1. T1 or E1 operation is determined by the transmit pulse shape selection, LEN2/1/0. The comparator thresholds are dynamically established at 50% percent of the peak level. This is acceptable for both T1 and E1 cases as pulse undershoot and overshoot is filtered internally.

Long Haul

The Long Haul receiver extracts data and clock from the input signal and outputs clock and synchronized data. The Long Haul receiver can receive signals over the entire range down to -40 dB at T1 and -36dB at E1 rates. The incoming pulses are amplified, equalized and filtered before being fed to the comparator for peak detection, slicing and data recovery.

Clock Recovery

The clock recovery circuit is a third-order phase lock loop. The clock and data recovery circuit is tolerant of long strings of consecutive zeros, and will successfully receive a 1-in-175, jitter-free input signal.

Data on RPOS and RNEG (RDATA), is stable and may be latched using the falling edge of recovered clock, RCLK. In host mode, CLKE, pin 28, determines the clock polarity for which output data is stable and valid as shown in Table 2. When CLKE is high, RPOS and RNEG (RDATA) are valid on the falling edge of RCLK. When CLKE is low, RPOS and RNEG are valid on the rising edge of RCLK.

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW	Don't Care	RPOS RNEG	RCLK	Rising
HIGH	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising

Table 2. Data Output/Clock Relationship

Jitter Tolerance

The receiver jitter tolerance is shown in Figure 8. The CS61581 has excellent jitter tolerance, accepting as much as 0.4UI of jitter from 10 kHz to 100 kHz, without error, in T1 operation, exceeding industry specifications such as AT&T 62411 for synchronizers. The jitter tolerance in this frequency range for E1 operation is 0.35UI.

Receiver Line Attenuation Indication

The LATN pin, pin 18, outputs a coded signal that represents the signal level at the input of the receiver. As shown in Figure 9, the LATN output is measured against RCLK to provide the signal level in 7.5 dB increments. In host mode, the receive input signal level can be read from the Equalizer Gain register, address 0x12, to greater resolution, dividing the input range into 20 steps of 2 dB increments.
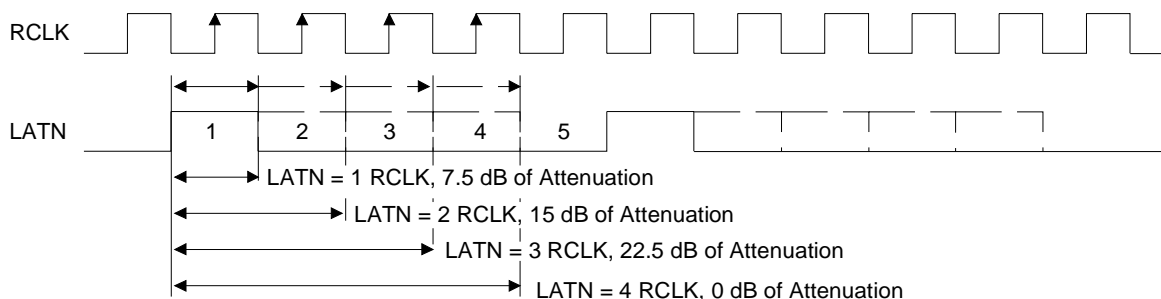
Figure 9. LATN Pulse Width encoding

Jitter Attenuator

Jitter attenuation can be implemented in either the transmit (JASEL is low) or receive (JASEL is high) paths, or it can be eliminated from the circuit by setting the XTALIN, pin 9, high. The jitter attenuator on the CS61581 does not require a crystal, and can be activated by setting XTALIN, pin 9, low (preferred) or by floating pin 9.

The jitter attenuator has two modes of operation depending on whether the CS61581 is configured for T1 or E1 operation (based on pulse shape selection). For T1, the jitter attenuator corner frequency is set at 4 Hz, with attenuation increasing at a 20 dB per decade rate above 4 Hz. For E1 the corner frequency is approximately 1.25 Hz in order to comply with ETSI 300 011, CTR12, and recommendation I.431. A typical jitter attenuation graph is shown in Figure 10.

Receiver Loss of Signal

The receiver will indicate loss of signal by setting LOS, pin 12 high (CR1.0 = 1 in host mode), upon power up, reset, when receiver gain is maximized, or upon receiving 175+/-15 consecutive zeros. Received zeros are counted based on recovered clock cycles. When in the LOS state, received data is not output from RPOS/RNEG (RDATA); but is squelched until the device comes out of LOS. The LOS condition is exited using the ANSI T1.231-1993 and ITU-T G.775 criteria, namely 12.5% ones density for 175+/-75 bit periods with no more than 100 consecutive zeros.
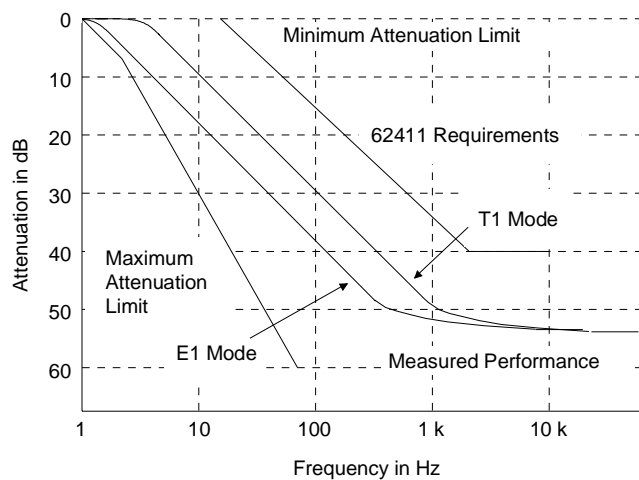

Figure 10. Typical Jitter Transfer Function

In Long Haul operation, the receiver recovers signals down to -40 dB for T1 and -36 dB for E1. In Short Haul mode, the receive sensitivity is typically -21 dB for T1 and -15 dB for E1, in accordance with I.431 and G.775. LOS will be declared beyond these signal levels. These LOS thresholds are compliant with all Short Haul applications.

In LOS, the RCLK frequency depends on whether MCLK is applied, and whether the jitter attenuator is in the transmit or receive path. If the jitter attenuator is in the receive path, the jitter attenuator will hold over the average incoming data frequency prior to LOS. RPOS (RDATA) and RNEG pins are forced low upon LOS.

When the jitter attenuator is in the transmit path or not used, the clock recovery is referenced to MCLK, if provided, or the crystal oscillator. The frequency of RCLK in this case will simply remain

slaved to the clock reference upon loss of data. The recovered clock remains as a 50% duty cycle clock.

The digital PLL in the clock recovery circuit of the CS61581 (just like most industry LIU's available) recovers clock from the edges of the incoming pulses (1's).

Timing is recovered by a phase selector which selects one of the phases from the internal synchronization clock (one of three clocks, 120 degrees apart in phase, at 16X of the data rate). Since the selection is made between a limited set of phases, the Digital Timing Recovery process has a small phase error built into the sampling process. By choosing 48 possible sampling phases, the CS61581 reduces the sampling error to a minimum.

Local Loopback

Local loopback is selected by setting LLOOP, pin 27, high (CR1.6 = 1 in host mode). Selecting local loopback causes clock and data presented on TCLK, TPOS/TNEG (TDATA) to be output at RCLK, RPOS/RNEG (RDATA). Local loopback disconnects the RTIP/RRING inputs from the line and connects them to the transmitter outputs thus enhancing testability. Inputs to the transmitter are still transmitted on TTIP and TRING, unless TAOS has been selected in which case, AMI-encoded continuous ones are transmitted at the TCLK frequency. The receiver RTIP and RRING inputs are ignored when local loopback is in effect.

Remote Loopback

Remote loopback is selected by setting RLOOP, pin 26, high (CR1.5 = 1 in host mode). In remote loopback, the recovered clock and data input on RTIP and RRING are sent back out on the line via TTIP and TRING. Selecting remote loopback overrides a TAOS request. The recovered clock and data from the incoming signal are also sent to RCLK, RPOS and RNEG (RDATA). Simultaneous selection of local and remote loopback modes will cause a device reset to occur (see Reset).

Network Loopback

Network Loopback (automatic remote loopback) can be commanded from the network when the Network Loopback detect function is enabled. In Host Mode, Network Loopback (NLOOP) detection is enabled by writing ones to TAOS, LLOOP, and RLOOP, then clearing these three bits on a successive write cycle. In hardware mode, Network Loopback can be enabled by tying RLOOP to RCLK or by setting TAOS, LLOOP, and RLOOP high for at least 200 ns, and then low. Once enabled Network Loopback functionality will remain in effect until RLOOP is activated or the device is reset.

When NLOOP detection is enabled, the receiver monitors the input data stream for the NLOOP data patterns (00001 = enable, 001 = disable). When an NLOOP enable data pattern is repeated for a minimum of five seconds (with less than 10E-3 BER), the device initiates a remote loopback. Once Network Loopback detection is enabled and activated by the NLOOP data pattern, the loopback is identical to Remote Loopback initiated at the device. NLOOP is reset if the disable pattern (001) is received for 5 seconds, or by activation of RLOOP. NLOOP is temporarily suspended by LLOOP, but the NLOOP state is not reset.

Alarm Indication Signal

The receiver sets the register bit, AIS, to "1" when less than 9 zeros are detected out of 8192 bit periods. AIS returns to "0" upon the first read after the AIS condition is removed, determined by 9 or more zeros out of 8192 bit periods.

Serial Interface

In the Host Mode, pins 24 through 28 serve as a microcontroller interface. On-chip registers can be written to via the SDI pin or read from via the SDO pin at the clock rate determined by SCLK. Through these registers, a host controller can be used to control operational characteristics and monitor device

status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 2. Data transfers are terminated by setting CS high. CS may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{CS}$ may go high any time to terminate the output and set SDO to high impedance.

Figure 11 shows the timing relationships for data transfers when CLKE = 0. When CLKE = 1, data bit D7 is held until the falling edge of the 16th clock

cycle. When CLKE = 0, data bit D7 is held valid until the rising edge of the 17th clock cycle. SDO goes high-impedance after $\overline{CS}$ goes high or at the end of the hold period of data bit D7.

SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bi-directional I/O port.

An address/command byte, shown in Figure 11, points to addresses 0x10 through 0x15 (address 0x10 shown), and precedes a data byte. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The last bit is ignored. Data to the internal registers is input on the eight clock cycles immediately following the address/command byte.

	7	6	5	4	3	2	1	0	ADDR
Control Register 1 LH (CR2.0 = 0) (CR1LH)	TAOS	LLOOP	RLOOP	LB02	LB01	CODER TAZ	NLOOP	LOS	0x10 R/W
Control Register 1 SH (CR2.0 = 1) (CR1SH)	TAOS	LLOOP	RLOOP	LEN2	LEN1	LEN0	RSVD	LOS	0x10 R/W
Control Register 2 LH (CR2.0 = 0) (CR2LH)	AIS	RAMPLSE	MATCHZ	LOOPDN	LOOPUP	RPWDN	TxHIZ	SH/$\overline{LH}$	0x11 R/W
Control Register 2 SH (CR2.0 = 1) (CR2SH)	AIS	RAMPLSE	MATCHZ	RSVD	RCODER	TCODER	TxHIZ	SH/$\overline{LH}$	0x11 R/W
Equalizer Gain (EQGAIN)	X	X	X	EQ4	EQ3	EQ2	EQ1	EQ0	0x12 R
RAM Address (RAM)	MSB	-	-	-	-	-	-	LSB	0x13 R/W
Control Register 3 (CR3)	QRSS-PATH	E1_LH	RST_ERR	QDET	QINS_ERR	QSYNC TEST	QGEN	TEST	0x14 R/W
Data Pattern Error Count (DPEC)	MSB	-	-	-	-	-	-	LSB	0x15 R

Table 3. Register
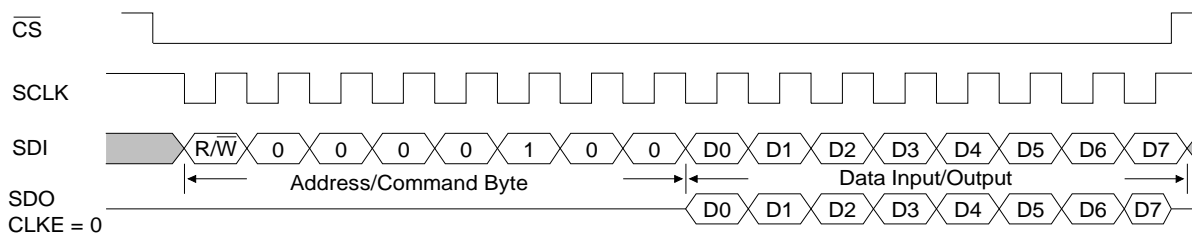
Figure 11. Input/Output Timing (showing address 0x10)

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Control Register 1 LH (CR2.0 = 0): Address 0x10

7 (MSB)	6	5	4	3	2	1	0 (LSB)
TAOS	LLOOP	RLOOP	LB02	LB01	CODER TAZ	NLOOP	LOS

TAOS   Transmit All Ones Select
        When TAOS = 1, all ones are transmitted at the TCLK frequency

LLOOP   Local Loopback
         When LLOOP = 1, data input at TPOS, TNEG (TDATA) is internally looped back and output on
         RPOS, RNEG (RDATA). TCLK is routed to RCLK, through the jitter attenuator, if activated.

RLOOP   Remote Loopback
         When RLOOP = 1, clock and data recovered by the receiver are sent back through the transmit
         path and retransmitted. The clock and data are routed through the jitter attenuator, if activated.

LBO2, 1   Line BuildOut
           LBO2   LBO1   Attenuation
           0   0   0 dB
           0   1   -7.5 dB
           1   0   -15 dB
           1   1   -22.5 dB
           For E1 long haul, only the 0 dB setting should be used when the part is configured for matched
           impedance drive with a 1:1.5 transformer.

CODER   Zero Substitution (valid only when TNEG (UBS) is tied high, invoking coder mode).

(TAZ)   Setting CODER to "1" enables B8ZS (HDB3) encoding and decoding.
         The substitution depends on whether the CS61581 is configured for T1 or E1 operation. via the
         E1_LH bit, CR3.6
         When not in coder mode (TPOS/TNEG are data inputs) setting TAZ to "1" causes all zeros to
         be transmitted.

NLOOP   Network Loopback
         NLOOP = 1 when a network loopback code has been detected on the received signal.
         An interrupt will occur when NLOOP changes state unless a "1" is written to NLOOP disabling
         the interrupt.

LOS   Loss Of Signal
       LOS = 1 when the loss of signal criteria have been met (175 zeros).
       LOS = 0 when a valid signal is being received.
       An interrupt will occur when LOS changes state unless a "1" is written to LOS disabling the in-
       terrupt.

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Control Register 1 SH (CR2.0 = 1): Address 0x10

7 (MSB)	6	5	4	3	2	1	0 (LSB)
TAOS	LLOOP	RLOOP	LEN2	LEN1	LEN0	RSVD	LOS

TAOS   Transmit All Ones Select
When TAOS = 1, all ones are transmitted at the TCLK frequency

LLOOP   Local Loopback
When LLOOP = 1, data input at TPOS/TNEG (TDATA) is internally looped back and output on RPOS/RNEG (RDATA). TCLK is routed to RCLK, through the jitter attenuator, if activated.

RLOOP   Remote Loopback
When RLOOP = 1, clock and data recovered by the receiver are sent back through the transmit path and retransmitted. The clock and data are routed through the jitter attenuator, if activated.

LEN [2:0]   Line Length Selection
Allows selection of a variety of transmit pulse shapes.
See Table 1 for details.
Note that the selection of T1 or E1 pulse shapes determines the operation of the device. When MATCHZ is set to "1" the transmitter's output impedance changes according to the pulse selected. For T1 pulses, the encoders and decoders are set to B8ZS, and the QRSS data pattern is 2^{20}-1 with 14 consecutive zeros, max. For E1 pulses, the encoders and decoders are set to HDB3, and the QRSS data pattern is 2^{15}-1.

RSVD   This bit is reserved.

LOS   Loss Of Signal
LOS = 1 when the loss of signal criteria have been met (175 zeros).
LOS = 0 when a valid signal is being received.
An interrupt will occur when LOS changes state unless a "1" is written to LOS disabling the interrupt.

Control Register 2 LH: Address 0x11

7 (MSB)	6	5	4	3	2	1	0 (LSB)
AIS	RAMPLSE	MATCHZ	LOOPDN	LOOPUP	RPWDN	TxHIZ	SH/LH

AIS   Alarm Indication Signal.
AIS = 1 when an all ones pattern is present at the receiver. This bit is reset to "0" by the first read occurring after the AIS condition has cleared.
An interrupt will occur when AIS is present unless a "1" is written to AIS disabling the interrupt.

RAMPLSE   When RAMPLSE = 1, output pulse shapes are determined by the codes in the internal, programmable, transmit RAM.

MATCHZ   Matched Impedance Drive
When MATCHZ = 1 the output impedance is set to match the line impedance.
The transmitter's output impedance depends on whether T1 or E1 operation is selected. A 1:1.5 transformer should be used when MATCHZ = 1, and a 1:2 transformer should be used when MATCHZ = 0.

LOOPDN   Loop Down
In Long Haul mode, setting LOOPDN to "1" causes the data pattern 001... to be repetitively transmitted.

LOOPUP   Loop Up
In Long Haul mode, setting LOOPUP to "1" causes the data pattern 00001... to be repetitively transmitted.

RPWDN   Receiver Power Down
When RPWDN = 1, the receiver circuitry is powered down, but the transmitter is still active.

TxHIZ   Transmitter High Impedance
When TxHIZ = 1 the transmitter goes to a low-power, high-impedance state

SH/$\overline{\text{LH}}$ Short Haul / Long Haul Select
When SH/$\overline{\text{LH}}$ = 0, the CS61581 is in the Long Haul mode.
When SH/$\overline{\text{LH}}$ = 1, the CS61581 is in the Short Haul mode. Note that it overwrites the E1_LH bit, if set.
SH/$\overline{\text{LH}}$ control the function of CR1, address 0x10, and CR2, address 0x11.

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Control Register 2 SH: Address 0x11

7 (MSB)	6	5	4	3	2	1	0 (LSB)
AIS	RAMPLSE	MATCHZ	RSVD	RCODER	TCODER	TxHIZ	SH/LH

AIS   Alarm Indication Signal.
AIS = 1 when an all ones pattern is present at the receiver. This bit is reset to "0" by the first read occurring after the AIS condition has cleared.
An interrupt will occur when AIS is present unless a "1" is written to AIS disabling the interrupt.

RAMPLSE   When RAMPLSE = 1, output pulse shapes are determined by the codes in the internal RAM.

MATCHZ   Matched Impedance Drive
When MATCHZ = 1 the output impedance is set to match the line impedance.
The transmitter's output impedance depends on whether T1 or E1 operation is selected. A 1:1.5 transformer should be used when MATCHZ = 1, and a 1:2 transformer should be used when MATCHZ = 0.

RSVD   Reserved. Set to "0" for normal operation.

RCODER   Receive Decoder Enable
In Short Haul mode, when TNEG is held high, setting RCODER to "1" causes the received data to be B8ZS/HDB3 decoded (depends on T1 or E1 pulse shape selection). When RCODER is set to "0" the decoders are set for AMI only. This bit has precedence over the external pin.

TCODER   Transmit Encoder Enable
In Short Haul mode, when TNEG is held high, when TCODER = 1 the transmitter B8ZS/HDB3 encoders are enabled (depends on T1 or E1 pulse shape selection). When TCODER is set to "0" the decoders are set for AMI only. This bit has precedence over the external pin.

TxHIZ   Transmitter High Impedance
When TxHIZ = 1 the transmitter goes to a low-power, high-impedance state

SH/LH   Short Haul / Long Haul Select
When SH/LH = 0, the CS61581 is in the Long Haul mode.
When SH/LH = 1, the CS61581 is in the Short Haul mode.
SH/LH controls the functions of CR1, address 0x10, and CR2, address 0x11.

Equalizer Gain (EQGAIN): Address 0x12

7 (MSB)	6	5	4	3	2	1	0 (LSB)
X	X	X	EQ4	EQ3	EQ2	EQ1	EQ0

EQ[4:0]   The receive equalizer gain settings are broken down into 20 segments and provided at the five LSBs of this register, EQ4 - EQ0. 00001 corresponds to -2 dB, 10100 corresponds to -40 dB. The three MSBs are don't cares.

RAM Address (RAM): Address 0x13

7 (MSB)	6	5	4	3	2	1	0 (LSB)
RAM.7	RAM.6	RAM.5	RAM.4	RAM.3	RAM.2	RAM.1	RAM.0

RAM[7:0]   The RAM address pointer for the arbitrary waveform memory;
a special write procedure must be followed to write the waveform RAM.

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Control Register 3 (CR3): Address 0x14

7 (MSB)	6	5	4	3	2	1	0 (LSB)
QRSSPATH	E1_LH	RST_ERR	QDET	QINS_ERR	QSYNC/Test	QGEN	Test

QRSSPATH   When QRSSPATH = 0 the QRSS pattern will be output from the recovered data pins, RPOS, RNEG (RDATA), and may be received at the transmitter inputs, TPOS, TNEG (TDATA). When QRSSPATH = 1 the QRSS pattern will be output from the line transmitter and may be received at the receiver.

E1_LH   E1 Long Haul
When E1_LH = 1, the following functionality changes: bit CR1LH.2 becomes HDB3 and can be used to enable the HDB3 encoder and decoder; when MATCHZ = 1, the output impedance of the transmitter will be set to match 120Ω; QRSS pattern is 2^{15}-1; the jitter attenuator is adjusted for CTR-12 compliance - knee at 1.25 Hz. Note that this bit is ignored if CR2.0 (SH/LH) = 1. When E1_LH = 0, bit CR1LH.2 is B8ZS, and the QRSS pattern is 2^{20}-1 with 14 zeros, max.

RST_ERR   Reset Data Pattern Error Count Register
Setting RST_ERR to "1" will clear the QRSS error count in the DPEC register. This bit is automatically cleared and will read as "0."

QDET   QRSS Detector Enable
When QDET = 1, the QRSS pattern detector is enabled. Errors detected and counted are stored in the DEPC register, address 0x15.

QINS_ERR   QRSS Error Insert
Setting QINS_ERR to "1" and then "0" causes an error to be inserted in the output QRSS pattern.

QSYNC/Test   QSYNC reads as "1" to indicate when the QRSS detector is synchronized to an input pattern. QSYNC is only valid when QDET = 1 enabling the pattern detector.
When writing this register, this bit must be set to "0" for normal operation.

QGEN   QRSS Generator Enable
When QGEN = 1, the QRSS generator is enabled. The QRSS pattern is output at the TTIP/TRING pins, or at the RPOS/RNEG (RDATA) pins, depending upon the state of the QRSSPATH bit. Errors can be generated using the QINS_ERR bit.

Test   Bit should be set to "0" for normal operation.

Data Pattern Error Count (DPEC): Address 0x15

7 (MSB)	6	5	4	3	2	1	0 (LSB)
DPEC.7	DPEC.6	DPEC.5	DPEC.4	DPEC.3	DPEC.2	DPEC.1	DPEC.0

DPEC[7:0]   Errors detected in the input QRSS pattern are counted and stored. This register saturates at 255 errors. The DPEC is cleared when the RST_ERR bit is written in the CR3 register.

Bits			Long Haul Mode Status
7	6	5	
0	0	0	Reset has occurred, or no program input
0	0	1	RLOOP active
0	1	0	LLOOP active
0	1	1	LOS has changed state since last Clear LOS occurred
1	0	0	TAOS active
1	0	1	NLOOP has changed state since last Clear NLOOP occurred
1	1	0	TAOS and LLOOP active
1	1	1	LOS and NLOOP have both changed state since last Clear NLOOP and Clear LOS

Table 4. Register 16 Decoding

Bits			Short Haul Mode Status
7	6	5	
0	0	0	Reset has occurred, or no program input
0	0	1	RLOOP active
0	1	0	LLOOP active
0	1	1	LOS has changed state since last Clear LOS occurred
1	0	0	TAOS active
1	0	1	Not used
1	1	0	TAOS and LLOOP active
1	1	1	Not Used

Table 5. Register 16 Decoding

The CS61581 is configured for Short Haul or Long Haul mode by using the serial port. Writing a "1" to SH/$\overline{LH}$ (CR2.0 = 1), places the device in Short Haul mode. Control Registers 1 and 2 are modified to reflect the configuration selected. Similarly E1 operation can be enabled by setting E1_LH to "1" (CR1.6 = 1), changing CR1.2 to "HDB3." The Control Register bit assignments are shown in Table 3.

An interrupt will occur ($\overline{INT}$ pulls low) in response to a change in the LOS, AIS or NLOOP bits. The interrupt is cleared when the host processor writes a "1" to the respective bit in the control register.

Writing a "1" to LOS or NLOOP over the serial interface has three effects:

1) The current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt).

2) Output data bits 5, 6 and 7 will be reset as appropriate.

3) Interrupts for the corresponding LOS and NLOOP will be prevented from occurring.

Writing a "0" to either LOS or NLOOP enables the corresponding interrupt for LOS and NLOOP.

Reading the registers returns their current status or setting. Register 16 outputs the status NLOOP and LOS and has bits 5, 6, and 7 encoded as shown in Tables 4 and 5.

Control Register 2 provides extended functionality as determined by the status of the short-haul/long-haul bit, SH/$\overline{LH}$. Control Register 3 and the Data Pattern Error Count register at addresses 0x14 and 0x15 relate to the QRSS (Quasi Random Signal Source) data generator and receiver.

Writing the arbitrary waveform RAM requires a deviation from normal serial port access. Register 19 is the RAM address register for the arbitrary waveform. Two consecutive address bytes are written; first the Address/Command Byte is written to address 0x13, followed by the address in RAM to be written. This dual address is then followed by the data byte for the waveform amplitude. There are 42 RAM byte locations (numbered h00 to h29).

Power On Reset / Reset

Upon power-up, the IC is held in a static state until the supply crosses a threshold of approximately 3 Volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, cal-

ibration of the transmit and receive sections commences. Because power up conditions can vary considerably, it is recommended that the device be reset after the power supply has stabilized to ensure a known initial operational condition.

The internal frequency generators can be calibrated only if a reference clock is present. The reference clock for the transmitter is provided by TCLK. The reference for the receiver is either the crystal oscillator or MCLK. If both the oscillator and MCLK are active, MCLK will be used as the reference source. The initial calibration should take less than 20 ms after pulses are input to the receiver.

In operation, the device is continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function forgoes any requirement to reset the line interface when in operation. However, a reset function is available which will reinitiate calibration and clear all registers and clear the Network Loopback function.

In Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. The reset will set all registers to "0" and initiate a calibration. A reset will also set LOS high in the Short Haul configuration.

In Hardware Mode, the CS61581 is reset by simultaneously setting RLOOP and LLOOP high for at least 200 ns. Hardware reset will clear Network Loopback functionality

Power Supply

The device operates from a single +5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. These pins should decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3 V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 47µF tantalum and 1.0µF mylar or ceramic capacitor

should be connected between TV+ and TGND, and a 0.1µF mylar or ceramic capacitor should be connected between RV+ and RGND. Place capacitors as closely as possible to their respective power supply pins. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

QRSS TEST MODE

In Host Mode, the CS61581 has the capability to generate and detect a QRSS (2^{20}-1 with 14 zeros max for T1; 2^{15}-1 for E1) test signal, in either the transmit or receive direction. Errors can be inserted and counted in the pattern. The QRSS test mode is controlled through Control Register 3, address 0x14. To initiate transmission the QRSS Signal on the TTIP and TRING leads, set QRSSPATH to "1" (CR3.7 = 1). Setting QGEN to "1" (CR3.1 = 1) initiates the pattern output. The QRSS pattern detector is enabled by writing a "1" to QDET (CR3.4 = 1).

When the detector synchronizes to an input pattern, QSYNC is set to "1." Errors detected in the received QRSS pattern are counted and stored in the Data Pattern Error Count, DPEC, register at address 0x15. An error can be inserted in the output data pattern by setting QINS_ERR bit to "1" then "0." The number of errors accumulated by the pattern detector are stored in the DPEC register. The DPEC register will accumulate to all ones, 255 errors, and stay at that level until reset. The DPEC register is reset to zero by setting the RST_ERR bit to "1" (CR3.3 = 1)

ARBITRARY WAVEFORM GENERATION

In addition to the predefined pulse shapes, the user can create custom pulse shapes using the host mode. This flexibility allows the board designer to accommodate non-standard cables, EMI filters, protection circuitry, etc.

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The arbitrary pulse shape of mark (a transmitted "1") is specified by describing it's pulse shape across three Unit Intervals (UIs). This allows, for example, the long-haul return-to-zero tail to extend into the next UI, or two UIs, as is required for isolated pulses.

Each UI is divided into multiple phases, and the users defines the amplitude of each phase. The waveform of a space (a transmitted "0") is fixed at zero volts. Examples of the phases are shown in Figure 12. In all cases, to define an arbitrary waveform, the user writes to the Waveform Register either 36, 39 or 42 times (12, 13 or 14 phases per UI for three UIs). The phases are written in the order: UI1/phase1, UI1/phase2, ... , UI1/phase14, UI2/phase1, ... , UI2/phase14, UI3/phase1, ... , UI3/phase14.

For E1, short haul applications the CS61581 divides the 488 ns UI into 12 uniform phases (40.7 ns
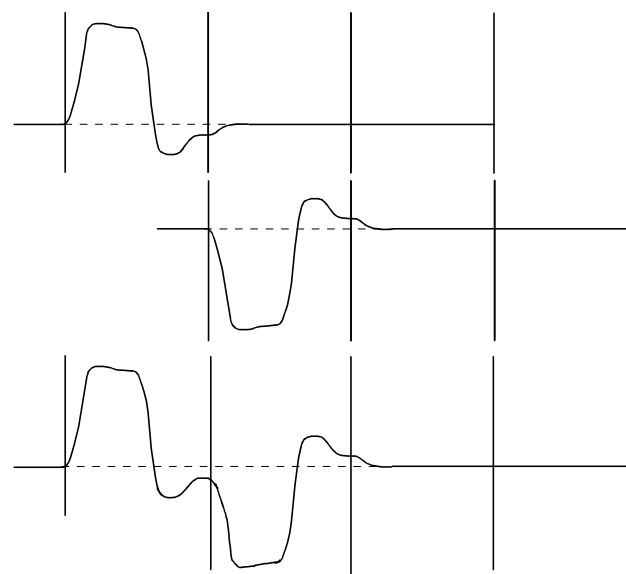

Figure 13. Example of Summing of Waveforms

each), and will ignore the phase amplitude information written for phases 13 and 14 of each UI.

For DSX-1 and DS1 applications, the CS61581 divides the 648 ns UI into 13 uniform phases (49.8 ns each), and will ignore the phase amplitude information written for phase 14 of each UI.

For E1 long haul applications, the CS61581 divides the 648 ns UI into 14 uniform phases (46.3 ns each), and uses the phase information written for all 14 phases of each UI.

When transmitting pulses, the CS61581 will add the amplitude information from the prior two symbols with the amplitude of the first UI of the current symbol before outputting a signal on TTIP/TRING. Therefore, a mark preceded by two spaces will be output exactly as the mark is programmed. However, when one mark is preceded by marks, the first portion of the last mark may be modified. With AMI data, where successive pulses have opposite polarity, the undershoot tail of one pulse will cause the rising edge of the next mark to rise more quickly, as shown in Figure 13.

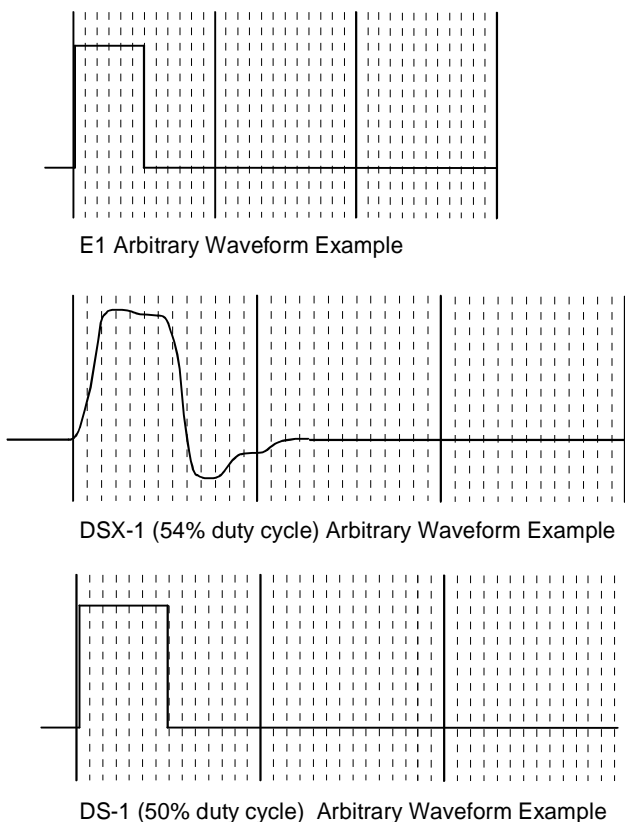The amplitude of each phase is described by a 7-bit, 2's compliment number, where a positive value de-

E1 Arbitrary Waveform Example

DSX-1 (54% duty cycle) Arbitrary Waveform Example

DS-1 (50% duty cycle) Arbitrary Waveform Example

Figure 12. Phase Definition of Arbitrary Waveforms

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scribes pulse amplitude, and a negative value describes pulse undershoot. The positive full value is hex 3F. The negative full value is hex 40. For T1, the typical output voltage is 38 mV/LSB. For E1 coax, the typical output voltage is 22 mV/LSB. For E1 shielded twisted pair, the typical output voltage is 27 mV/LSB. All voltages are peak voltages across the TTIP and TRING outputs.

On the secondary of a 1:2 step-up transformer, the mV/LSB is twice the values stated above. Note that although the full scale digital input is 3F, it is recommended that full scale output voltage on the transformer primary be limited to 2.4 Vpk. At higher output voltages, the driver may not drive the requested output voltage.

The amplitude information for all phases is written via the serial-port to Arbitrary Pulse Shape registers as described in an earlier section. Each phase amplitude is written as an eight-bit byte, where the first phase of the symbol is written first.

In serial-port host mode, the amplitude bytes are written LSB first. The contents of the Arbitrary Waveform register can be verified by performing a read.

For arbitrary waveform operation, the transmitter output impedance is controlled in short haul mode by setting the LEN 2/1/0 bits.

LEN2/1/0   output impedance

0/0/0	75Ω
0/0/1	120Ω
0/1/1	100Ω
0/1/0	100Ω, 6V pulse

For long haul operation, driver impedance is determined by the desired selection of MATCHZ and E1_LH bits. When MATCHZ is set to "0" the output impedance is low. When MATCHZ is set to 1, E1_LH determines whether the driver is set for 100Ω (E1_LH = 0) or 120Ω (E1_LH = 1).

Diagnostic Mode	Availability (Note 25)		Host Mode (Note 26) Maskable
	H/W	Host	
Loopback Modes			
Local Loopback (LLOOP)	Yes	Yes	No
Remote Loopback (RLOOP)	Yes	Yes	No
In-band Network Loopback (NLOOP)	Yes	Yes	Yes
Internal Data Pattern Generation and Detection			
Transmit All Ones (TAOS)	Yes	Yes	No
Quasi-Random Signal Source (QRSS)	No	Yes	No
In-band Loop-up/down Code Generator	No	Yes	No
Error Insertion and Detection			
Quasi-Random Signal Detection (QDET)	No	Yes	No
Quasi-Random Signal Error Insertion (QINS_ERR)	No	Yes	No
Bipolar Violation Detection (BPV)	Yes	Yes	No
Alarm Condition Monitoring			
Receive Loss of Signal Monitoring (LOS)	Yes	Yes	Yes
Receive Alarm Indication Signal Monitoring (AIS)	No	Yes	Yes
Other Diagnostic Reports			
Receive Line Attenuation Indicator (LATN)	Yes	Yes	No

Table 5. CS61581 Diagnostic Mode Availability

Notes: 25. In Hardware Mode the Diagnostic Modes are selected by directly setting the pins on the device; in Host Mode, the appropriate register bits are written for Diagnostic Modes.

26. In Host Mode the interrupts can be masked by writing a "1" to the LOS bit; there is no masking in the Hardware Mode.

CIRRUS LOGIC PRODUCT DATA SHEET

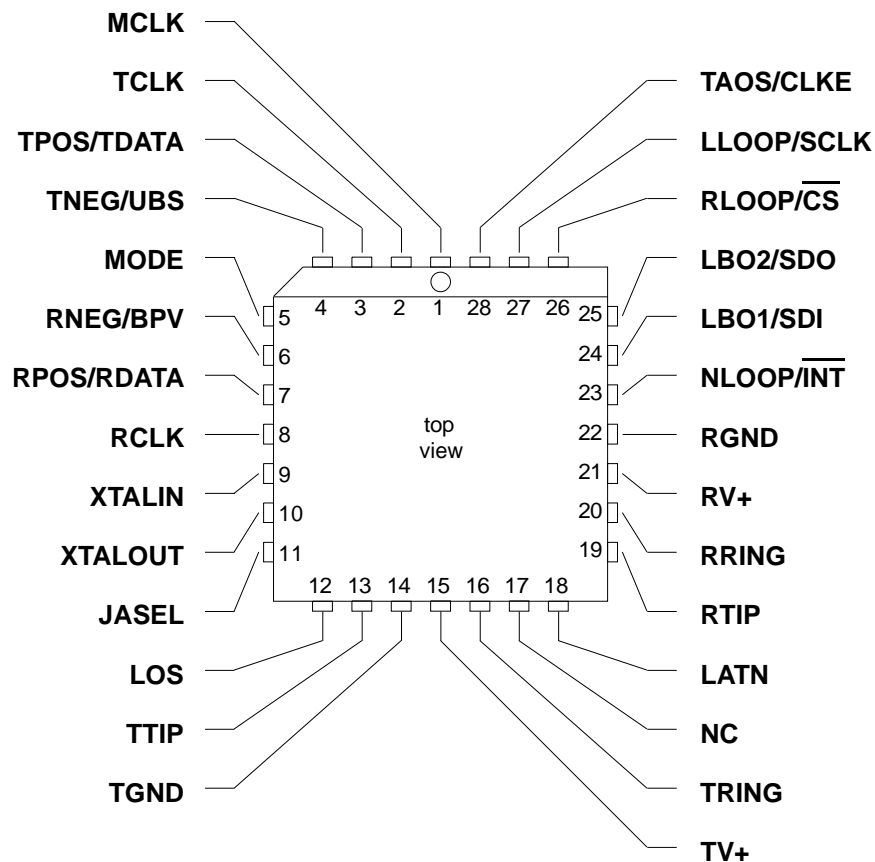| Turns ratio: Low Impedance Output/Hardware Mode	1:2 step-up transmit, 1:1 receive
Turns ratio: Matched Impedance Output	1:1.5 step-up transmit, 1:1 receive
Primary inductance	1.2 mH min at 772 kHz
Primary leakage inductance	0.5 µH max at 772 kHz with secondary shorted
Secondary leakage inductance	0.5 µH max at 772 kHz
Interwinding capacitance	40 pF max, primary to secondary
ET-constant	16 V-µs min

Table 6. Transformer Specification

Turns Ratio(s)	Manufacturer	Part Number	Package Type
1:1CT	Pulse Engineering	PE-64936	1.5 kV, through-hole, single
	Valor	PT5008	
	Schott	67130840	
	Valor	ST5085	1.5 kV, surface mount, single
	Schott	31187	
1:2CT	Pulse Engineering	PE-65351	1.5 kV, through-hole, single
	Valor	PT5004	
	Schott	617130850	
	Valor	ST5086	1.5 kV, surface mount, single
	Schott	31188	
1:1.5CT	Pulse Engineering	T-1054	1.5 kV, through-hole, single
	Schott	31705	
	Valor	ST5074	1.5 kV, surface mount, single
	Schott	31706	
1:1CT 1:2CT	Pulse Engineering	PE-68678	1.5 kV, surface mount, dual
	Valor	ST5162	
	Pulse Engineering	PE-68877	1.5 kV, surface mount, dual extended temp.
	Pulse Engineering	T-1068	1.5 kV, surface mount, quad port
	Valor	ST5173	
	Pulse Engineering	T-1031	3 kV, surface mount, dual
1:1CT 1:1.5CT	Pulse Engineering	T-1022	1.5 kV, surface mount, dual
	Valor	ST5221	
	Pulse Engineering	T-1077	1.5 kV, surface mount, dual extended temp
	Pulse Engineering	T-1081	3 kV, surface mount, dual

Table 7. Recommended Tranformers for the CS61581

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PIN DESCRIPTION

MCLK	1	28	TAOS/CLKE
TCLK	2	27	LLOOP/SCLK
TPOS/TDATA	3	26	RLOOP/$\overline{CS}$
TNEG/UBS	4	25	LBO2/SDO
MODE	5	24	LBO1/SDI
RNEG/BPV	6	23	NLOOP/$\overline{INT}$
RPOS/RDATA	7	22	RGND
RCLK	8	21	RV+
XTALIN	9	20	RRING
XTALOUT	10	19	RTIP
JASEL	11	18	LATN
LOS	12	17	NC
TTIP	13	16	TRING
TGND	14	15	TV+

MCLK
TCLK   **TAOS/CLKE**
TPOS/TDATA   **LLOOP/SCLK**
TNEG/UBS   **RLOOP/$\overline{CS}$**
MODE   **LBO2/SDO**
RNEG/BPV   5 4 3 2 1 28 27 26 25   **LBO1/SDI**
                                            24   **NLOOP/$\overline{INT}$**
RPOS/RDATA 6   23
RCLK   7   22   **RGND**
XTALIN   8   top   21   **RV+**
XTALOUT   9   view   20   **RRING**
JASEL   10   19   **RTIP**
                11
                12 13 14 15 16 17 18   **LATN**
LOS   **NC**
TTIP   **TRING**
TGND   **TV+**

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CIRRUS LOGIC

POWER SUPPLIES

TV+ - Power Supply, Transmit Driver, Pin 15.

Power supply for the transmit driver; typically +5 Volts.

TGND - Ground Transmit Driver, Pin 14.

Power supply ground for the transmit driver; typically 0 Volts.

RV+ - Power Supply, Pin 21.

Power supply for all subcircuits except the transmit driver; typically +5 Volts.

RGND - Ground, Pin 22.

Power supply ground for all subcircuits except the transmit driver; typically 0 Volts.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.

A 6.176 MHz (or 8.192 MHz) crystal can be connected across these pins. This oscillator provides the reference frequency for the LIU if MCLK is not provided. The load capacitance presented to the crystal by these pins should be approximately 19pF (IC and package, when soldered into a circuit board). The jitter attenuator may be disabled by tying pin 9 to RV+ through a 1kΩ resistor, and floating XTALOUT. When pin 9 has no clock input, a clock must be supplied to the MCLK pin. Alternatively an external 6.176 MHz (8.192 MHz) clock can be driven into pin 9, and the jitter attenuator circuit will operate.

If MCLK is provided, and XTALIN is tied low or floated, the jitter attenuator will be enabled.

Control

MCLK - Master Clock Input, Pin 1.

Either MCLK or the crystal oscillator provide the master frequency reference for the CS61581. If both MCLK and the crystal oscillator are present, the oscillator is ignored. MCLK should be 1.544 MHz for T1 and 2.048 MHz) for E1. In a Loss of Signal state, RCLK will be derived from MCLK, through the jitter attenuator, if active. If MCLK is not provided, the jitter attenuator will hold the RCLK frequency in a Loss of Signal state. MCLK should be grounded if it is not used.

MODE - Mode Select Input, Pin 5.

Setting the MODE pin high puts the CS61581 into Host Mode where the device is controlled by a microprocessor, via a serial port. Setting the MODE pin low, configures the part for hardware mode control where various control and status are provided on dedicated pins. The MODE pin is internally pulled down placing the part in Hardware Mode when this pin is left floating. Tying the MODE pin to RCLK places the chip in Hardware Mode and enables the B8ZS encoder/decoder (provided that coder mode has been enabled; see the description for TNEG/UBS pin).

TAOS - Transmit All Ones Select Input, Pin 28 (Hardware Mode).

Setting TAOS to logic 1 causes continuous ones to be transmitted at the TCLK frequency. When TAOS is high, TPOS and TNEG (TDATA) are not output at the TTIP/TRING pins. TAOS is overridden by Remote Loopback. Setting TAOS, LLOOP, and RLOOP high simultaneously enables Network Loopback detection.

LLOOP - Local Loopback Input, Pin 27(Hardware Mode).

Setting LLOOP to a logic 1 internally routes the transmitter input to the receiver output. If TAOS is low, the signal being output from the transmitter will be internally routed to the receiver inputs allowing nearly the entire chip to be tested. If TAOS and LLOOP are set high at the same time, the local loopback will occur at the jitter attenuator (excluding the transmit and receive circuitry) and the transmitter will transmit all ones. Simultaneously setting RLOOP and LLOOP high while TAOS is low resets the CS61581. Simultaneously setting RLOOP, LLOOP and TAOS high enables Network Loopback detection.

RLOOP - Remote Loopback Input, Pin 26 (Hardware Mode).

Setting RLOOP to a logic 1 causes the received signal to be passed through the jitter attenuator (if active) and retransmitted onto the line. The internal encoders/decoders will be bypassed in Remote Loopback. Simultaneously setting RLOOP and LLOOP high while TAOS is low resets the CS61581. Simultaneously setting RLOOP, LLOOP and TAOS high enables Network Loopback detection.

LBO1, LBO2 - Line Build Out 1 and 2, Pins 24 and 25 (Hardware Mode).

Transmitted line build out pulse shapes are selected by setting LBO1/2: 0/0 = 0 dB, 0/1 = -7.5 dB, 1/0 = -15 dB, and 1/1 = -22.5 dB.

JASEL - Jitter Attenuator Select, Pin 11.

If the jitter attenuator is enabled (crystal oscillator active, or XTALIN tied low or floated with MCLK provided), setting JASEL high places the jitter attenuator in the receive path; setting JASEL low places the jitter attenuator in the transmit path.

NC - No Connect, Pin 17.

The input voltage to this pin does not effect normal operation.

Status

LOS - Loss Of Signal Output, Pin 12.

LOS goes high when 175 consecutive zeros are received. LOS returns low when the ones density reaches 12.5% (based on 175 consecutive bit periods, starting with a one and containing less than 100 consecutive zeros, as prescribed in ANSI T1.231-1993 and ITU-T G.775). If LOS is true, and the jitter attenuator is in the receive path, RCLK will smoothly transition to MCLK if provided; RCLK will retain the frequency prior to LOS if MCLK is grounded. If the jitter attenuator is NOT in the receive path, RCLK will become the reference clock frequency (MCLK) if provided, or the crystal oscillator.

NLOOP - Network Loopback Output, Pin 23 (Hardware Mode).

NLOOP goes high when a 00001 pattern is received for five seconds putting the CS61581 into network (remote) loopback. NLOOP is deactivated upon receipt of a 001 pattern for five seconds, or by selection of LLOOP or RLOOP.

LATN - Line Attenuation Indication Output, Pin 18.

LATN is an encoded output that indicates the receive equalizer gain setting in relation to a five RCLK cycle period. If LATN is high for one RCLK cycle, the equalizer is set for 7.5 dB gain, two cycles = 15 dB gain, three cycles = 22.5 dB gain, four cycles = 0 dB. LATN may be sampled on the rising edge of RCLK.

Serial Control Interface

$\overline{\text{INT}}$ - Interrupt Output, Pin 23 (Host Mode).

$\overline{\text{INT}}$ pulls low to flag the host processor when NLOOP, AIS or LOS changes state. $\overline{\text{INT}}$ is an open drain output and should be tied to the supply through a resistor.

SDI - Serial Data Input, Pin 24 (Host Mode).

Data input to the on-chip register is sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25 (Host Mode).

Status and control information are output from the on-chip register on SDO. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low, SDO is valid on the falling edge of SCLK. SDO goes to a high-impedance state when the serial port is being written to, or after bit D7 is output or $\overline{\text{CS}}$ goes high (whichever occurs first).

CS - Chip Select, Pin 26 (Host Mode).

The serial interface is accessible when $\overline{\text{CS}}$ transitions from high to low.

SCLK - Serial Clock Input, Pin 27 (Host Mode).

SCLK is used to write or read data bits to or from the serial port registers.

CLKE - Clock Edge, Pin 28 (Host Mode).

Setting CLKE to logic 1 causes RPOS and RNEG (RDATA) to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG (RDATA) to be valid on the rising edge of RCLK and SDO to be valid on the falling edge of SCLK.

Data Input/Output

TCLK - Transmit Clock Input, Pin 2.

The 1.544 MHz (2.048 MHz) transmit clock is input on this pin. TPOS and TNEG or TDATA are sampled on the falling edge of TCLK.

TPOS/TNEG - Transmit Positive Pulse, Transmit Negative Pulse, Pins 3 and 4.

Data input to TPOS and TNEG is sampled on the falling edge of TCLK and transmitted onto the line at TTIP and TRING. An input on TPOS results in transmission of a positive pulse; an input on TNEG results in transmission of a negative pulse. If TNEG, pin 4, is held high for 16 TCLK cycles, the CS61581 reconfigures for unipolar (single pin NRZ) data input at pin 3, TDATA. If pin 4 goes low the CS61581 switches back to two-pin bipolar data input format.

TDATA - Transmit Data, Pin 3.

When pin 4, TNEG/UBS, is held high, pin 3 becomes TDATA, a single-line NRZ (unipolar) data input sampled on the falling edge of TCLK.

UBS - Unipolar / Bipolar Select, Pin 4.

When UBS is held high for 16 consecutive TCLK cycles (15 consecutive bipolar violations) the CS61581 reconfigures for unipolar (single-line NRZ) data input / output format. Pin 3 becomes TDATA, pin 7 becomes RDATA, and pin 6 becomes BPV.

RCLK - Recovered Clock Output, Pin 8.

RCLK outputs the clock recovered from the input signal at RTIP and RRING. In a Loss of Signal state RCLK reverts to the MCLK frequency, or retains the frequency prior to the LOS state, depending on the clocks provided. See the LOS pin description.

RNEG/RPOS - Receive Negative Pulse, Receive Positive Pulse, Pins 6 and 7.

Recovered data output on RPOS and RNEG is stable and valid on the rising edge of RCLK in Hardware Mode. In Host Mode, CLKE determines the edge of RCLK on which RPOS and RNEG are valid. A positive pulse on RTIP with respect to RRING generates a logic 1 on RPOS; a positive pulse on RRING with respect to RTIP generates a logic 1 on RNEG.

RDATA - Received Data, Pin 7.

Unipolar data (single-line NRZ) data is output on RDATA when pin 4, TNEG/UBS, is held high.

BPV - Bipolar Violation, Pin 6.

When pin 4 is held high, received bipolar violations are flagged by BPV (RNEG) going high along with the offending bit output from RDATA. If the B8ZS or HDB3 encoder/decoder is activated, BPV will not flag bipolar violations resulting from valid zero substitutions.

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28 PIN PLASTIC (PDIP) PACKAGE DRAWING

TOP VIEW

SEATING PLANE

BOTTOM VIEW

SIDE VIEW
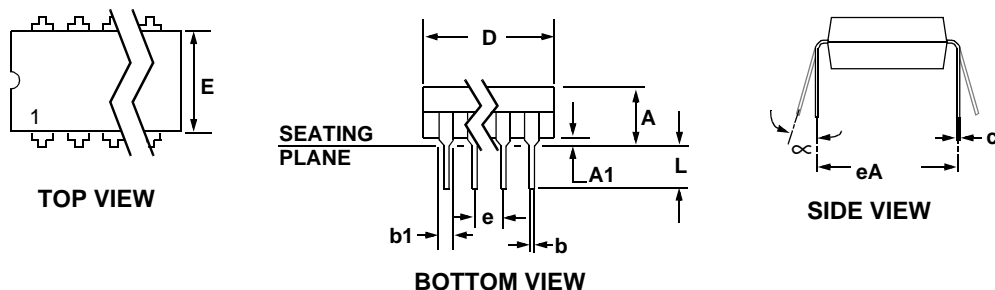
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.155	0.200	3.94	5.08
A1	0.020	0.040	0.51	1.02
b	0.014	0.022	0.36	0.56
b1	0.040	0.065	1.02	1.65
c	0.008	0.015	0.20	0.38
D	1.435	1.465	36.45	36.83
E	0.540	0.560	13.72	14.22
e	0.095	0.105	2.41	2.67
eA	0.600	0.625	15.24	15.87
L	0.125	0.150	3.18	3.81
∝	0°	15°	0°	15°

Notes: 1. Positional tolerance of leads shall be within 0.25 mm (0.010 in.) at maximum material condition, in relation to seating plane and each other.

2. Dimension eA to center of leads when formed parallel.

3. Dimension E does not include mold flash.

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28L PLCC PACKAGE DRAWING
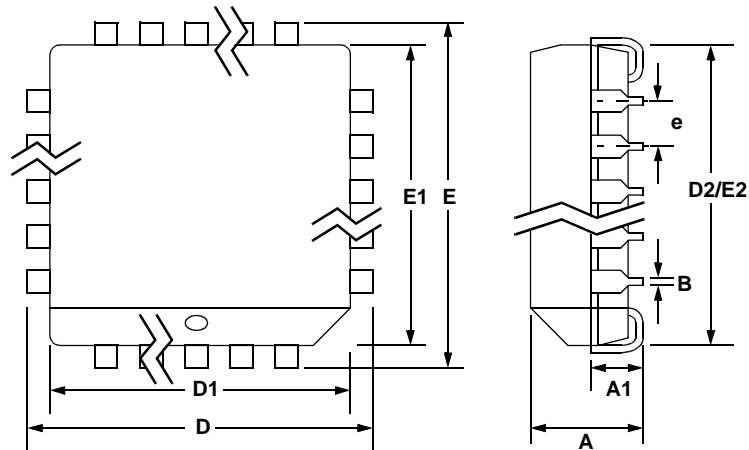
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.043	4.572
A1	0.090	0.120	2.205	3.048
B	0.013	0.021	0.319	0.533
D	0.485	0.495	11.883	12.573
D1	0.450	0.456	11.025	11.582
D2	0.390	0.430	9.555	10.922
E	0.485	0.495	11.883	12.573
E1	0.450	0.456	11.025	11.582
E2	0.390	0.430	9.555	10.922
e	0.040	0.060	0.980	1.524

JEDEC # : MS-018

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APPLICATIONS
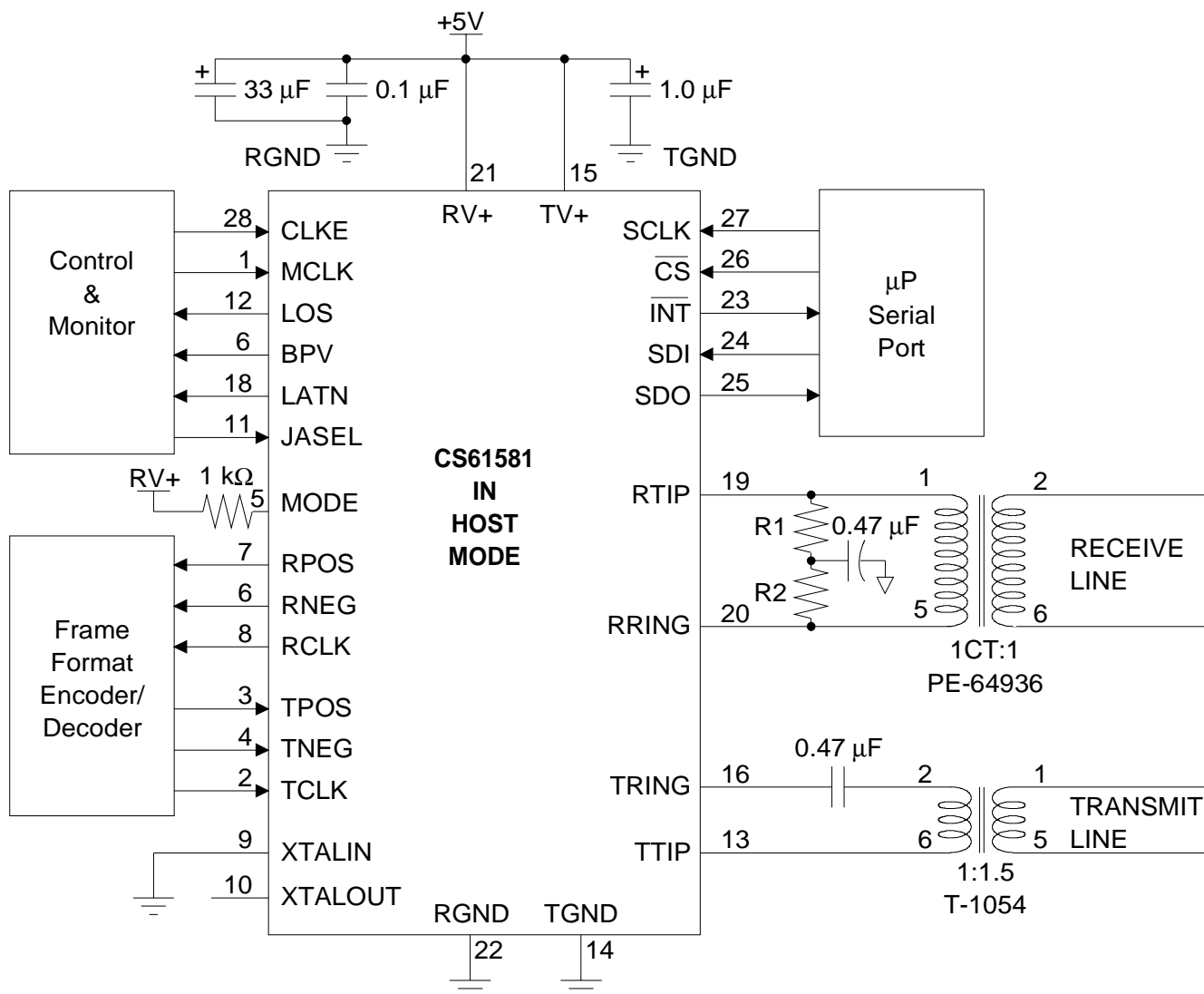
Figure 14. Matched Impedance Output Configuration

	T1 **100 Ω**	**E1** **75 Ω**	**E1** **120 Ω**
R1 (Ω)	50	37.5	60
R2 (Ω)	50	37.5	60

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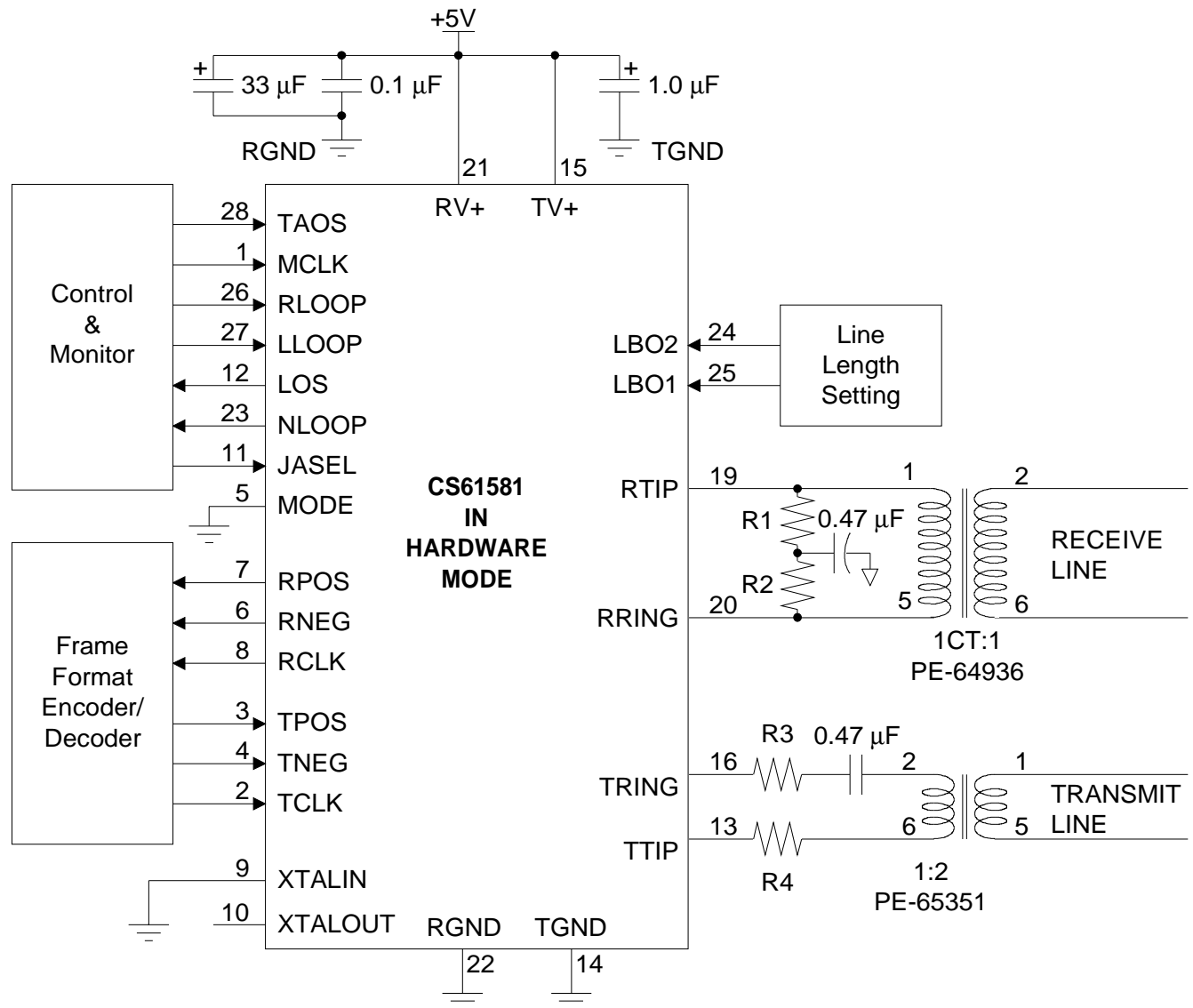
Figure 15. Low Impedance Output Configuration

	T1 **100 Ω**	**E1** **75 Ω**	**E1** **120 Ω**
R1 (Ω)	50	37.5	60
R2 (Ω)	50	37.5	60
R3 (Ω)	9.1	9.1	9.1
R4 (Ω)	9.1	9.1	9.1

CIRRUS LOGIC PRODUCT DATA SHEET
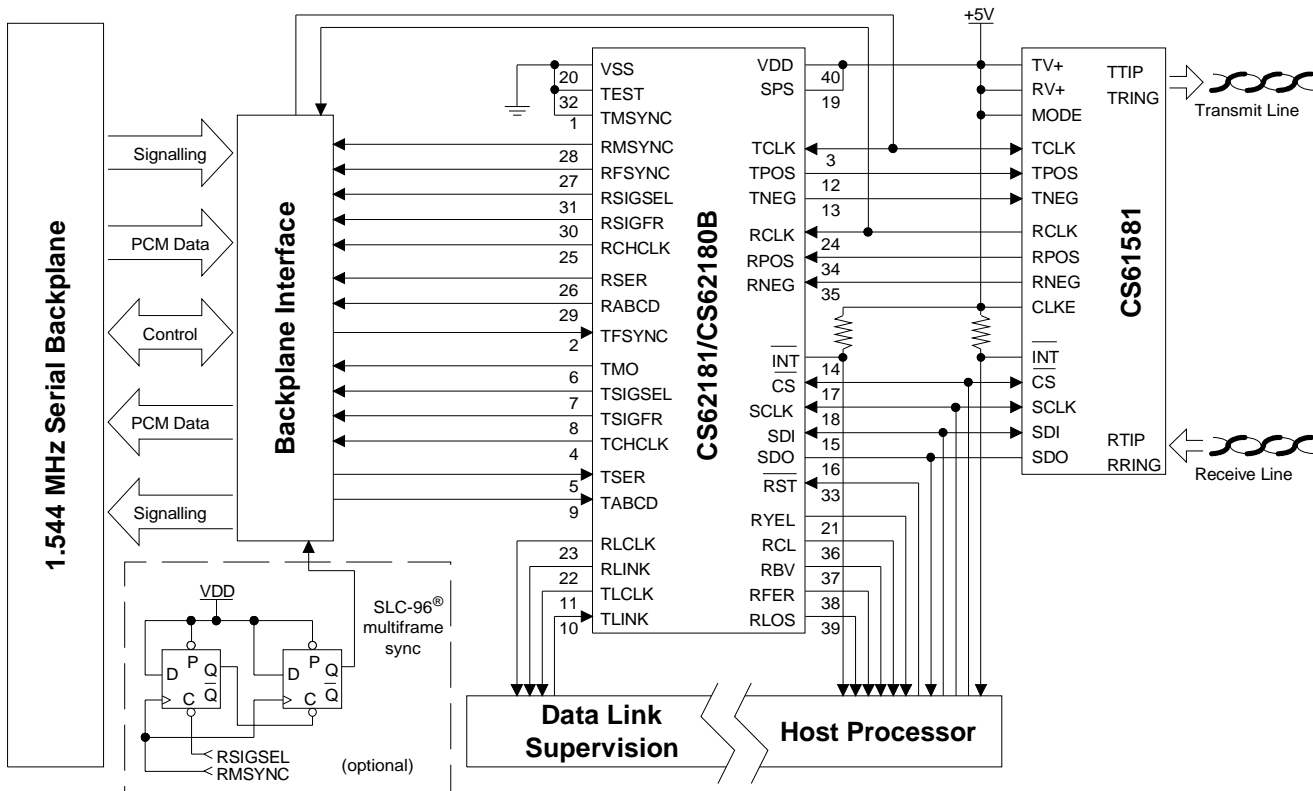
Figure 16. Typical System Connection

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• Notes •

SMART Analog™