A DIVISION OF CIRRUS LOGIC

**CS5522/24/28**

# *2-, 4-, or 8-Channel, 24-Bit Buffered ΔΣ Multi-Range ADC*

## Features

- Delta-Sigma A/D Converter
  - Linearity Error: 0.0007%FS
  - Noise Free Resolution: 18-bits
- Buffered Bipolar/Unipolar Input Ranges
  - 25 mV, 55 mV, 100 mV, 1 V, 2.5 V and 5 V
- Chopper Stabilized Instrumentation Amplifier
- On-Chip Charge Pump Drive Circuitry
- Multiplexer
- Conversion Data FIFO
- Programmable/Auto Channel Sequencer
- 2-Bit Output Latch
- Simple three-wire serial interface
  - SPI™ and Microwire™ Compatible
  - Schmitt Trigger on Serial Clock (SCLK)
- Output Settles in One Conversion Cycle
- 50/60 Hz ±3 Hz Simultaneous Rejection
- Buffered $V_{REF}$ with +5 V Input Capability
- System and Self-Calibration with R/W Registers per Channel
- Single +5 V Analog Supply
  +3.0 V or +5 V Digital Supply
- Low Power Mode Consumption: 5.5 mW

## General Description

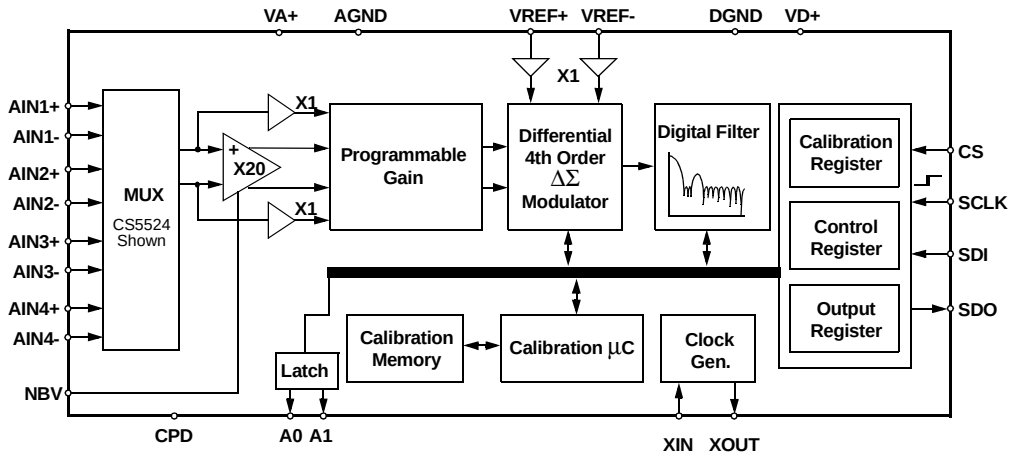
The 24-bit CS5522/24/28 are highly integrated ΔΣ A/D converters which include an instrumentation amplifier, a PGA (programmable gain amplifier), a multi-channel multiplexer, digital filters, and self and system calibration circuitry.

The chips are designed to provide their own negative supply which enables their on-chip instrumentation amplifiers to measure bipolar ground-referenced signals less-than or equal to ±100 mV.

The digital filters provide programmable output update rates of 1.88 Hz, 3.76 Hz, 7.51 Hz, 15 Hz, 30 Hz, 61.6 Hz, 84.5 Hz, and 101.1 Hz when operating from a 32 kHz crystal. The CS5522/24/28 are capable of producing output update rates up to 303 Hz with a 100kHz clock. The filters are designed to settle to full accuracy for the selected output update rate within one conversion cycle. When operated at word rates of 15 Hz or less, the digital filters reject both 50 and 60 Hz line interference ±3 Hz simultaneously.

Low power, single conversion settling time, programmable output rates, and the ability to handle negative input signals make these single supply products ideal solutions for isolated and non-isolated applications.

**ORDERING INFORMATION**
See page 34.




*Preliminary Product Information* | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ***Accuracy*** | | | | | |
| Resolution | | - | - | 24 | Bits |
| Linearity Error | | - | ±0.0007 | ±0.0015 | %FS |
| Bipolar Offset | (Note 3) | - | ±16 | ±32 | $LSB_{24}$ |
| Unipolar Offset | (Note 3) | - | ±32 | ±64 | $LSB_{24}$ |
| Offset Drift | (Notes 3 and 4) | - | 20 | - | nV/°C |
| Bipolar Gain Error | | - | ±8 | ±31 | ppm |
| Unipolar Gain Error | | - | ±16 | ±62 | ppm |
| Gain Drift | (Note 4) | - | 1 | 3 | ppm/°C |
| ***Voltage Reference Input*** | | | | | |
| Range | (VREF+) - (VREF-) | 1 | 2.5 | VA+ | V |
| VREF+ | | (VREF-)+1 | - | VA+ | V |
| VREF- | | NBV | - | (VREF+)-1 | V |
| Common Mode Rejection | dc | - | 110 | - | dB |
| | 50, 60 Hz | - | 130 | - | dB |
| Input Capacitance | | - | 16 | - | pF |
| CVF Current | (Note 5) | - | 5 | - | nA |

Notes: 1. Applies after system calibration at any temperature within -40 °C ~ +85 °C.
2. Specifications guaranteed by design, characterization, and/or test.
3. Specification applies to the device only and does not include any effects by external parasitic thermocouples.
4. Drift over specified temperature range after calibration at power-up at 25 °C.
5. See the section of the data sheet which discusses input models.

## RMS NOISE (Notes 6 and 7)

| Output Rate (Hz) | -3 dB Filter Frequency | Input Range, (Bipolar/Unipolar Mode) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 25 mV | 55 mV | 100 mV | 1 V | 2.5 V | 5 V |
| 1.88 | 1.64 | 90 nV | 90 nV | 130 nV | 1 µV | 2 µV | 4 µV |
| 3.76 | 3.27 | 110 nV | 130 nV | 190 nV | 1.5 µV | 3 µV | 7 µV |
| 7.51 | 6.55 | 170 nV | 200 nV | 250 nV | 2 µV | 5 µV | 10 µV |
| 15.0 | 12.7 | 250 nV | 300 nV | 500 nV | 4 µV | 10 µV | 15 µV |
| 30.0 | 25.4 | 500 nV | 1 µV | 1.5 µV | 15 µV | 45 µV | 85 µV |
| 61.6 | 50.4 | 2 µV | 4 µV | 8 µV | 72 µV | 190 µV | 350 µV |
| 84.5 (Note 8) | 70.7 | 10 µV | 20 µV | 30 µV | 340 µV | 900 µV | 2 mV |
| 101.1 (Note 8) | 84.6 | 30 µV | 55 µV | 105 µV | 1.1 mV | 2.4 mV | 5.3 mV |

Notes: 6. Wideband noise aliased into the baseband. Referred to the input. Typical values shown for 25 °C.
7. For Peak-to-Peak Noise multiply by 6.6 for all ranges and output rates.
8. For input ranges <100 mV and output rates >60 Hz, 16.384 kHz chopping frequency is used.

## ANALOG CHARACTERISTICS (Continued)

| Parameter | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ***Analog Input*** | | | | | | |
| Common Mode + Signal on AIN+ or AIN- | | Bipolar/Unipolar Mode | | | | |
| NBV = -1.8 to -2.5 V | Range = 25 mV, 55 mV, or 100 mV | | -0.150 | - | 0.950 | V |
| | Range = 1 V, 2.5 V, or 5 V | | NBV | - | VA+ | V |
| NBV = AGND | Range = 25 mV, 55 mV, or 100 mV | | 1.85 | - | 2.65 | V |
| | Range = 1 V, 2.5 V, or 5 V | | 0.0 | - | VA+ | V |
| Common Mode Rejection | dc | | - | 120 | - | dB |
| | 50, 60 Hz | | - | 120 | - | dB |
| Input Capacitance | | | - | 10 | - | pF |
| CVF Current on AIN+ or AIN- | | (Note 5) | | | | |
| | Range = 25 mV, 55 mV, or 100 mV | | - | 100 | 300 | pA |
| | Range = 1 V, 2.5 V, or 5 V | | - | 10 | - | nA |
| ***System Calibration Specifications*** | | | | | | |
| Full Scale Calibration Range | | Bipolar/Unipolar Mode | | | | |
| | 25 mV | | 10 | - | 32.5 | mV |
| | 55 mV | | 25 | - | 71.5 | mV |
| | 100 mV | | 40 | - | 105 | mV |
| | 1 V | | 0.40 | - | 1.30 | V |
| | 2.5 V | | 1.0 | - | 3.25 | V |
| | 5 V | | 2.0 | - | VA+ | V |
| Offset Calibration Range | | Bipolar/Unipolar Mode | | | | |
| | 25 mV | | - | - | ±12.5 | mV |
| | 55 mV | | - | - | ±27.5 | mV |
| | 100 mV | (Note 9) | - | - | ±50 | mV |
| | 1 V | | - | - | ±0.5 | V |
| | 2.5 V | | - | - | ±1.25 | V |
| | 5 V | | - | - | ±2.50 | V |
| ***Power Supplies*** | | | | | | |
| DC Power Supply Currents (Normal Mode) | | $I_{A+}$ | - | 1.5 | 1.9 | mA |
| | | (Note 10)$I_{D+}$ | - | 90 | 135 | µA |
| | | $I_{NBV}$ | - | 525 | 700 | µA |
| Power Consumption | Normal Mode | (Note 11) | - | 9 | 12 | mW |
| | Low Power Mode | | - | 5.5 | 7 | mW |
| | Standby | | - | 1.2 | - | mW |
| | Sleep | | - | 500 | - | µW |
| Power Supply Rejection | dc Positive Supplies | | - | 120 | - | dB |
| | dc NBV | | - | 110 | - | dB |

Notes: 9. The maximum full scale signal can be limited by saturation of circuitry within the internal signal path.

10. Measured with Charge Pump Drive off.

11. All outputs unloaded. All input CMOS levels.

## 5 V DIGITAL CHARACTERISTICS ($T_A$ = 25 °C; VA+, VD+ = 5 V ±5%; GND = 0; See Notes 2 and 12.))

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High-Level Input Voltage | All Pins Except XIN and SCLK | $V_{IH}$ | 0.6 VD+ | - | - | V |
| | XIN | | (VD+)-0.5 | - | - | V |
| | SCLK | | (VD+) - 0.45 | - | - | V |
| Low-Level Input Voltage | All Pins Except XIN and SCLK | $V_{IL}$ | - | - | 0.8 | V |
| | XIN | | - | - | 1.5 | V |
| | SCLK | | - | - | 0.6 | V |
| High-Level Output Voltage | | $V_{OH}$ | | | | |
| | All Pins Except CPD and SDO (Note 13) | | (VA+) - 1.0 | - | - | V |
| | CPD, $I_{out}$ = -4.0 mA | | (VD+) - 1.0 | - | - | V |
| | SDO, $I_{out}$ = -5.0 mA | | (VD+) - 1.0 | - | - | V |
| Low-Level Output Voltage | | $V_{OL}$ | | | | |
| | All Pins Except CPD and SDO, $I_{out}$ = 1.6 mA | | - | - | 0.4 | V |
| | CPD, $I_{out}$ = 2 mA | | - | - | 0.4 | V |
| | SDO, $I_{out}$ = 5.0 mA | | - | - | 0.4 | V |
| Input Leakage Current | | $I_{in}$ | - | ±1 | ±10 | µA |
| 3-State Leakage Current | | $I_{OZ}$ | - | - | ±10 | µA |
| Digital Output Pin Capacitance | | $C_{out}$ | - | 9 | - | pF |

Notes: 12. All measurements performed under static conditions.

13. $I_{out}$ = -100 µA unless stated otherwise. ($V_{OH}$ = 2.4 V @ $I_{out}$ = -40 µA.)

## 3 V DIGITAL CHARACTERISTICS ($T_A$ = 25 °C; VA+ = 5 V ±5%; VD+ = 3.0 V ±10%; GND = 0; See Notes 2 and 12.)

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High-Level Input Voltage | All Pins Except XIN and SCLK | $V_{IH}$ | 0.6 VD+ | - | - | V |
| | XIN | | (VD+)-0.5 | - | - | V |
| | SCLK | | (VD+) - 0.45 | - | - | V |
| Low-Level Input Voltage | All Pins Except XIN and SCLK | $V_{IL}$ | - | - | 0.16 VD+ | V |
| | XIN | | - | - | 0.3 | V |
| | SCLK | | - | - | 0.6 | V |
| High-Level Output Voltage | | $V_{OH}$ | | | | |
| | All Pins Except CPD and SDO, $I_{out}$ = -400 µA | | (VA+) - 0.3 | - | - | V |
| | CPD, $I_{out}$ = -4.0 mA | | (VD+) - 1.0 | - | - | V |
| | SDO, $I_{out}$ = -5.0 mA | | (VD+) - 1.0 | - | - | V |
| Low-Level Output Voltage | | $V_{OL}$ | | | | |
| | All Pins Except CPD and SDO, $I_{out}$ = 400 µA | | - | - | 0.3 | V |
| | CPD, $I_{out}$ = 2 mA | | - | - | 0.4 | V |
| | SDO, $I_{out}$ = 5.0 mA | | - | - | 0.4 | V |
| Input Leakage Current | | $I_{in}$ | - | ±1 | ±10 | µA |
| 3-State Leakage Current | | $I_{OZ}$ | - | - | ±10 | µA |
| Digital Output Pin Capacitance | | $C_{out}$ | - | 9 | - | pF |

## DYNAMIC CHARACTERISTICS

| Parameter | Symbol | Ratio | Unit |
|---|---|---|---|
| Modulator Sampling Frequency | $f_s$ | XIN/4 | Hz |
| Filter Settling Time to 1/2 LSB (Full Scale Step) | $t_s$ | $1/f_{out}$ | s |

## RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0 V; See Note 14.))

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DC Power Supplies | Positive Digital | VD+ | 2.7 | 5.0 | 5.25 | V |
| | Positive Analog | VA+ | 4.75 | 5.0 | 5.25 | V |
| Analog Reference Voltage | (VREF+) - (VREF-) | $VRef_{diff}$ | 1.0 | 2.5 | VA+ | V |
| Negative Bias Voltage | | NBV | -1.8 | -2.1 | -2.5 | V |

Notes: 14. All voltages with respect to ground.

## ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V; See Note 14.)

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DC Power Supplies | (Note 15) | | | | | |
| | Positive Digital | VD+ | -0.3 | - | +6.0 | V |
| | Positive Analog | VA+ | -0.3 | - | +6.0 | V |
| Negative Bias Voltage | Negative Potential | NBV | +0.3 | -2.1 | -3.0 | V |
| Input Current, Any Pin Except Supplies | (Note 16 and 17) | $I_{IN}$ | - | - | ±10 | mA |
| Output Current | | $I_{OUT}$ | - | - | ±25 | mA |
| Power Dissipation | (Note 18) | PDN | - | - | 500 | mW |
| Analog Input Voltage | VREF pins | $V_{INR}$ | NBV -0.3 | - | (VA+) + 0.3 | V |
| | AIN Pins | $V_{INA}$ | NBV -0.3 | - | (VA+) + 0.3 | V |
| Digital Input Voltage | | $V_{IND}$ | -0.3 | - | (VD+) + 0.3 | V |
| Ambient Operating Temperature | | $T_A$ | -40 | - | 85 | °C |
| Storage Temperature | | $T_{stg}$ | -65 | - | 150 | °C |

Notes: 15. No pin should go more negative than NBV - 0.3 V.

16. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pins.

17. Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.

18. Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

## SWITCHING CHARACTERISTICS ($T_A$ = 25 °C; VA+ = 5 V ±5%; VD+ = 3.0 V ±10% or 5 V ±5%; Levels: Logic 0 = 0 V, Logic 1 = VD+; $C_L$ = 50 pF.))

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Master Clock Frequency (Note 19) | XIN | | | | |
| External Clock or Internal Oscillator | | 30 | 32.768 | 100 | kHz |
| Master Clock Duty Cycle | | 40 | - | 60 | % |
| Rise Times (Note 20) | $t_{rise}$ | | | | |
| Any Digital Input Except SCLK | | - | - | 1.0 | µs |
| SCLK | | - | - | 100 | µs |
| Any Digital Output | | - | 50 | - | ns |
| Fall Times (Note 20) | $t_{fall}$ | | | | |
| Any Digital Input Except SCLK | | - | - | 1.0 | µs |
| SCLK | | - | - | 100 | µs |
| Any Digital Output | | - | 50 | - | ns |
| ***Start-up*** | | | | | |
| Oscillator Start-up Time XTAL = 32.768 kHz (Note 21) | $t_{ost}$ | - | 500 | - | ms |
| Power-on Reset Period | $t_{por}$ | - | 2006 | - | XIN cycles |
| ***Serial Port Timing*** | | | | | |
| Serial Clock Frequency | SCLK | 0 | - | 2 | MHz |
| SCLK Falling to $\overline{CS}$ Falling for continuous running SCLK (Note 22) | $t_0$ | 100 | - | - | ns |
| Serial Clock Pulse Width High | $t_1$ | 250 | - | - | ns |
| Pulse Width Low | $t_2$ | 250 | - | - | ns |
| ***SDI Write Timing*** | | | | | |
| $\overline{CS}$ Enable to Valid Latch Clock | $t_3$ | 50 | - | - | ns |
| Data Set-up Time prior to SCLK rising | $t_4$ | 50 | - | - | ns |
| Data Hold Time After SCLK Rising | $t_5$ | 100 | - | - | ns |
| SCLK Falling Prior to $\overline{CS}$ Disable | $t_6$ | 100 | - | - | ns |
| ***SDO Read Timing*** | | | | | |
| $\overline{CS}$ to Data Valid | $t_7$ | - | - | 150 | ns |
| SCLK Falling to New Data Bit | $t_8$ | - | - | 150 | ns |
| $\overline{CS}$ Rising to SDO Hi-Z | $t_9$ | - | - | 150 | ns |

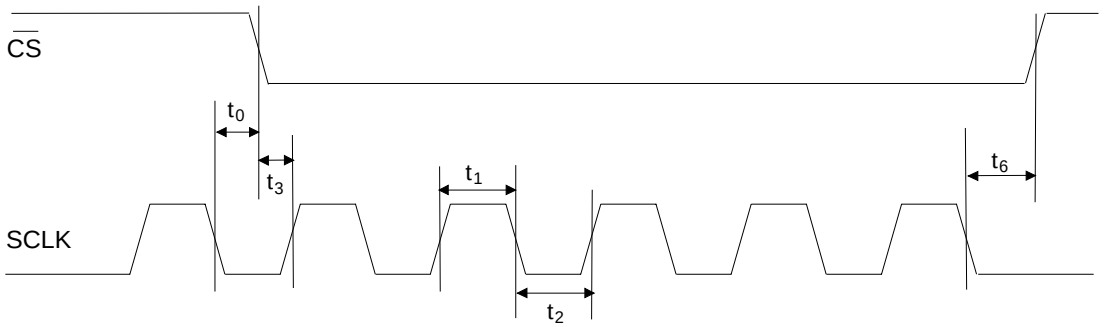
Notes: 19. Device parameters are specified with a 32.768 kHz clock; however, clocks up to 100 kHz can be used for increased throughput.

20. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

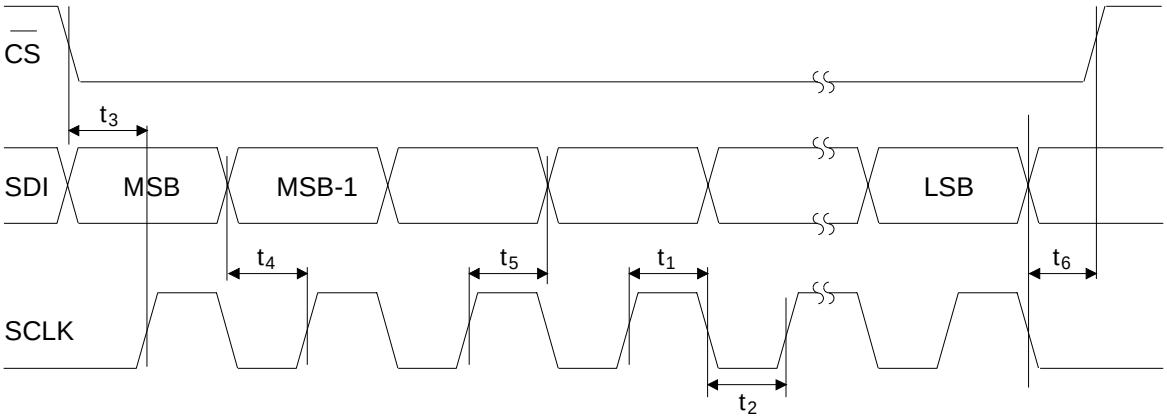
21. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

22. Applicable when SCLK is continuously running.

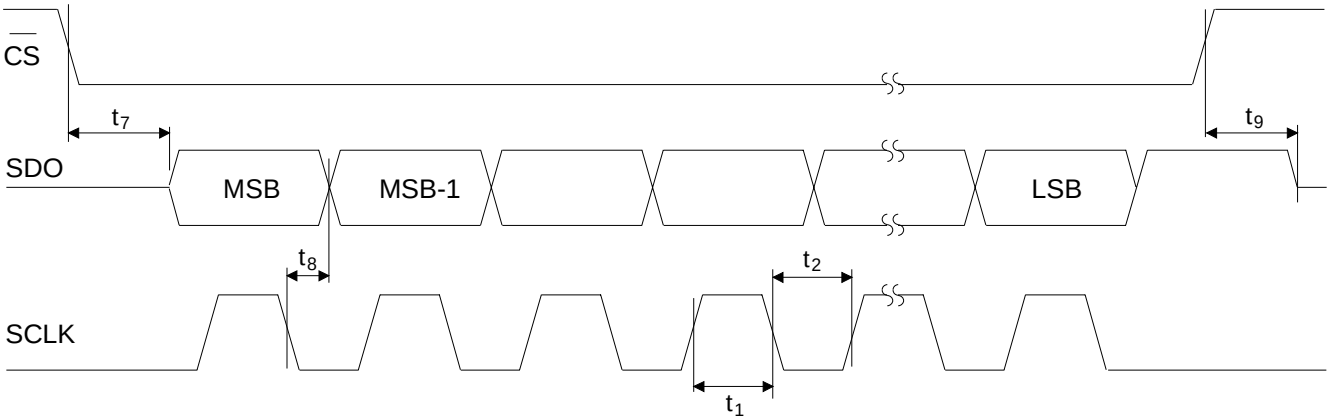
Specifications are subject to change without notice.




**Continuous Running SCLK Timing (Not to Scale)**




**SDI Write Timing (Not to Scale)**




**SDO Read Timing (Not to Scale)**

## GENERAL DESCRIPTION

The CS5522/24/28 are 24-bit converters which include a chopper-stabilized instrumentation amplifier input, and an on-chip programmable gain amplifier. They are optimized for measuring low-level unipolar or bipolar signals in process control and medical applications.

The CS5522/24/28 also include a fourth order delta-sigma modulator, a calibration microcontroller, eight digital filters used to select between eight output update rates, a 2-bit analog latch, a multiplexer, and a serial port.

The CS5522/24/28 include a CPD (Charge Pump Drive) output (shown in Figure 1) which provides a negative bias voltage to the on-chip instrumentation amplifier when used with a combination of external diodes and capacitors. This makes the converters ideal for thermocouple temperature measurements because the biasing scheme enables the CS5522/24/28 to measure negative voltages with respect to ground without the need for a negative supply.

### Theory of Operation

The CS5522/24/28 A/D converters are designed to operate from a single +5 V analog supply with several different input ranges. See the ***Analog Characteristics*** section on page 3 for details.

Figure 1 illustrates the CS5522/24/28 connected to generate their own negative bias supply using the on-chip CPD (Charge Pump Drive). This enables the CS5522/24/28 to measure ground referenced signals with magnitudes down to -100mV. Figure 2 illustrates a charge pump circuit when the converters are powered from a +3.0 V digital supply. Alternatively, the negative bias supply can be generated from a negative supply voltage or a resistive divider as illustrated in Figure 3.

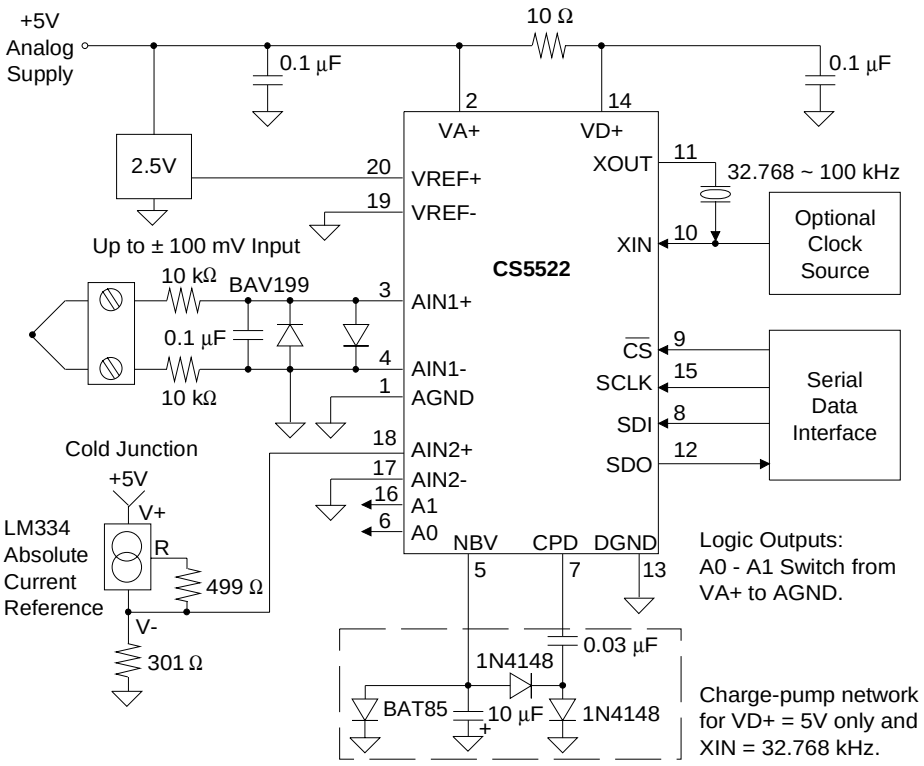



**Figure 1. CS5522/24/28 Configured to use on-chip charge pump to supply NBV.**

Figure 4 illustrates the CS5522/24/28 connected to measure ground referenced unipolar signals of a positive polarity using the 1 V, 2.5 V, and 5 V ranges on the converter. For the 25 mV, 55 mV, and 100 mV ranges the signal must have a common mode near +2.5 V (NBV = 0V).

The CS5522/24/28 are optimized for the measurement of thermocouple outputs, but are also well suited for the measurement of ratiometric bridge transducer outputs. Figure 5 illustrates the CS5522/24/28 connected to measure the output of a ratiometric differential bridge transducer while operating from a single +5 V supply.

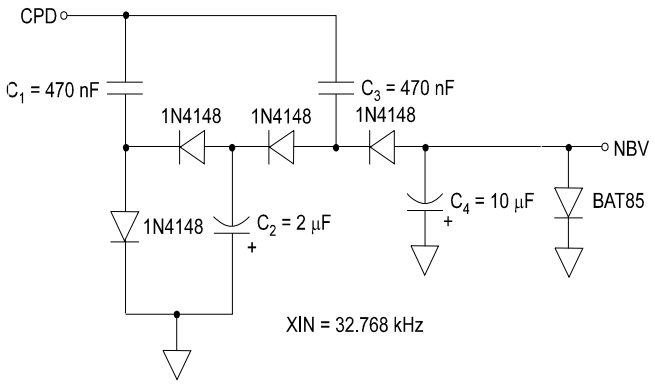



**Figure 2. Charge Pump Drive Circuit for VD+ = 3 V.**

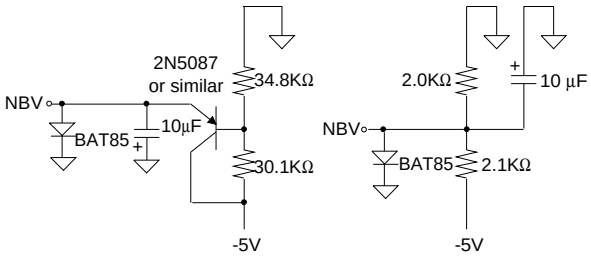



**Figure 3. Alternate NBV Circuits.**

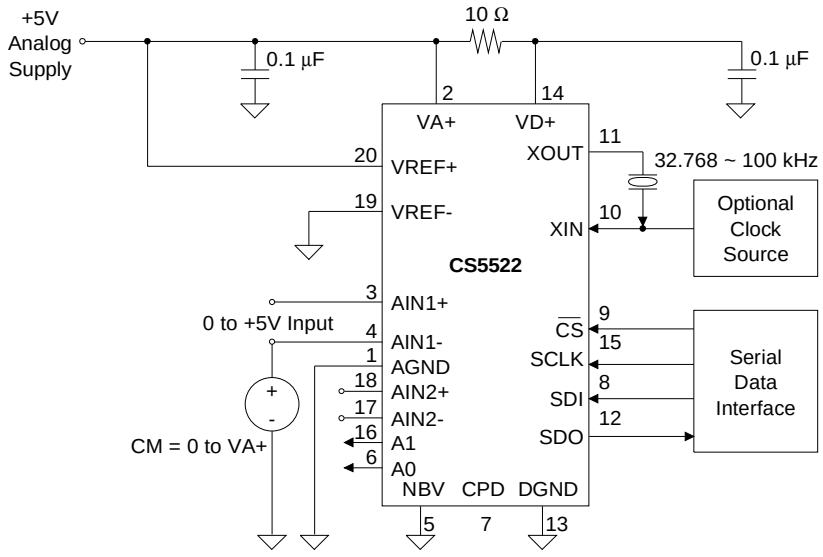



**Figure 4. CS5522/24/28 Configured for ground-referenced Unipolar Signals.**

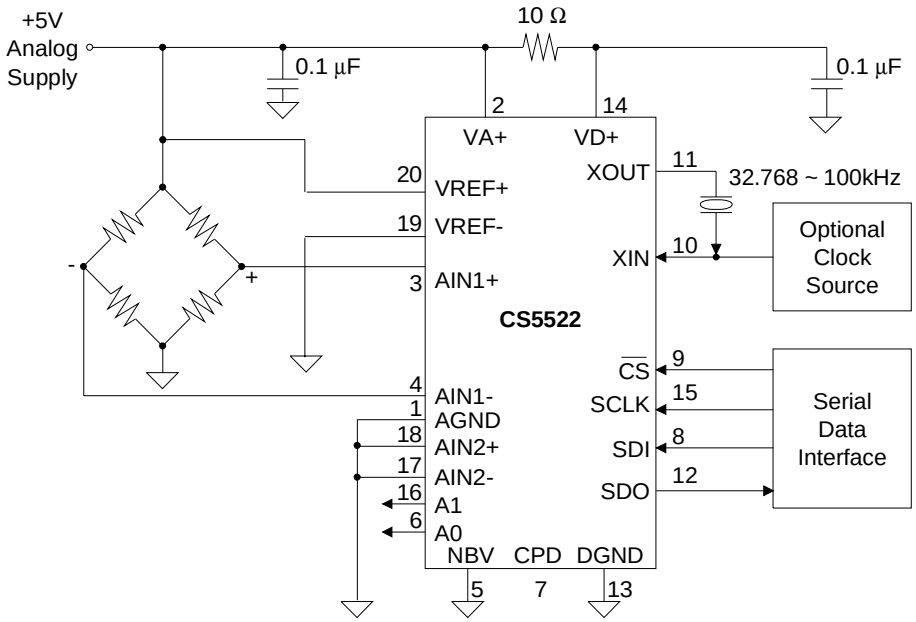



**Figure 5. CS5522/24/28 Configured for Single Supply Bridge Measurement.**

## System Initialization

When power to the CS5522/24/28 are applied, the chips are held in a reset condition until the 32.768 kHz oscillator has started and a counter-timer elapses. Due to the high Q of the 32.768 kHz crystal, the oscillator takes 400-600 ms to start. The counter-timer counts 2006 oscillator clock cycles to make sure the oscillator is fully stable. During this time-out period the serial port logic is reset and the RV (Reset Valid) bit in the configuration register is set to indicate that a valid reset occurred. After a reset, the on-chip registers are initialized to the following states and the converter is placed in the command mode where it waits for a valid command.

| | |
|---|---|
| configuration register: | 000040(H) |
| offset registers: | 000000(H) |
| gain registers: | 400000(H) |
| channel setup registers: | 000000(H) |

*Note: A system reset can be initiated at any time by writing a logic 1 to the RS (Reset System) bit in the configuration register. After a reset, the RV bit is set until the configuration register is read. The user must then write a logic 0 to the RS bit to take the part out of reset mode.*

## Serial Port Overview

The CS5522/24/28's serial port includes a microcontroller which contains a command register, a configuration register, and a gain and offset register for each input channel. The serial port also includes a programmable channel sequencer which can sequence up to 16 channels to be converted. The sequencer consists of channel-setup registers (CSRs) which contain information about the modes used when conversions are performed. To complement the sequencer a conversion data FIFO (CDF, read only) is included to store up to sixteen data conversions. All registers except the 8-bit command register are 24-bits in length. The conversion data FIFO is just an array of 24-bit conversion data registers used to store conversion words until the FIFO is read.

The serial port has two modes of operation: the command mode and the data mode. After a system initialization or reset, the serial port is initialized into command mode where it waits to receive a valid command (the first 8-bits into the serial port). Tables 1 and 2 can be used to decode all valid commands. Once a valid command is received, the byte

instructs the converter to read from or write to a register(s), perform a conversion or a calibration, or perform a NULL command. If a command other than start calibration or NULL command is received, the serial port enters data mode. In data mode, either the internal registers, the CSRs, or the CDF (read only) are read from or written to. The number of bytes transferred depends on the type of register/FIFO being accessed and the way it is accessed. Once the data is transferred, the serial port either remains in data mode or returns to the command mode. The mode which is entered depends on the status of the loop (LP), the MC (multiple conversion), and the RC (read convert) bits in the configuration register. More information concerning the LP bit is provided in the Conversion/Calibration Protocol section. Note that SDO falls to logic 0 anytime a calibration or conversion is completed.

## Serial Port Interface

The CS5522/24/28's serial interface consists of four control lines: $\overline{CS}$, SCLK, SDI, SDO.

$\overline{CS}$, Chip Select, is the control line which enables access to the serial port. If the $\overline{CS}$ pin is tied low, the port can function as a three wire interface.

SCLK, Serial Clock, is the serial bit-clock which controls the shifting of data to or from the ADC's serial port. The $\overline{CS}$ pin must be held low (logic 0) before SCLK transitions can be recognized by the port logic.

SDI, Serial Data In, is the data signal used to transfer data to the converters.

SDO, Serial Data Out, is the data signal used to transfer output data from the converters. The SDO output will be held at high impedance any time $\overline{CS}$ is at logic 1. Figure 6 illustrates the serial sequence necessary to write to, or read from the serial port's registers.

To accommodate optoisolators SCLK is designed with a Schmitt-trigger input to allow an optoisolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking or sourcing up to 5 mA to directly drive an optoisolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcing 5 mA.

## Serial Port Initialization

The serial port is initialized to the command mode whenever a power-on reset is performed inside the converter, or when the user transmits the port initialization sequence. The port initialization sequence involves clocking 15 bytes of all 1's, followed by one byte with the following bit contents '11111110'. This sequence places the chip in the command mode where it waits for a valid command to be written.

## Channel-Setup Registers

Table 3 depicts the channel-setup registers (CSRs). The CS5522 has two CSRs. The CS5524 has four CSRs and the CS5528 has eight CSRs. Each CSR contains two logical channels which are programmed by the user to contain data conversion information such as: 1) state of the output latch pins, 2) output word rate, 3) gain range, 4) polarity, and 5) the address of a physical input channel to be converted. Note that a particular physical input channel can be represented in more than one logical channel with different output rates, gain ranges, and conversion modes. Once programmed the CSRs act as a sequencer and determine the order in which conversions are performed. To program the CSRs twelve bits are needed to configure each logical channel. For example, to configure CSR #2 in the CS5522, bits 23 to 12 contain information on the third logical channel and bits 11 to 0 contain information on the fourth logical channel. Note that while reading/writing CSRs, only an even number of logical channels are accessed. The depth bits in the configuration register can only be set to: 0001, 0011, 0101, 0111, 1001, 1011, 1101, 1111 for accessing CSRs.

## *Command Register*

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| CB | CSB2 | CSB1 | CSB0 | R/$\overline{W}$ | RSB2 | RSB1 | RSB0 |

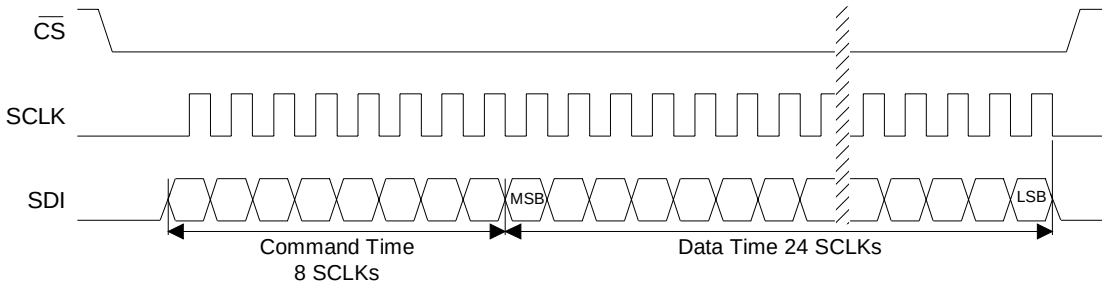
| BIT | NAME | VALUE | FUNCTION |
|---|---|---|---|
| D7 | Command Bit, CB | 0<br>1 | Must be logic 0 for these commands.<br>See Table 2. |
| D6-D4 | Channel Select Bits, CSB2-CSB0 | 000<br>.<br>.<br>111 | CSB2-CSB0 provide the address of one of the eight physical channels. These bits are used to access the calibration registers associated with respective channels.<br>Note: These bits are ignored when reading the data register. |
| D3 | Read/$\overline{Write}$, R/$\overline{W}$ | 0<br>1 | Write to selected register.<br>Read from selected register. |
| D2-D0 | Register Select Bit, RSB2-RSB0 | 000<br>001<br>010<br>011<br>100<br>101<br><br><br><br>110<br>111 | Reserved<br>Offset Register<br>Gain Register<br>Configuration Register<br>Conversion Data FIFO (read only)<br>Channel Set-up Registers<br>- register is 48-bits long for CS5522<br>- register is 96-bits long for CS5524<br>- register is 192-bits long for CS5528<br>Reserved<br>Reserved |

**Table 1. Command-Set with MSB=0**

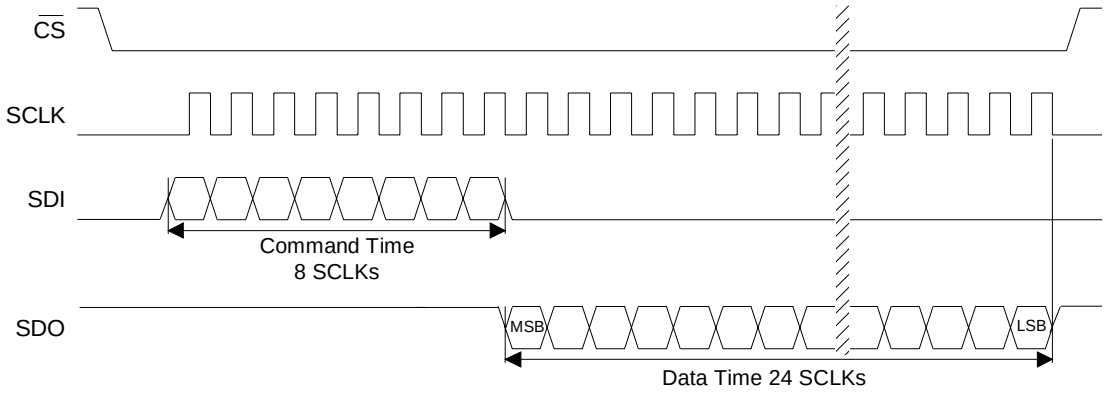
| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| CB | CPB3 | CPB2 | CPB1 | CPB0 | CC2 | CC1 | CC0 |

| BIT | NAME | VALUE | FUNCTION |
|---|---|---|---|
| D7 | Command Bit, CB | 0<br>1 | See Table 1.<br>Must be logic 1 for these commands. |
| D6-D3 | Channel Pointer Bits, CPB3-CPB0 | 0000<br>.<br>.<br>.<br>1111 | These bits are used as pointers to the logical channels.<br>Note: The MC bit, must be logic 0 for these bits to take effect. When MC = 1, these bits are ignored. The LP, MC, and RC bits in the configuration register are ignored during calibration. |
| D2-D0 | Conversion/Calibration Bits, CC2-CC0 | 000<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | Normal Conversion<br>Self-Offset Calibration<br>Self-Gain Calibration<br>Reserved<br>Reserved<br>System-Offset Calibration<br>System-Gain Calibration<br>Reserved |

**Table 2. Command-Set with MSB=1**




**Write Cycle**




**Read Cycle**

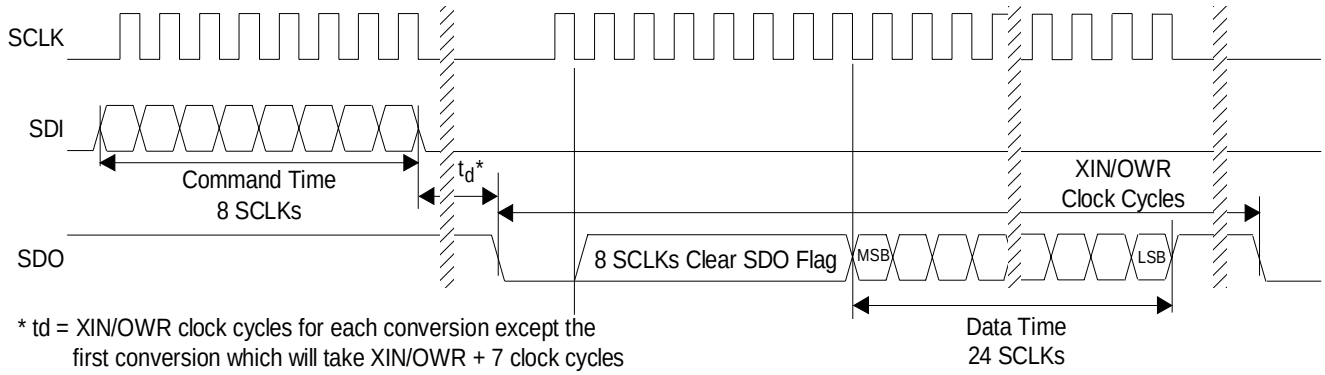
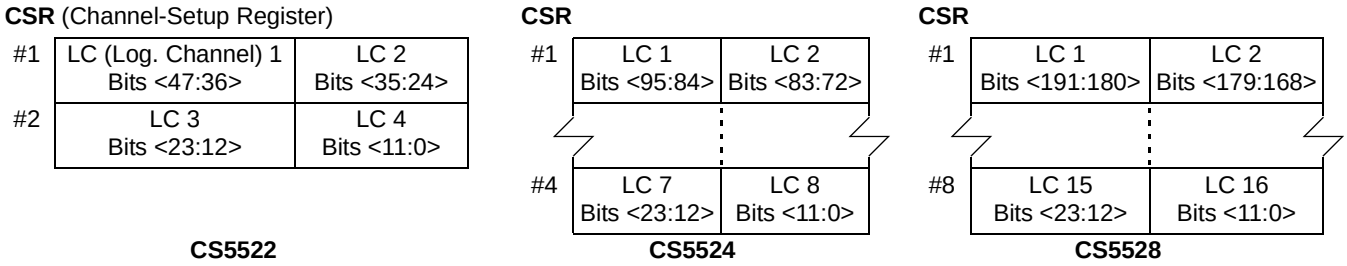



**Figure 6. Command and Data Word Timing.**

## *Channel-Setup Registers*




| D23(MSB) | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | A0 | CS2 | CS1 | CS0 | WR2 | WR1 | WR0 | G2 | G1 | G0 | U/$\overline{B}$ |

| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | A0 | CS2 | CS1 | CS0 | WR2 | WR1 | WR0 | G2 | G1 | G0 | U/$\overline{B}$ |

| BIT | NAME | VALUE | | FUNCTION |
|---|---|---|---|---|
| D23-D22/ D11-D10 | Latch Outputs, A1-A0 | 00 | *R | Latch Output Pins A1-A0 mimic D23/D11-D22/D10 register bits. |
| D21-D19/ D9-D7 | Channel Select, CS2-CS0 | 000<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | R | Select physical channel 1.<br>Select physical channel 2.<br>Select physical channel 3.<br>Select physical channel 4.<br>Select physical channel 5.<br>Select physical channel 6.<br>Select physical channel 7.<br>Select physical channel 8. |
| D18-D16/ D6-D4 | Word Rate, WR2-WR0 | 000<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | R | 15.0 Hz (2180 XIN cycles).<br>30.0 Hz (1092 XIN cycles).<br>61.6 Hz (532 XIN cycles).<br>84.5 Hz (388 XIN cycles).<br>101.1 Hz (324 XIN cycles).<br>1.88 Hz (17444 XIN cycles).<br>3.76 Hz (8724 XIN cycles).<br>7.51 Hz (4364 XIN cycles). |
| D15-D13/ D3-D1 | Gain Bits, G2-G0 | 000<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | R | 100 mV (assumes VREF Differential = 2.5 V)<br>55 mV<br>25 mV<br>1.0 V<br>5.0 V<br>2.5 V<br>Not used.<br>Not used. |
| D12/D0 | Unipolar/Bipolar, U/$\overline{B}$ | 0<br>1 | R | Bipolar measurement mode.<br>Unipolar measurement mode. |

* R indicates the bit value after the part is reset

**Table 3. Channel-Setup Registers**

### *Configuration Register*

| D23(MSB) | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| NU | NU | CFS1 | CFS0 | NU | MC | LP | RC | DP3 | DP2 | DP1 | DP0 |

| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PSS | PD | PS/$\overline{R}$ | LPM | RS | RV | OD | OF | NU | NU | NU | NU |

| BIT | NAME | VALUE | | FUNCTION |
|---|---|---|---|---|
| D23-D22 | Not Used, NU | 00 | R* | Must always be logic 0. |
| D21-D20 | Chop Frequency Select, CFS1-CFS0 | 00<br>01<br>10<br>11 | R | 256 Hz Amplifier chop frequency.<br>4,096 Hz Amplifier chop frequency.<br>16,384 Hz Amplifier chop frequency.<br>1,024 Hz Amplifier chop frequency. |
| D19 | Not Used, NU | 0 | R | Must always be logic 0. |
| D18 | Multiple Conversion, MC | 0<br>1 | R | Perform single channel conversions. MC bit is ignored during calibrations.<br>Perform multiple conversions on logical channels in the channel-setup register by issuing only one command with MSB = 1. |
| D17 | Loop, LP | 0<br>1 | R | Don't loop. LP bit is ignored during calibrations.<br>The conversions on the single channel (MC = 0) or multiple channels (MC = 1) are continuously performed. |
| D16 | Read Convert, RC | 0<br>1 | R | Don't wait for user to finish reading data before starting new conversions.<br>The RC bit is used in conjunction with the LP bit when the LP bit is set to logic 1. If LP = 0, the RC bit is ignored. If LP = 1, the ADC waits for user to read data conversion(s) before converting again. The RC bit is ignored during calibrations. Refer to Calibration Protocol for details. |
| D15-D12 | Depth Pointer, DP3-DP0 | 0000<br>.<br>.<br>1111 | R | When writing or reading the CSRs, these bits (DP3-DP0) determine the number of CSR's to be accessed. They are also used to determine how many logical channels are converted when MC=1 and a command byte with its MSB = 1 is issued. Note that the CS5522 has two CSRS, the CS5524 has four CSRs, and the CS5528 has 8 CSRs. |
| D11 | Power Save Select, PSS | 0<br>1 | R | Standby Mode (Oscillator active, allows quick power-up).<br>Sleep Mode (Oscillator inactive). |
| D10 | Pump Disable, PD | 0<br>1 | R | Charge Pump Enabled.<br>For PD = 1, the CPD pin goes to a Hi-Z output state. |
| D9 | Power Save/$\overline{Run}$, PS/$\overline{R}$ | 0<br>1 | R | Run.<br>Power Save. |
| D8 | Low Power Mode, LPM | 0<br>1 | R | Normal Mode.<br>Reduced Power Mode. |
| D7 | Reset System, RS | 0<br>1 | R | Normal Operation.<br>Activate a Reset cycle. To return to Normal Operation write bit to zero. |
| D6 | Reset Valid, RV | 0<br>1 | <br>R | No reset has occurred or bit has been cleared (read only).<br>Bit is set after a Valid Reset has occurred. (Cleared when read.) |
| D5 | Oscillation Detect, OD | 0<br>1 | R | Bit is clear when an oscillation condition has not occurred (read only).<br>Bit is set when an oscillatory condition is detected in the modulator. |
| D4 | Overrange Flag, OF | 0<br>1 | R | Bit is clear when an overrange condition has not occurred (read only).<br>Bit is set when input signal is more positive than the positive full scale, more negative than zero (unipolar mode), or when the input is more negative than the negative full scale (bipolar mode). |
| D3-D0 | Not Used, NU | 0000 | R | Must always be logic 0. |

* R indicates the bit value after the part is reset

**Table 4. Configuration Register**

## Conversion Protocol

To acquire single or multiple conversion(s) a command byte is issued with its MSB=1 and CC2-CC0 = '000'. The type of conversion(s) performed and the way to access the resulting data is determined by the MC (multiple conversion), the LP (loop), and the RC (read convert) bits in the configuration register. MC's, LP's, and RC's functional descriptions follow. The other bits in the configuration register are detailed in Table 4.

MC = 0 LP = 0 RC = X

Based on the information provided in the channel-setup registers (CSRs), a single conversion is performed on the physical channel referenced by the logical channel. The command byte contains the pointer address of the logical channel to be used during the conversion embedded in it. The serial port enters data mode as soon as the 8-bit command byte to start a conversion is issued. The port remains in data mode during conversion. Upon the completion of the conversion, SDO falls to logic 0. Thirty-two SCLKs are needed to acquire the conversion. The first 8 SCLKs are used to clear the SDO flag. The last 24 are needed to read the conversion result. After reading the data, the serial port returns to the command mode, where it waits for a new command to be issued.

MC = 0 LP = 1 RC = 0

Based on information contained in the CSRs, a single conversion is repeatedly performed on the physical channel referenced by the logical channel. The command byte contains the pointer address of the logical channel to be used during conversion. Once a conversion is complete, SDO falls to indicate that a conversion is ready. Thirty-two SCLKs are needed to acquire the conversion (which must be acquired within a certain window, refer to Figure 6). The first 8 SCLKs are used to clear the SDO flag. The next 24 are needed to read the conversion result. If '00000000' is provided to SDI during the first 8 SCLKs when the SDO flag is cleared, the converter remains in this conversion mode and continues to convert the selected channel. While in this mode, the user may choose to acquire only the conversions required for his application as SDO rises and falls to indicate the availability of a new conversion. To exit this conversion mode the user must provide '11111111' to the SDI pin during the first 8 SCLKs. If the user decides to exit, 24 SCLKs are required to clock out the last conversion before the converter will return to the command mode.

MC = 0 LP = 1 RC = 1

Based on information provided in the CSRs, a single conversion is performed repeatedly on the physical channel referenced by the logical channel. The command byte contains the pointer address of the logical channel to be used during the conversion embedded in it. After a conversion cycle is complete, SDO falls and the serial port is placed in the data mode where it will remain until the conversion data is read. If the user doesn't read the conversion word the converter stops performing new conversions and SDO will remain low until the conversion data is acquired. To acquire the conversion data thirty-two SCLKs are needed. The first 8 SCLKs are used to clear the SDO flag. The next 24 are needed to read the conversion result. If '00000000' is provided to SDI during the first 8 SCLKs to clear the SDO flag, a new conversion cycle will be started after the conversion data is read. To exit this conversion mode and return to the command mode, the user must provide '11111111' to the SDI during the first 8 SCLKs. A final 24 SCLKs are required to clock out the last conversion data.

MC = 1 LP = 0 RC = X

Based on information provided in the CSRs, multiple conversions are performed once on the physical channels referenced by the logical channels of the CSRs. The first two conversions are based on the information in the channel-setup register (CSR) #1 (logical channels one and two); the third and fourth conversions are based on information in the CSR

#2 (logical channels three and four); and so on up to 16 conversions when the CS5528 is used. The depth (DP3-DP0) information bits in the configuration register determine how many conversions are performed and hence must be initialized before this conversion mode is entered. Upon completion of the conversions, SDO falls to indicate that the conversion data set is ready to be read. To read the conversions from the conversion data FIFO, the user must first issue 8 SCLKs to clear the SDO flag. To read the conversions, the user must then supply 24x(N) SCLKs. N is defined here as the number of logical channels being converted which is the decimal equivalent of depth + 1. For example, if DP3-DP0 = '0010', N = (2+1) = 3. To return to the command mode, the user must read all the conversion data from the FIFO because the serial port remains in data mode during the conversions and during the read of the data. Whether '00000000' or '11111111' is provided to the SDI during the 8 SCLKs needed to clear the SDO flag, the serial port returns to the command mode after the conversion data FIFO is read.

MC = 1 LP = 1 RC = 0

Based on information provided in the CSRs, multiple conversions are repeatedly performed on the physical channels referenced by the logical channels of the CSRs. This conversion mode is similar to the conversion mode when MC=1, LP=0, and RC=X. Once a conversion data set is converted the conversions are stored in the conversion data FIFO. The only exception is that the converter then returns to the top of the CSRs (i.e. to logical channel one of CSR #1) and repeats. As before, SDO falls to indicate when a data set is compete. Once SDO falls, the user has three options: 1) exit after reading the conversion data FIFO; this is accomplished by providing SDI '11111111' during the first 8 SCLKS and then giving 24xN more SCLKs to acquire the conversion data; 2) provide no SCLKs and remain in this mode without reading the data; in this case, SDO rises and falls once a new set of conversions is complete to indicate that a new set of data is ready to acquire; or 3) read the conversion data FIFO and remain in this mode; this is accomplished by providing SDI with '00000000' during the first 8 SCLKs and then giving 24xN more SCLKs to read the conversion data; the user must finish reading the FIFO before the first logical channel of CSR #1 finishes a new conversion.

MC = 1 LP = 1 RC = 1

Based on information provided in the CSRs, multiple conversions are performed repeatedly on the logical channel of the CSR. This mode is similar to the conversion mode when MC=1, LP=1, and RC=0. The only exception is that the converter stops and waits for the conversion data FIFO to be emptied before new conversions are started. As before SDO falls when a data set is complete. Once SDO falls, the user has two options: 1) exit after emptying the FIFO; this is accomplished by providing SDI '11111111' during the first 8 SCLKs and then giving 24xN more SCLKs to read the conversion data; or 2) empty the conversion data FIFO and remain in this mode; this is accomplished by providing SDI with '00000000' during the first 8 SCLKs and then giving 24xN more SCLKs to read the conversion data. After the FIFO is emptied, the converter returns to the top of the CSRs (i.e. to logical channel one of CSR#1) and repeats.

## Calibration Protocol

To perform a calibration the user must send a command byte with its MSB=1, its pointer bits (CPB3-CPB0) set to address the desired logical channel to be calibrated, and the appropriate calibration bits (CC2-CC0) set to choose the type of calibration to be performed. Proper calibration assumes that the CSRs have been previously initialized because the information concerning the physical channel, its filter rate, gain range, and polarity, comes from the channel-setup register being addressed by the pointer bits in the command byte.

Once the CSRs are initialized all future calibrations can be performed with one command byte. Once a calibration cycle is complete SDO falls and the results are stored in either the gain or offset register for the physical channel being calibrated. Note that if additional calibrations are performed on the same physical channel referenced by a different logical channel with different filter rates, gain ranges, or conversion modes, the last calibration results will replace the effects from the previous calibration as only one offset and gain register is available per physical channel. One final note is that only one calibration is performed with each command byte. To calibrate all the channels additional calibration commands are necessary.

## Use of Pointers in Command Byte

Any time a calibration command is issued (CB=1 and proper CC2-CC0 bits set) or any time a normal conversion command is issued (CB=1, CC2=CC1=CC0=0, MC=0), the bits D6-D3 (or CPB3 - CPB0) in the command byte are used as pointers to address one of the logical channels in the channel-setup registers (CSRs). Table 5 details the pointer the bits address. Note that for the CS5524, D6-D3 can only be 0000 - 0111 (8 logical channels). For the CS5522, D6-D3 (or CPB3 - CPB0) can only be 0000 - 0011 (4 logical channels). Five example situations that a user might encounter when acquiring a conversion or calibrating the converter follow. These examples assume that the user is using a CS5528 (16 logical channels) and that its CSRs are programmed with the following physical channel order: 6, 1, 6, 2, 6, 3, 6, 4, 6, 5, 6, 2, 6, 7, 6, 8.

| D6 - D3 (CPB3-CPB0) | CSR Address | Logical Channel |
|---|---|---|
| 0000 | CSR #1 | 1st |
| 0001 | CSR #1 | 2nd |
| 0010 | CSR #2 | 3rd |
| 0011 | CSR #2 | 4th |
| 0100 | CSR #3 | 5th |
| 0101 | CSR #3 | 6th |
| 0110 | CSR#4 | 7th |
| 0111 | CSR #4 | 8th |
| 1000 | CSR #5 | 9th |
| 1001 | CSR #5 | 10th |
| 1010 | CSR #6 | 11th |
| 1011 | CSR #6 | 12th |
| 1100 | CSR #7 | 13th |
| 1101 | CSR #7 | 14th |
| 1110 | CSR #8 | 15th |
| 1111 | CSR #8 | 16th |

**Table 5. Command Byte Pointer Table**

Example 1: The configuration register has the following bits as shown: DP3-DP0 = '1001', MC = 1, LP = 1, RC = 0. The command byte issued is '1XXXX000'. These settings instruct the converter to repeatedly perform multiple single conversions on ten logical channels. The order in which the channels are converted is: 6, 1, 6, 2, 6, 3, 6, 4, 6, 5. SDO falls after physical channel 5 is converted. To acquire the 10 conversions 8 SCLKs with SDI = 0 are required to clear the SD0 flag. Then 240 more SCLKs are required to read the conversion data from the FIFO. The order in which the data is provided is the same as the order in which the channels are converted. The first 3 bytes of data correspond to the first logical channel which in this example is physical channel 6; the next 3 bytes of data correspond to the second logical channel which in this example is physical channel 1; and, the last 3 bytes of data corresponds to 10th logical channel which here is physical channel 5. Since the logical channels are converted in the background, while the data is being read, the user must finish reading the conversion data FIFO before it is updated with new conversions. To exit this conversion mode the user

must provide '11111111' to SDI during the first 8 SCLKs. If a byte of 1's is provided, the serial port returns to the command mode only after the conversion data FIFO is emptied (in this case 10 conversions are acquired). Note that in this example physical channel 6 is converted five times. Each conversion could be with the same or different filter rates depending on the setting of logical channels 1, 3, 5, 7 and 9. Note that there is only one offset and one gain register per physical channel. Therefore, any physical channel can only be calibrated for the gain range selected during calibration. Specifying a different gain range in the logical channel setting than the range that was calibrated will result in a gain error.

Example 2: The configuration register has the following bits as shown: DP3-DP0 = '0101', MC = 1, LP = 0, RC = X. The command issued is '1XXXX000'. These settings instruct the converter to perform a single conversion on six logical channels once. The order in which the channels are converted is 6, 1, 6, 2, 6, and 3. SDO falls after physical channel 3 is converted. To acquire the 6 conversions 8 SCLKs are required to clear the SD0 flag. Then 144 additional SCLKs are required to get the conversion data. Again, the order in which the data is provided is the same as the order in which the channels are converted. After the last 3 bytes of the conversion data corresponding to physical channel 3 is read, the serial port automatically returns to the command mode where it will remain until the next valid command byte is received.

Example 3: The configuration register has the following bits as shown: DP3-DP0 = 'XXXX', MC = 0, LP = 1, RC = 1. The command byte issued is '10011000'. These settings instruct the converter to repeatedly convert the fourth logical channel as CPB3-CPB0 = '0011' (which happens to be physical channel 2 in this example). SDO falls after physical channel 2 is converted. To acquire the conversion 32 SCLKs are required. The first 8 SCLKs are needed to clear the SD0 flag. As in Example 1, if '00000000' is provided to the SDI pin during the first 8 SCLKs, the conversion is performed again on physical channel 2. The converter will remain in data mode until '11111111' is provided during the first 8 SCLKs following the fall of SD0. After '11111111' is provided, 24 additional SCLKs are required to transfer the last 3 bytes of conversion data before the serial port will return to the command mode.

Example 4: The configuration register has the following bits as shown: DP3-DP0 = 'XXXX', MC = 0, LP = 0, RC = X. The command issued is '11110000'. These settings instruct the converter to convert the 15th logical channel once, as CPB3 - CPB0 = '1110' (which happens to be physical channel 6 in this example). SDO falls after physical channel 6 is converted. To read the conversion, 32 SCLKs are then required. Once acquired, the serial port returns to the command mode.

Example 5: The configuration register has the following bits as shown: DP3-DP0 = 'XXXX', MC = X, LP = X, RC = X. The command issued is '10101101'. These settings instruct the converter to perform a system offset calibration of the 6th logical channel (which is physical channel 3 in this example). During calibration the serial port remains in the command mode. Once the calibration is completed, SDO falls. To perform additional calibrations, more commands have to be issued.

***Notes:*** *1) The configuration register must be written before channel-setup registers (CSRs) because the depth information contained in the configuration register defines how many of the CSRs to use. 2) The CSRs need to be written irrespective of single conversion or multiple single conversion mode. 3) When single conversions (MC = 0) are desired, the channel address is embedded in the command byte. In the multiple single conversion mode (MC = 1), channels are selected in a preprogrammed order based on information contained in the CSRs and the depth bits (DP3-DP0) of the configuration register. 4) Once the CSRs are programmed, multiple conversions on up to 16 logical channels can be performed by issuing only one command byte. 5) The single conversion mode also requires only one command, but whenever another*

*or a different single conversion is wanted, this command or a modified version of it has to be issued again. 6) The NULL command is used to keep the serial port in command mode, once it is in command mode.*

## Analog Input

Figure 7 illustrates a block diagram of the analog input signal path inside the CS5522/24/28. The front end consists of a multiplexer, a chopper-stabilized instrumentation amplifier with 20X gain and a programmable gain section. The instrumentation amplifier is powered from VA+ and from the NBV (Negative Bias Voltage) pin allowing the CS5522/24 to be operated in either of two analog input configurations. The NBV pin can be biased to a negative voltage between -1.8 V and -2.5 V, or tied to AGND (for the CS5528, NBV has to be between -1.8V and -2.5V for the lower input ranges when the amplifier is engaged). The choice of the operating mode for the NBV voltage depends upon the input signal and its common mode voltage.

For the 25 mV, 55 mV, and 100 mV input ranges, the input signals to AIN+ and AIN- are amplified by the 20X instrumentation amplifier. For ground referenced signals with magnitudes less then 100 mV, the NBV pin should be biased with -1.8 V to -2.5 V. If NBV is tied between -1.8 V and -2.5 V, the (Common Mode + Signal) input on AIN+ and AIN- must stay between -0.150 V and 0.950 V to ensure proper operation. Alternatively, NBV can be tied to AGND (except for the CS5528 where all inputs are AGND referenced) where the input (Common Mode + Signal) on AIN+ and AIN- must stay between 1.85 V and 2.65 V to ensure that the amplifier operates properly.

For the 1 V, 2.5 V, and 5 V input ranges, the instrumentation amplifier is bypassed and the input signals are connected to the Programmable Gain block. Whether NBV tied between -1.8 V and -2.5 V or tied to AGND, the (Common Mode + Signal) input on AIN+ and AIN- must stay between NBV and VA+.

The CS5522/24/28 can accommodate full scale ranges other than 25 mV, 55 mV, 100 mV, 1 V, 2.5 V and 5 V by performing a system calibration with-

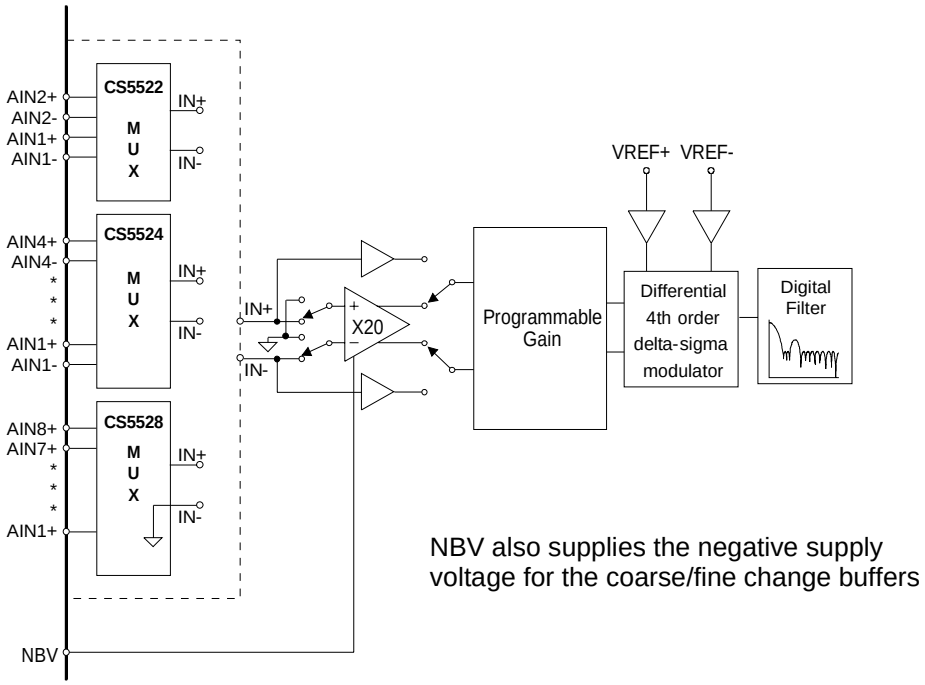



**Figure 7. Multiplexer Configuration**

in the limits specified. See the **Calibration** section for more details. Another way to change the full scale range is to increase or to decrease the voltage reference to other than 2.5 V. See the **Voltage Reference** section for more details.

Three factors set the operating limits for the input span. They include: instrumentation amplifier saturation, modulator 1's density, and a lower reference voltage. When the 25 mV, 55 mV or 100 mV range is selected, the input signal (including the common mode voltage and the amplifier offset voltage) must not cause the 20X amplifier to saturate in either its input stage or output stage. To prevent saturation the absolute voltages on AIN+ and AIN- must stay within the limits specified (refer to the '***Analog Input***' table on page 3). Additionally, the differential output voltage of the amplifier must not exceed 2.8 V. The equation

$$ABS(VIN + VOS) \times 20 = 2.8\ V$$

defines the differential output limit, where

$$VIN = (AIN+) - (AIN-)$$

is the differential input voltage and VOS is the absolute maximum offset voltage for the instrumentation amplifier (VOS will not exceed 40 mV). If the differential output voltage from the amplifier exceeds 2.8 V, the amplifier may saturate, which will cause a measurement error.

The input voltage into the modulator must not cause the modulator to exceed a low of 20 percent or a high of 80 percent 1's density. The nominal full scale input span of the modulator (from 30 percent to 70 percent 1's density) is determined by the VREF voltage divided by the Gain Factor. See Table 6 to determine if the CS5522/24/28 are being used properly. For example, in the 55 mV range, to determine the nominal input voltage to the modulator, divide VREF (2.5 V) by the Gain Factor (2.2727).

When a smaller voltage reference is used, the resulting code widths are smaller causing the converter output codes to exhibit more changing codes for a fixed amount of noise. Table 6 is based upon a VREF = 2.5 V. For other values of VREF, the values in Table 6 must be scaled accordingly.

Figure's 8 and 9 illustrate the input models for the AIN and VREF pins. The dynamic input current for each of the pins can be determined from the models shown and is dependent upon the setting of the CFS1 and CFS0 (Chop Frequency Select) bits. The effective input impedance for the AIN+ and AIN- pins remains constant for the three low level measurement ranges (25 mV, 55 mV, and 100 mV). The input current is lowest with the CFS bits cleared to logic 0s.

***Note:*** *Residual noise appears in the converter's baseband for output word rates greater than 61.6 Hz if the CFS bits are logic 0. To eliminate the residual noise for word rates of 61.6 Hz and lower, 256 Hz chopping is recommended, and for 84.5 Hz and 101.1 Hz filters, 4096 Hz chopping is recommended. Note that C=48pF is for input current modeling only. For physical input capacitance see 'Input Capacitance' specification under 'Analog Characteristics' on page 3.*

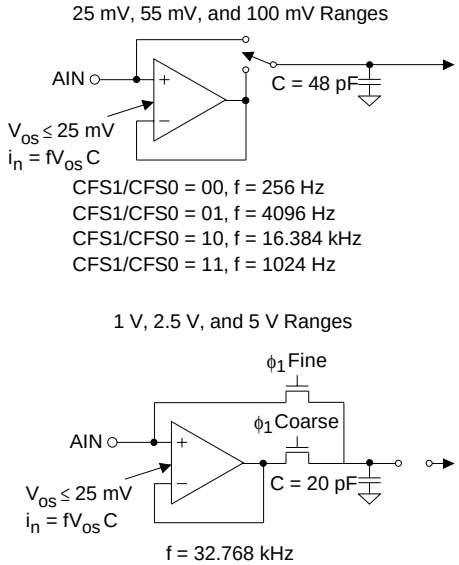



**Figure 8. Input models for AIN+ and AIN- pins for each range.**

| Input Range(1) | Max. Differential Output 20X Amplifier | VREF | Gain Factor | Δ-Σ Nominal(1) Differential Input | Δ-Σ(1) Max. Input |
|---|---|---|---|---|---|
| ± 25 mV | 2.8 V (2) | 2.5V | 5 | ± 0.5 V | ± 0.75 V |
| ± 55 mV | 2.8 V (2) | 2.5V | 2.272727... | ± 1.1 V | ± 1.65 V |
| ± 100 mV | 2.8 V (2) | 2.5V | 1.25 | ± 2.0 V | ± 3.0 V |
| ± 1.0 V | - | 2.5V | 2.5 | ± 1.0 V | ± 1.5 V |
| ± 2.5 V | - | 2.5V | 1.0 | ± 2.5 V | ± 5.0 V |
| ± 5.0 V | - | 2.5V | 0.5 | ± 5.0 V | 0V, VA+ |

**Table 6. Relationship between Full Scale Input, Gain Factors, and Internal Analog Signal Limitations**

Note: 1. The converter's actual input range, the delta-sigma's nominal full scale input, and the delta-sigma's maximum full scale input all scale directly with the value of the voltage reference. The values in the table assume a 2.5 V VREF voltage.
2. The 2.8 V limit at the output of the 20X amplifier is the differential output voltage.

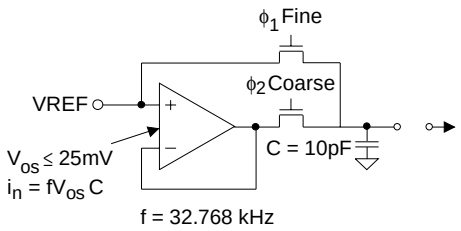



**Figure 9. Input model for VREF+ and VREF- pins.**

## Charge Pump Drive

The CPD (Charge Pump Drive) pin of the converter can be used with external components (shown in Figure 1) to develop an appropriate negative bias voltage for the NBV pin. When CPD is used to generate the NBV, the NBV voltage is regulated with an internal regulator loop referenced to VA+. Therefore, any change on VA+ results in a proportional change on NBV. With VA+ = 5 V, NBV's regulation is set proportional to VA+ at approximately -2.1 V.

Figure 3 illustrates a means of supplying NBV voltage from a -5 V supply. For ground based signals with the instrumentation amplifier engaged (when in the 25mV, 55mV, or 100mV ranges), the voltage on the NBV pin should at no time be less negative than -1.8 V or more negative than -2.5 V. To prevent excessive voltage stress to the chip when the instrumentation amplifier isn't engaged (when in the 1V, 2.5V, or 5V ranges) the NBV voltage should not be more negative than -2.5 V.

The components in Figure 1 are the preferred components for the CPD filter. However, smaller capacitors can be used with acceptable results. The 10 µF ensures very low ripple on NBV. Intrinsic safety requirements prohibit the use of electrolytic capacitors. In this case, four 0.47 µF ceramic capacitors in parallel can be used.

***Note:*** *The charge pump is designed to nominally provide 400µA of current for the instrumentation amplifier when a 0.03µF pumping capacitor is used (XIN = 32.768 kHz). When a larger pumping capacitor is used, the charge pump can source more current to power external loads. Refer to Applications Note 146 for more details on using the charge pump with external loads.*

## Voltage Reference

The CS5522/24/28 are specified for operation with a 2.5 V reference voltage between the VREF+ and VREF- pins of the device. For a single-ended reference voltage, such as the LT1019-2.5, the reference voltage is input into the VREF+ pin of the converter and the VREF- pin is grounded.

The differential voltage between the VREF+ and VREF- can be any voltage from 1.0 V up to VA+, however, the VREF+ cannot go above VA+ and the VREF- pin can not go below NBV.

## Calibration

The CS5522/24/28 offer five different calibration functions including self calibration and system calibration. However, after the CS5522/24/28 are reset, the converter is functional and can perform measurements without being calibrated. In this case, the converter will utilize the initialized values of the on-chip registers (Gain = 1.0, Offset = 0.0) to calculate output words for the ±100 mV range. Any initial offset and gain errors in the internal circuitry of the chip will remain.

The gain and offset registers, which are used for both self and system calibration, are used to set the zero and full-scale points of the converter's transfer function. One LSB in the offset register is $2^{-24}$ proportion of the input span (bipolar span is 2 times the unipolar span). The MSB in the offset register determines if the offset to be trimmed is positive or negative (0 positive, 1 negative). The converter can typically trim ±50 percent of the input span. The gain register spans from 0 to $(4 - 2^{-22})$. The decimal equivalent meaning of the gain register is

$$D = b_{MSB}2^{1} + (b_0 2^{0} + b_1 2^{-1} + \ldots + b_N 2^{-N}) = b_{MSB}2^{1} + \sum_{i=0}^{N} b_i 2^{-i}$$

where the binary numbers have a value of either zero or one ($b_0$ corresponds to bit MSB-1, N=22). Refer to Table 7 for details.

The offset and gain calibration steps each take one conversion cycle to complete. At the end of the calibration step, SDO falls and the calibration control bits will be set back to logic 0.

## Self Calibration

The CS5522/24/28 offer both self offset and self gain calibrations. For the self-calibration of offset in the 25mV, 55mV, and 100mv ranges, the converters internally tie the inputs of the instrumentation amplifier together and route them to the AIN- pin as shown in Figure 10 (in the CS5528 they are routed to AGND). For proper self-calibration of offset to occur in the 25 mV, 55 mV, and 100 mV ranges, the AIN- pin must be at the proper common-mode-voltage as specified in 'Common Mode +Signal AIN+/-' specification under 'Analog Input' section on page 3 (if AIN- = 0V, NBV must be between -1.8 V to -2.5 V). For self-calibration of offset in the 1.0 V, 2.5 V, and 5 V ranges, the inputs of the modulator are connected together and then routed to the VREF- pin as shown in Figure 11.

For self-calibration of gain, the differential inputs of the modulator are connected to VREF+ and VREF- as shown in Figure 12. For any input range

### *Offset Register*

| | MSB | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ***Register*** | Sign | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-19}$ | $2^{-20}$ | $2^{-21}$ | $2^{-22}$ | $2^{-23}$ | $2^{-24}$ |
| Reset (R) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

One LSB represents $2^{-24}$ proportion of the input span (bipolar span is 2 times unipolar span)
Offset and data word bits align by MSB (bit MSB-4 of offset register changes bit MSB-4 of data)

### *Gain Register*

| | MSB | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ***Register*** | $2^{1}$ | $2^{0}$ | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-17}$ | $2^{-18}$ | $2^{-19}$ | $2^{-20}$ | $2^{-21}$ | $2^{-22}$ |
| Reset (R) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The gain register span is from 0 to $(4\text{-}2^{-22})$. After Reset the (MSB-1) bit is 1, all other bits are 0.

**Table 7. Offset and Gain Registers**

other than the 2.5 V range, the converter's gain error can not be completely calibrated out. This is due to the lack of an accurate full scale voltage internal to the chips. The 2.5 V range is an exception because the external reference voltage is 2.5 V nominal and is used as the full scale voltage. In addition, when self-calibration of gain is performed in the 25 mV, 55 mV, and 100 mV input ranges, the instrumentation amplifier's gain is not calibrated. These two factors can leave the converters with a gain error of up to ±20% after self-calibration of gain. Therefore, a system gain calibration is required to get better accuracy, except for the 2.5 V range.

## System Calibration

For the system calibration functions, the user must supply the converters calibration signals which represent ground and full scale. When a system offset calibration is performed, a ground reference signal must be applied to the converters. See Figures 13 and 14.

As shown in Figures 15 and 16, the user must input a signal representing the positive full scale point to perform a system gain calibration. In either case, the calibration signals must be within the specified calibration limits for each specific calibration step (refer to the System Calibration Specifications). If a system gain calibration is performed the following conditions must be met: 1) Full-scale input must not saturate the 20X instrumentation amplifi-

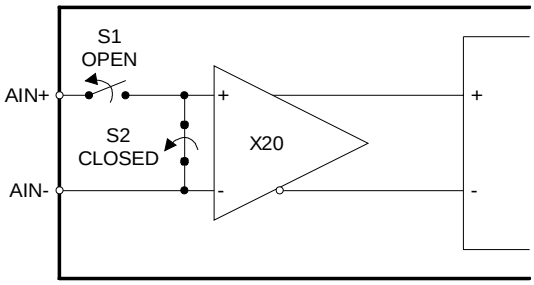



**Figure 10. Self Calibration of Offset (Low Ranges).**

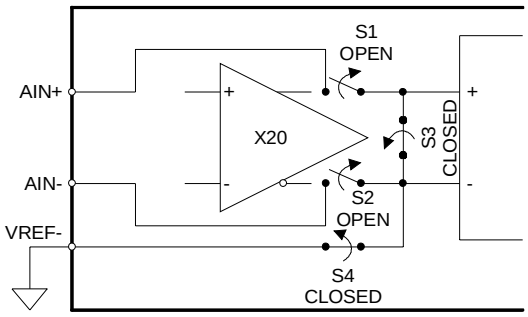



**Figure 11. Self Calibration of Offset (High Ranges).**

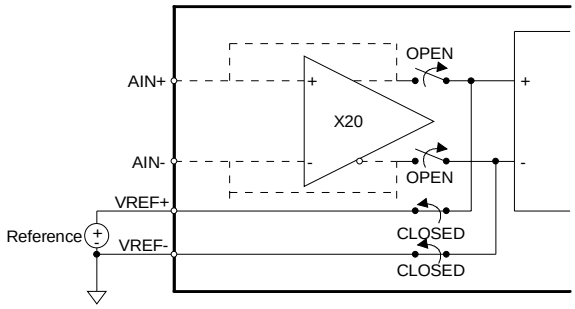



**Figure 12. Self Calibration of Gain (All Ranges).**

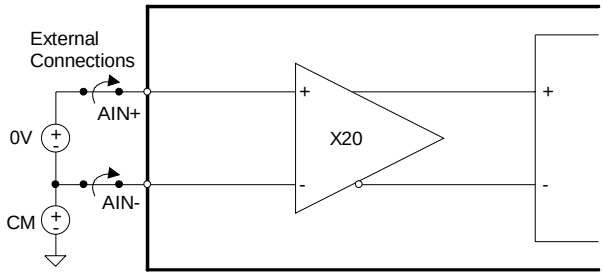



**Figure 13. System Calibration of Offset (Low Ranges).**

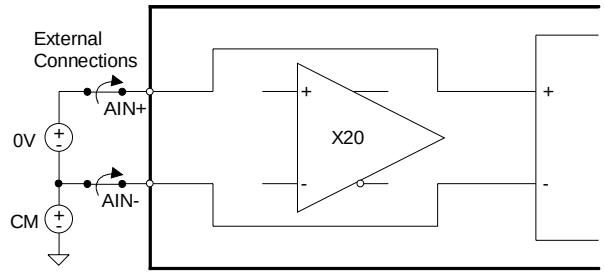



**Figure 14. System Calibration of Offset (High Ranges).**

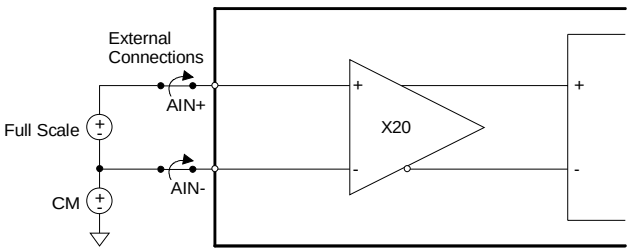



**Figure 15. System Calibration of Gain (Low Ranges)**

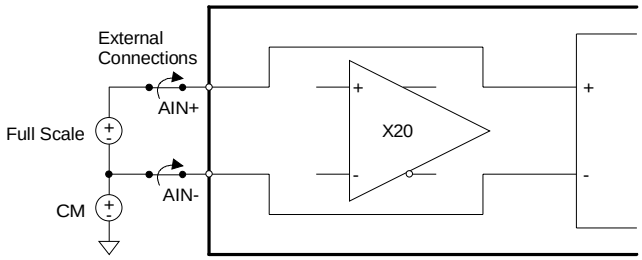



**Figure 16. System Calibration of Gain (High Ranges).**

er, if the calibration is on an input range where the instrumentation amplifier is involved. 2) The 1's density of the modulator must not be greater than 80 percent (the input to the ΔΣ modulator must not exceed the maximum input which Table 6 specifies). 3) The input must not cause the resulting gain register's content, decoded in decimal, to exceed 3.9999998 (see the discussion of operating limits on input span under the *Analog Input* and *Limitations in Calibration Range* sections). The above conditions require the full scale input voltage to the modulator to be at least 25 percent of the nominal value.

The converter's input ranges were chosen to guarantee gain calibration accuracy to 1 LSB when gain calibration is performed. This is useful when a user wants to manually scale the full scale range of the converter and maintain accuracy. For example, if a gain calibration is performed with a 2.5 V full scale voltage and a 1.25 V input range is desired, the user can read the contents of the gain register, shift it by 1 bit, and then write the results back to the gain register.

Assuming a system can provide two known voltages, the following equations allow the user to manually compute the calibration register's values based on two uncalibrated conversions (see note). The offset and gain calibration registers are used to adjust a typical conversion as follows:

$$Rc = (Ru + Co) * Cg / 2^{22}.$$

Calibration can be performed using the following equations:

$$Co = (Rc0/G - Ru0)$$

$$Cg = 2^{22} * G$$

where $G = (Rc1 - Rc0)/(Ru1-Ru0)$.

***Note:*** *Uncalibrated conversions imply that the gain and offset registers are at default {gain register = 0x400000 (Hex) and offset register = 0x000000 (Hex)}.*

The variables are defined below.

| | | |
|---|---|---|
| V0 | = | First calibration voltage |
| V1 | = | Second calibration voltage (greater than V0) |
| Ru | = | Result of any uncalibrated conversion |
| Ru0 | = | Result of uncalibrated conversion V0 (24-bit integer or 2's complement) |
| Ru1 | = | Result of uncalibrated conversion of V1 (24-bit integer or 2's complement) |
| Rc | = | Result of any conversion |
| Rc0 | = | Desired calibrated result of converting V0 (24-bit integer or 2's complement) |
| Rc1 | = | Desired calibrated result of converting V1 (24-bit integer or 2's complement) |
| Co | = | Offset calibration register value (24-bit 2's complement) |
| Cg | = | Gain calibration register value (24-bit integer) |

## Calibration Tips

Calibration steps are performed at the output word rate selected by the WR2-WR0 bits of the configuration register. Since higher word rates result in conversion words with more peak-to-peak noise, calibration should be performed at lower output word rates. Also, to minimize digital noise near the device, the user should wait for each calibration step to be completed before reading or writing to the serial port.

For maximum accuracy, calibrations should be performed for offset and gain (selected by changing the G2-G0 bits of the configuration register). Note that only one gain range can be calibrated per physical channel. And if factory calibration of the user's system is performed using the system calibration

capabilities of the CS5522/24/28, the offset and gain register contents can be read by the system microcontroller and recorded in EEPROM. These same calibration words can then be uploaded into the offset and gain registers of the converter when power is first applied to the system, or when the gain range is changed.

## Limitations in Calibration Range

System calibration can be limited by signal headroom in the analog signal path inside the chip as discussed under the ***Analog Input*** section of this data sheet. For gain calibration the full scale input signal can be reduced to the point in which the gain register reaches its upper limit of ($4\text{-}2^{-22}$ decimal) or FFFFFF (hexadecimal). Under nominal conditions, this occurs with a full scale input signal equal to about 1/4 the nominal full scale. With the converter's intrinsic gain error, this full scale input signal may be higher or lower. In defining the minimum Full Scale Calibration Range (FSCR) under "Analog Characteristics", margin is retained to accommodate the intrinsic gain error. Alternatively the input full scale signal can be increased to a point in which the modulator reaches its 1's density limit of 80 percent, which under nominal condition occurs when the full scale input signal is 1.5 times the nominal full scale. With the chip's intrinsic gain error, this input full scale input signal maybe higher or lower. In defining the maximum FSCR, margin is again incorporated to accommodate the intrinsic gain error. In addition, for full scale inputs greater than the nominal full scale value of the range selected, there is some voltage at which various internal circuits may saturate due to limited amplifier headroom. This is most likely to occur in the 100mV range.

## Analog Output Latch Pins

The A1-A0 pins of the converter mimic the D23/D11-D22/D10 bits of the channel setup registers. A1-A0 can be used to control external multiplexers and other logic functions outside the converter. The outputs can sink or source at least 1 mA, but it is recommended to limit drive currents to less than 20 µA to reduce self-heating of the chip. These outputs are powered from VA+, hence, their output voltage for a logic 1 will be limited to the VA+ voltage.

## Output Word Rate Selection

The WR2-WR0 bits of the channel-setup registers set the output conversion word rate of the converter as shown in Table 4. The word rates indicated in the table assume a master clock of 32.768 kHz. Upon reset the converter is set to operate with an output word rate of 15.0 Hz.

## Clock Generator

The CS5522/24/28 include a gate which can be connected with an external crystal to provide the master clock for the chip. The chips are designed to operate using a low-cost 32.768 kHz "tuning fork" type crystal. One lead of the crystal should be connected to XIN and the other to XOUT. Lead lengths should be minimized to reduce stray capacitance.

The converters will operate with an external (CMOS compatible) clock with frequencies up to 100kHz the crystal. Figure 17 details the converter's performance at increased clock rates.

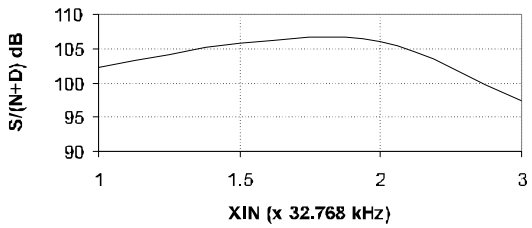



**Figure 17. High Speed Clock Performance**

The 32.768 kHz crystal is normally specified as a time-keeping crystal with tight specifications for both initial frequency and for drift over temperature. To maintain excellent frequency stability, these crystals are specified only over limited operating temperature ranges (i.e. -10 °C to +60 °C).

However, applications with the CS5522/24/28 don't generally require such tight tolerances.

## Digital Filter

The CS5522/24/28 have eight different linear phase digital filters which set the output word rates (OWRs) as stated in Table 4. These rates assume that XIN is 32.768 kHz. Each of the filters has a magnitude response similar to that shown in Figure 18. The filters are optimized to settle to full accuracy every conversion and yield better than 80 dB rejection for both 50 and 60 Hz with output word rates at or below 15.0 Hz.

The converter's digital filters scale with XIN. For example with an output word rate of 15 Hz, the filter's corner frequency is typically 12.7 Hz. If XIN is increased to 64.536 kHz the OWR doubles and the filter's corner frequency moves to 25.4 Hz.

## Output Coding

The CS5522/24/28 output data in binary format when operating in unipolar mode and in two's complement when operating in bipolar mode.

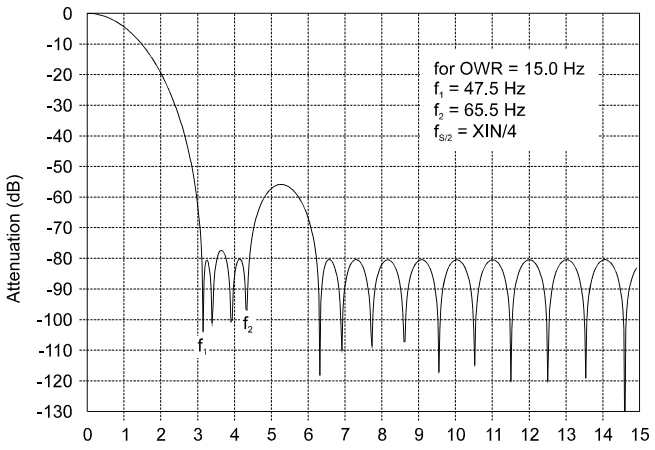



**Figure 18. Filter Response (Normalized to Output Word Rate = 1)**

The output conversion word is 24 bits, or three bytes long, as shown in Table 8. The MSB is output first followed by the rest of the data bits in descending order.

## Power Consumption

The CS5522/24/28 accommodate four power consumption modes: normal, low power, standby, and

### *Output Conversion Data (24 bits)*

| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | LSB |

| Unipolar Input Voltage | Offset Binary | Bipolar Input Voltage | Two's Complement |
|---|---|---|---|
| >(VFS-1.5 LSB) | FFFFFF | >(VFS-1.5 LSB) | 7FFFFF |
| VFS-1.5 LSB | FFFFFF<br>------<br>FFFFFE | VFS-1.5 LSB | 7FFFFF<br>------<br>7FFFFE |
| VFS/2-0.5 LSB | 800000<br>------<br>7FFFFF | -0.5 LSB | 000000<br>------<br>FFFFFF |
| +0.5 LSB | 000001<br>------<br>000000 | -VFS+0.5 LSB | 800001<br>------<br>800000 |
| <(+0.5 LSB) | 000000 | <(-VFS+0.5 LSB) | 800000 |

Note: VFS in the table equals the voltage between ground and full scale for any of the unipolar gain ranges, or the voltage between ± full scale for any of the bipolar gain ranges. See text about error flags under overrange conditions.

**Table 8. CS5522/24/28 Output Coding and Data Conversion Word**

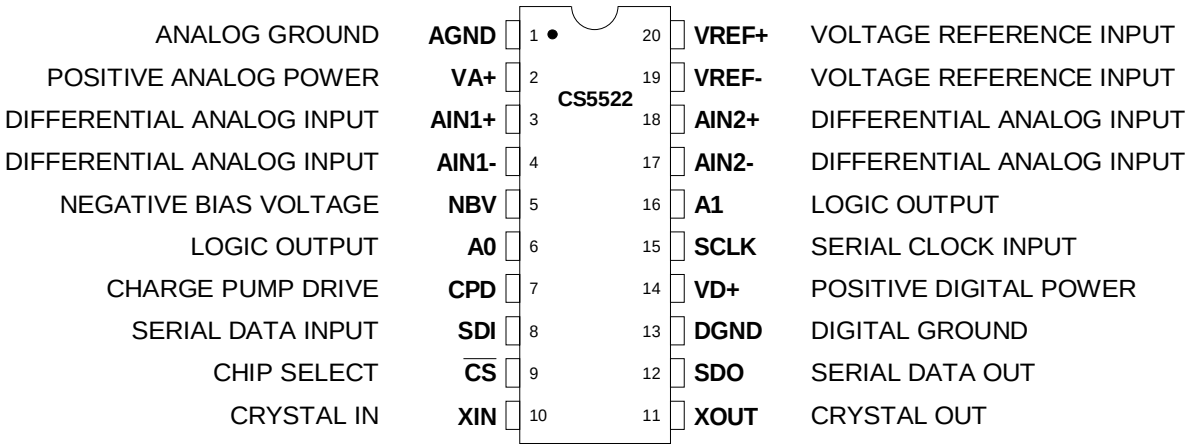
sleep. The normal mode, the default mode, is entered after a power-on-reset and typically consumes 9.0 mW. The low power mode is an alternate mode that reduces the consumed power to 5.5 mW. It is entered by setting bit D8 (the low power mode bit) in the configuration register to logic 1. Slightly degraded noise or linearity performance should be expected in the low power mode. The final two modes are referred to as the power save modes. They power down most of the analog portion of the chip and stop filter convolutions. The power save modes are entered whenever the PS/$\overline{R}$ bit of the configuration register is set to logic 1. The particular power save mode entered depends on state of bit D11 (PSS, the Power Save Select bit) in the configuration register. If PSS is logic 0, the converter enters the standby mode reducing the power consumption to 1.2 mW. The standby mode leaves the oscillator and the on-chip bias generator running. This allows the converter to quickly return to the normal or low power mode once the PS/$\overline{R}$ bit is set back to a logic 1. If PSS and PS/$\overline{R}$ in the configuration register are set to logic 1, the sleep mode is entered reducing the consumed power to around 500 µW. Since the sleep mode disables the oscillator, approximately a 500ms oscillator start-up delay period is required before returning to the normal or low power mode.

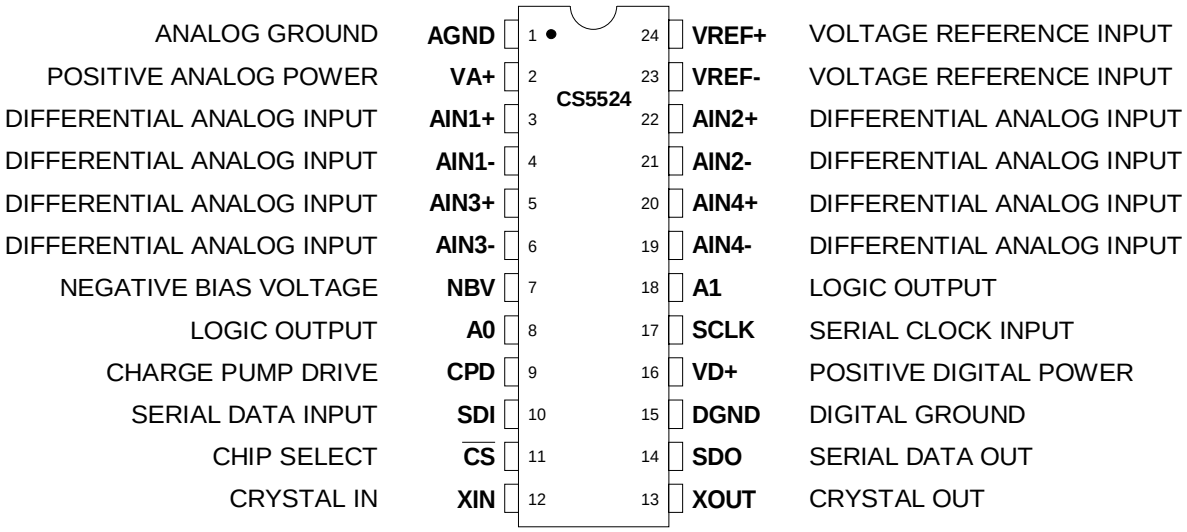
## PCB Layout

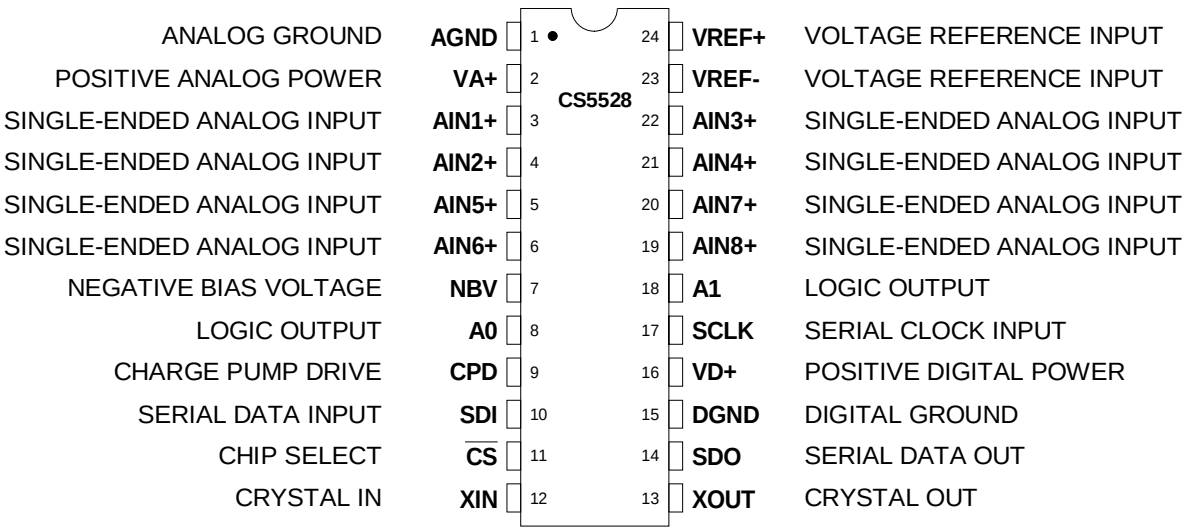
The CS5522/24/28 should be placed entirely over an analog ground plane with both the AGND and DGND pins of the device connected to the analog plane. Place the analog-digital plane split immediately adjacent to the digital portion of the chip. If separate digital (VD+) and analog (VA+) supplies are used, it is recommended that a diode be placed between them (the cathode of the diode should point to VA+). If the digital supply comes up before the analog supply, the ADC may not start up properly.

***Note:*** *See the CDB5522 data sheet for suggested layout details and Applications Note 18 for more detailed layout guidelines. Before layout, please call for our Free Schematic Review Service.*

## PIN DESCRIPTIONS



### *Clock Generator*

**XIN; XOUT - Crystal In; Crystal Out.**

A gate inside the chip is connected to these pins and can be used with a crystal to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be supplied into the XIN pin to provide the master clock for the device.

### *Control Pins and Serial Data I/O*

**$\overline{\text{CS}}$ - Chip Select.**

When active low, the port will recognize SCLK. When high the SDO pin will output a high impedance state. $\overline{\text{CS}}$ should be changed when SCLK = 0.

**SDI - Serial Data Input.**

SDI is the input pin of the serial input port. Data will be input at a rate determined by SCLK.

**SDO - Serial Data Output.**

SDO is the serial data output. It will output a high impedance state if $\overline{\text{CS}}$ = 1.

**SCLK - Serial Clock Input.**

A clock signal on this pin determines the input/output rate of the data for the SDI/SDO pins respectively. This input is a Schmitt trigger to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{\text{CS}}$ is low.

**A0, A1 - Logic Outputs.**

The logic states of A0-A1 mimic the states of the D22/D10-D23/D11 bits of the channel-setup register. Logic Output 0 = AGND, and Logic Output 1 = VA+.

### *Measurement and Reference Inputs*

**AIN1+, AIN1-, AIN2+, AIN2- AIN3+, AIN3-, AIN4+, AIN4- - Differential Analog Input.**

Differential input pins into the CS5522 and CS5524 devices.

**AIN1+, AIN2+, AIN3+, AIN4+, AIN5+, AIN6+, AIN7+, AIN8+ - Single-Ended Analog Input.**

Single-ended input pins into the CS5528.

**VREF+, VREF- - Voltage Reference Input.**

Fully differential inputs which establish the voltage reference for the on-chip modulator.

**NBV - Negative Bias Voltage.**

Input pin to supply the negative supply voltage for the 20X gain instrumentation amplifier and coarse/fine charge buffers. May be tied to AGND if AIN+ and AIN- inputs are centered around +2.5 V; or it may be tied to a negative supply voltage (-2.1 V typical) to allow the amplifier to handle low level signals more negative than ground. When using the CS5528 in either the 25mV, 55mV or 100mV range, the analog inputs are expected to be ground referenced; therefore, NBV must be between -1.8 to -2.5 to ensure proper operation.

**CPD - Charge Pump Drive.**

Square wave output used to provide energy for the charge pump.

### *Power Supply Connections*

**VA+ - Positive Analog Power.**

Positive analog supply voltage. Nominally +5 V.

**VD+ - Positive Digital Power.**

Positive digital supply voltage. Nominally +3.0 V or +5 V.

**AGND - Analog Ground.**

Analog Ground.

**DGND - Digital Ground.**

Digital Ground.

## SPECIFICATION DEFINITIONS

### Linearity Error

The deviation of a code from a straight line which connects the two endpoints of the A/D Converter transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

### Differential Nonlinearity

The deviation of a code's width from the ideal width. Units in LSBs.

### Full Scale Error

The deviation of the last code transition from the ideal [{(VREF+) - (VREF-)} - 3/2 LSB]. Units are in LSBs.

### Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above the voltage on the AIN- pin.). When in unipolar mode (U/$\overline{B}$ bit = 1). Units are in LSBs.

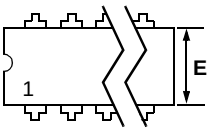
### Bipolar Offset

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below the voltage on the AIN- pin). When in bipolar mode (U/$\overline{B}$ bit = 0). Units are in LSBs.

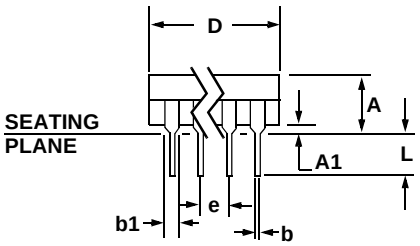
## ORDERING GUIDE

| Model Number | Linearity Error (Max) | Temperature Range | Package |
|---|---|---|---|
| CS5522-AP | ±0.0015% | -40°C to +85°C | 20-pin 0.3" Skinny Plastic DIP |
| CS5522-AS | ±0.0015% | -40°C to +85°C | 20-pin 0.2" Plastic SSOP |
| CS5524-AP | ±0.0015% | -40°C to +85°C | 24-pin 0.3" Skinny Plastic DIP |
| CS5524-AS | ±0.0015% | -40°C to +85°C | 24-pin 0.2" Plastic SSOP |
| CS5528-AP | ±0.0015% | -40°C to +85°C | 24-pin 0.3" Skinny Plastic DIP |
| CS5528-AS | ±0.0015% | -40°C to +85°C | 24-pin 0.2" Plastic SSOP |

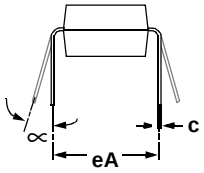
## 20 PIN PLASTIC (PDIP) PACKAGE DRAWING




TOP VIEW




BOTTOM VIEW




SIDE VIEW

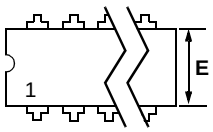
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| **DIM** | **MIN** | **MAX** | **MIN** | **MAX** |
| A | 0.155 | 0.180 | 3.94 | 4.57 |
| A1 | 0.020 | 0.040 | 0.51 | 1.02 |
| b | 0.015 | 0.022 | 0.38 | 0.56 |
| b1 | 0.050 | 0.065 | 1.27 | 1.65 |
| c | 0.008 | 0.015 | 0.20 | 0.38 |
| D | 0.960 | 1.040 | 24.38 | 26.42 |
| E | 0.240 | 0.260 | 6.10 | 6.60 |
| e | 0.095 | 0.105 | 2.41 | 2.67 |
| eA | 0.300 | 0.325 | 7.62 | 8.25 |
| L | 0.125 | 0.150 | 3.18 | 3.81 |
| ∝ | 0° | 15° | 0° | 15° |

Notes: 1. Positional tolerance of leads shall be within 0.25 mm (0.010 in.) at maximum material condition, in relation to seating plane and each other.

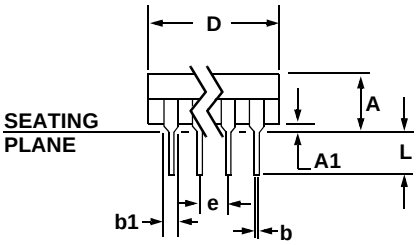
2. Dimension eA to center of leads when formed parallel.

3. Dimension E does not include mold flash.

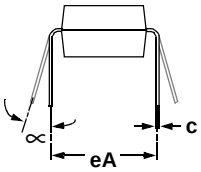
## 24 PIN SKINNY (PDIP) PACKAGE DRAWING




TOP VIEW




BOTTOM VIEW




SIDE VIEW

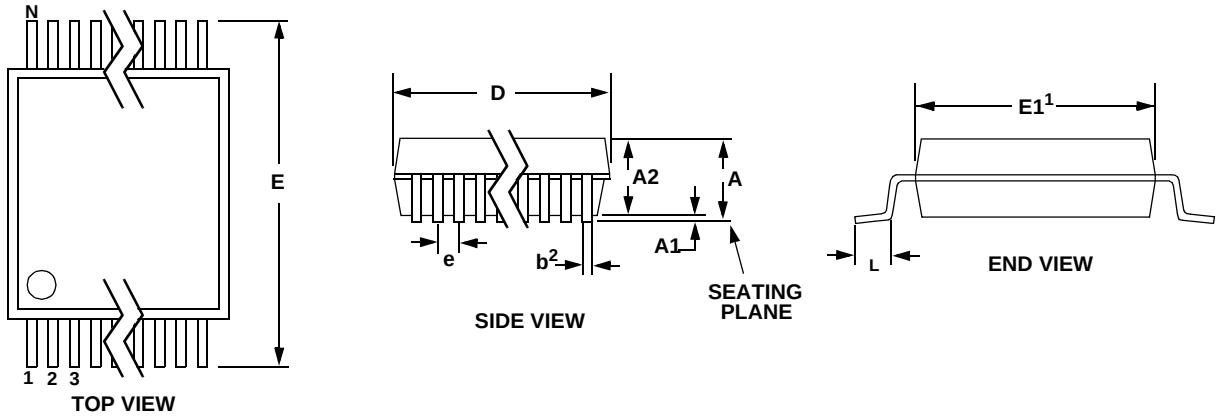
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| **DIM** | **MIN** | **MAX** | **MIN** | **MAX** |
| A | 0.155 | 0.180 | 3.94 | 4.57 |
| A1 | 0.020 | 0.040 | 0.51 | 1.02 |
| b | 0.014 | 0.022 | 0.36 | 0.56 |
| b1 | 0.040 | 0.065 | 1.02 | 1.65 |
| c | 0.008 | 0.015 | 0.20 | 0.38 |
| D | 1.235 | 1.265 | 31.37 | 32.13 |
| E | 0.240 | 0.260 | 6.10 | 6.60 |
| e | 0.095 | 0.105 | 2.41 | 2.67 |
| eA | 0.300 | 0.325 | 7.62 | 8.25 |
| L | 0.125 | 0.150 | 3.18 | 3.81 |
| ∝ | 0° | 15° | 0° | 15° |

Notes: 1. Positional tolerance of leads shall be within 0.25 mm (0.010 in.) at maximum material condition, in relation to seating plane and each other.

2. Dimension eA to center of leads when formed parallel.

3. Dimension E does not include mold flash.

## 20 PIN SSOP PACKAGE DRAWING



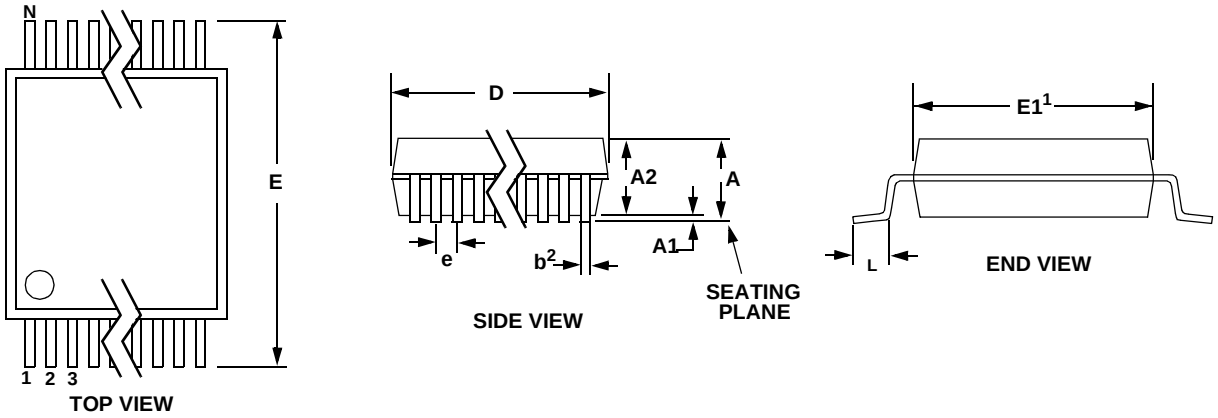

| | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX | |
| A | -- | 0.084 | -- | 2.13 | |
| A1 | 0.002 | 0.010 | 0.05 | 0.25 | |
| A2 | 0.064 | 0.074 | 1.62 | 1.88 | |
| b | 0.009 | 0.015 | 0.22 | 0.38 | 2,3 |
| D | 0.272 | 0.295 | 6.90 | 7.50 | 1 |
| E | 0.291 | 0.323 | 7.40 | 8.20 | |
| E1 | 0.197 | 0.220 | 5.00 | 5.60 | 1 |
| e | 0.024 | 0.027 | 0.61 | 0.69 | |
| L | 0.025 | 0.040 | 0.63 | 1.03 | |
| ∝ | 0° | 8° | 0° | 8° | |

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

## 24 PIN SSOP PACKAGE DRAWING




| | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX | |
| A | -- | 0.084 | -- | 2.13 | |
| A1 | 0.002 | 0.010 | 0.05 | 0.25 | |
| A2 | 0.064 | 0.074 | 1.62 | 1.88 | |
| b | 0.009 | 0.015 | 0.22 | 0.38 | 2,3 |
| D | 0.311 | 0.335 | 7.90 | 8.50 | 1 |
| E | 0.291 | 0.323 | 7.40 | 8.20 | |
| E1 | 0.197 | 0.220 | 5.00 | 5.60 | 1 |
| e | 0.024 | 0.027 | 0.61 | 0.69 | |
| L | 0.025 | 0.040 | 0.63 | 1.03 | |
| ∝ | 0° | 8° | 0° | 8° | |

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

# • Notes •