A DIVISION OF CIRRUS LOGIC

CS4912

Multi-Function Digital Audio Processor

Features

- 24-bit DSP with On-chip Program RAM, Data RAM, and Stereo DAC
- 24x24 Multiplier with 48-bit Accumulator
- CD Quality Stereo DAC with Output Filter
- I^2C® or SPI Serial Control Port
- Integrated S/PDIF Digital Transmitter Port
- Serial Audio Port, up to 4 In/6 Out
- Asynchronous Audio Input Port
- Programmable Phase Locked Loop
- +5 Volt Only CMOS, 44-pin PLCC

Crystal DSP Application Firmware Kits

- Car Audio Processing for Head or Amp Units
  - Crossover Filters, Parametric or Graphic EQs
  - Compressor, Peak Limiter, Noise Gate
  - 4-channel Adjustable Time Delay
- Dolby® Surround Pro Logic™ Decoder
  - Multiple Output Configurations
  - 3D Virtual Surround for 2 Speaker Playback
- Musical Instrument Reverb/Effects

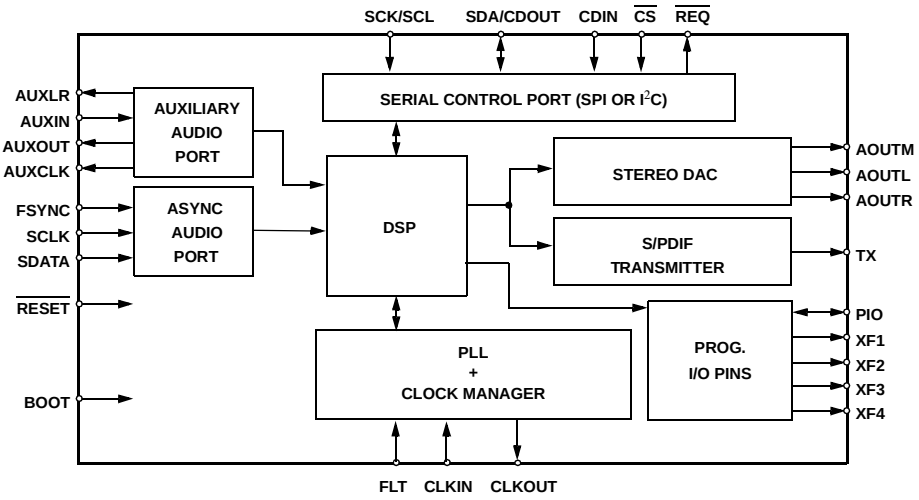
Description

The CS4912 is a highly integrated and cost effective audio processing system for a variety of applications. This device integrates a 24-bit DSP with on-chip program and data RAM, a stereo DAC, a full-duplex serial audio interface, a digital audio transmitter, an asynchronous audio input port, a serial control port, and a phase-locked loop clock generator. The CS4912 may be coupled with an ADC such as the CS5331 for 2-in / 2-out audio applications. A 2-in / 4-out system would include the CS4912 and a stereo CODEC (CS4222), and a 4-in / 6-out system can be built using the CS4912 with two CODECs and a small amount of external logic.

The CS4912 is configured for specific applications by DSP code loaded into the on-chip RAM. The device can be initialized by an external microcontroller, or booted directly from a serial EEPROM using a small amount of external logic. The CRD4912 board is an evaluation platform for the CS4912, with complete documentation to simplify the design process. CS4912 application firmware kits are available for Car Audio Processing, Dolby Pro Logic Decoding, and Reverb/Effects applications. Ordering information for the application firmware kits is included in the CRD4912 data sheet.

ORDERING INFORMATION

CS4912-CL	44-pin PLCC
CRD4912-01	Reference Design Kit



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

Cirrus Logic, Inc.
Crystal Semiconductor Products Division
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.crystal.com

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Parameter*		Symbol	Min	Typ	Max	Unit
Dynamic Performance						
DAC Resolution			16	-	-	Bits
DAC Differential Nonlinearity		DNL	-	-	±0.9	LSB
Total Harmonic Distortion	AOUTL, AOUTR (Note 1) AOUTM	THD	- -	0.01 0.02	0.015 0.03	%
Instantaneous Dynamic Range (DAC not muted, A weighted)	AOUTL, AOUTR (Note 1) AOUTM	IDR	85 80	90 85	- -	dB
Interchannel Isolation	(Note 1)		-	85	-	dB
Interchannel Gain Mismatch			-	-	0.2	dB
Pass Band Flatness			-3.0	-	+0.2	dB
Full Scale Output Voltage	AOUTL, AOUTR (Note 1) AOUTM		2.66 2.7	2.88 3.0	3.2 3.3	Vpp
Gain Drift			-	100	-	ppm/°C
Deviation from Linear Phase			-	-	5	Deg
Out of Band Energy	(Fs/2 to 2 Fs)		-	-60	-	dB
Analog Output Load	Resistance Capacitance		8 -	- -	- 100	kΩ pF
Power Supply						
Power Supply Rejection	(1 kHz)		-	40	-	dB
Power Supply Consumption	VA+ VD+		- -	20 100	40 140	mA mA

D/A INTERPOLATION FILTER CHARACTERISTICS (See graphs toward the end of this data sheet)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (-3 dB)		0	-	0.476 Fs	Hz
Passband Ripple		-	-	±0.1	dB
Transition Band		0.442 Fs	-	0.567 Fs	Hz
Stop Band		≥0.567 Fs	-	-	Hz
Stop Band Rejection		50	-	-	dB
Stop Band Rejection with Ext. 2 Fs RC filter		57	-	-	dB
Group Delay		-	12/Fs	-	s

Notes: 1. 10 kΩ, 100 pF load for each analog signal (Left, Right).
30 kΩ, 100 pF load for analog Mono signal.

* Refer to *Parameter Definitions* at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Unit
DC Power Supplies	Positive Digital	VD+	-0.3	6.0	V
	Positive Analog	VA+	-0.3	6.0	V
	|VA+ - VD+|		-	0.4	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	(VD+) + 0.4	V
Ambient Operating Temperature (power applied)		T_{Amax}	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0 V; all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	Positive Digital	VD+	4.50	5.0	5.50	V
	Positive Analog	VA+	4.50	5.0	5.50	V
	|VA+ - VD+|		-	-	0.4	V
Ambient Operating Temperature		T_A	0	-	+ 70	°C

DIGITAL CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V ±10%; measurements performed under static conditions.)

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage		V_{IH}	2.2	-	-	V
	SCK/SCL		2.5	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	0.8	V
High-Level Output Voltage at I_o = -2.0 mA		V_{OH}	VD x 0.9	-	-	V
Low-Level Output Voltage at I_o = 2.0 mA		V_{OL}	-	-	VD x 0.1	V
Input Leakage Current	(Note 2)	I_{in}	-	-	1.0	µA

SWITCHING CHARACTERISTICS - CLOCKS (T_A = 25 °C; VA+, VD+ = 5 V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Reference Clock Frequency		CLKIN	0.256	12.288	30	MHz
Reference Clock Duty Cycle		CYCK	40	50	60	%
Alternate Clock	P = 0	ALTCLK	-	512 Fs	-	Hz
	P = 1		-	768 Fs	-	Hz
Clock Output		CLKOUT	-	-	384 Fs	Hz

2. Not Valid for pin numbers 9, 12, 13, and 30 which are configured with on-chip pull-down resistors. Not valid for pin number 29 which is a static input signal and should be tied to either VD+ or DGND.

SWITCHING CHARACTERISTICS - EXTERNAL FLAGS (T_A = 25 °C; VA+, VD+ = 5 V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Rise time of XF1-XF4	(Note 3)	t_{rxf}	-	-	200	ns
Fall time of XF1-XF4	(Note 3)	t_{fxf}	-	-	100	ns

SWITCHING CHARACTERISTICS - PROGRAMMABLE INPUT/OUTPUT

(T_A = 25 °C; VA+, VD+ = 5 V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Input Frequency	f_{pio}	-	-	350	kHz
Input Rise Time	t_{rpio}	-	-	200	ns
Input Fall Time	t_{fpio}	-	-	200	ns
Output Rise Time	t_{rpo}	-	-	200	ns
Output Fall Time	t_{fpo}	-	-	200	ns

SWITCHING CHARACTERISTICS - BOOT INITIALIZATION

(T_A = 25 °C; VA+, VD+ = 5 V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20 pF)

Parameter		Symbol	Min	Max	Unit
BOOT Rising to $\overline{\text{RESET}}$ Rising Setup Time		t_{bsu}	350	-	ns
$\overline{\text{RESET}}$ Rising to Boot Falling Hold Time		t_{bh}	450	-	ns
$\overline{\text{CS}}$ Rising to $\overline{\text{RESET}}$ Rising Setup Time		t_{cssu}	200	-	ns
$\overline{\text{RESET}}$ Rising to $\overline{\text{CS}}$ Hold Time		t_{csh}	400	-	ns
$\overline{\text{RESET}}$ Low Time		t_{rlow}	50	-	µs
SCK/SCL Delay Time from $\overline{\text{RESET}}$ Rising	(Note 4)	t_{rsc}	2	-	ms
SCK/SCL falling to $\overline{\text{CS}}$ rising on last byte of download		t_{sfcr}	3	-	µs

Notes: 3. 2 kΩ pull-up to 5 V supply on XF1-XF4 pins

4. This delay is necessary after any rising edge of $\overline{\text{RESET}}$ to allow time for the part to initialize and for the on-board PLL to stabilize.

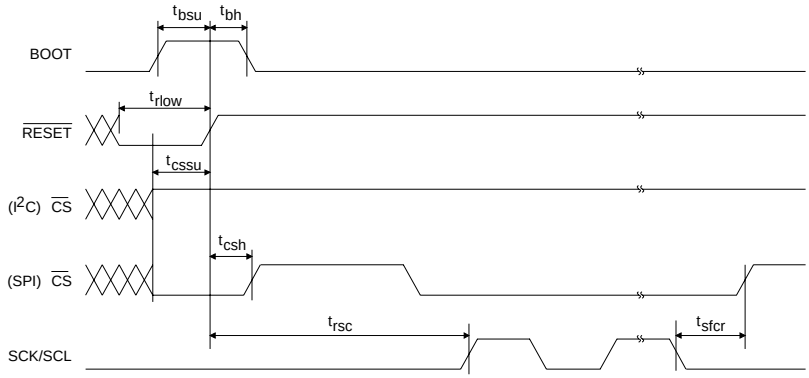


Figure 1. Boot Timing

SWITCHING CHARACTERISTICS - CONTROL PORT (T_A = 25 °C; VA+, VD+ = 5 V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20 pF)

Parameter		Symbol	Min	Max	Unit
SPI Mode ($\overline{CS}$ = 0)					
SCK/SCL Clock Frequency	(slow mode) (fast mode)	f_{sck} f_{sck}	- -	350 2000	kHz
$\overline{CS}$ Falling to SCK/SCL Rising	(slow mode)	t_{css}	20	-	ns
Rise Time of Both CDIN and SCK/SCL Lines	(slow mode)	t_r	-	50	ns
Fall Time of Both CDIN and SCK/SCL Lines	(slow mode) (fast mode)	t_f t_f	- -	300 50	ns ns
SCK/SCL Low Time	(slow mode) (fast mode)	t_{scl} t_{scl}	1100 150	- -	ns ns
SCK/SCL High Time	(slow mode) (fast mode)	t_{sch} t_{sch}	1100 150	- -	ns ns
Setup Time CDIN to SCK/SCL Rising	(slow mode) (fast mode)	t_{cdisu}	250 50	- -	ns ns
Hold Time SCK/SCL Rising to CDIN	(Note 5)	t_{cdih}	50	-	ns
Transition Time from SCK/SCL to CDOUT Valid	(Note 6)	t_{scdov}	-	40	ns
Time from SCK/SCL Rising to $\overline{REQ}$ Rising	(Note 7)	t_{scrh}	-	200	ns
Rise Time for $\overline{REQ}$	(Note 7)	t_{rr}	-	50	ns
Fall Time for $\overline{REQ}$	(Note 7)	t_{rf}	-	20	ns
Hold Time for $\overline{REQ}$ from SCK/SCL Rising		t_{scrl}	0	-	ns
Time from SCK/SCL Falling to $\overline{CS}$ Rising		t_{sccsh}	20	-	ns
High Time Between Active $\overline{CS}$		t_{csht}	200	-	ns

Notes: 5. Data must be held for sufficient time to bridge 300(50) ns transition time of SCK/SCL.

6. CDOUT should NOT be sampled during this time period.

7. 2 kΩ Pull-up resistor to VD+, DSP clock is 36.864 MHz.

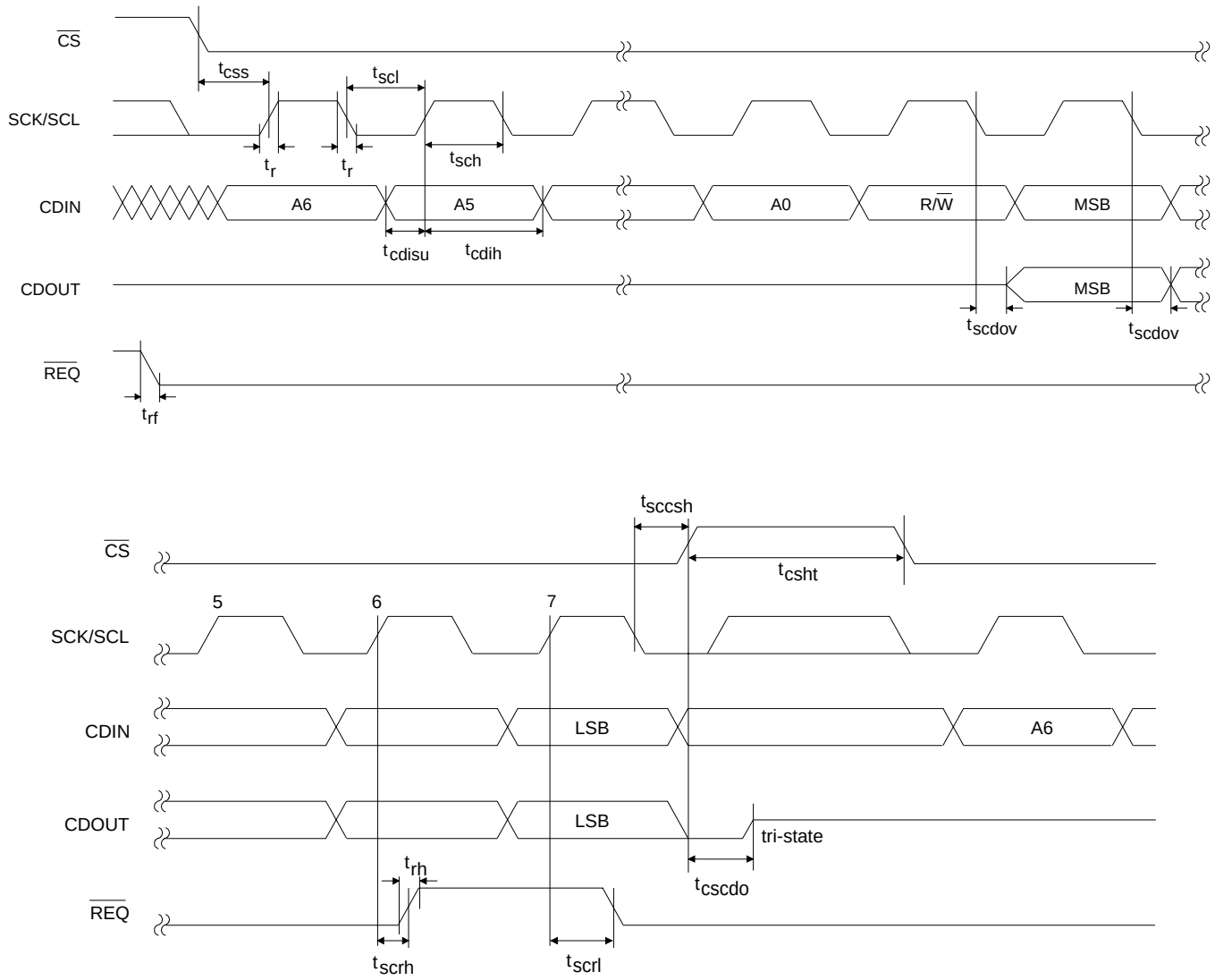


Figure 2. SPI Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT (T_A = 25 °C; VA+, VD+ = 5 V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20 pF)

Parameter		Symbol	Min	Max	Units
I^2C Mode ($\overline{CS}$=1)					
SCK/SCL Clock Frequency	(slow mode) (fast mode)	f_{scl}	- -	100 400	kHz
Bus Free Time Between Transmissions		t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0	-	µs
Clock Low Time	(slow mode) (fast mode)	t_{low}	4.7 1.2	- -	µs
Clock High Time	(slow mode) (fast mode)	t_{high}	4.0 1.0	- -	µs
SDA Setup Time to SCK/SCL Rising		t_{sud}	250	-	ns
SDA Hold Time from SCK/SCL Falling	(Note 8)	t_{hdd}	0	-	µs
Rise Time of Both SDA and SCK/SCL	(Note 9)	t_r	-	50	ns
Fall Time of Both SDA and SCK/SCL		t_f	-	300	ns
Time from SCK/SCL Falling to CS4912 ACK		t_{sca}	-	40	ns
Time from SCK/SCL Falling to SDA Valid During READ Operation		t_{scsdv}	-	40	ns
Time from SCK/SCL Rising to $\overline{REQ}$ Rising	(Note 7)	t_{scrh}	-	200	ns
Hold Time for $\overline{REQ}$ from SCK/SCL Rising)		t_{scrl}	0	-	ns
Rise Time for $\overline{REQ}$	(Note 7)	t_{rr}	-	50	ns
Fall Time for $\overline{REQ}$		t_{rf}	-	20	ns
Setup Time for Stop Condition		t_{susp}	4.7	-	µs

Notes: 8. Data must be held for sufficient time to bridge the 300 ns transition time of SCK/SCL.

9. This rise time is shorter than the I^2C specifications recommend, please refer to the section on SCP communications for more information.

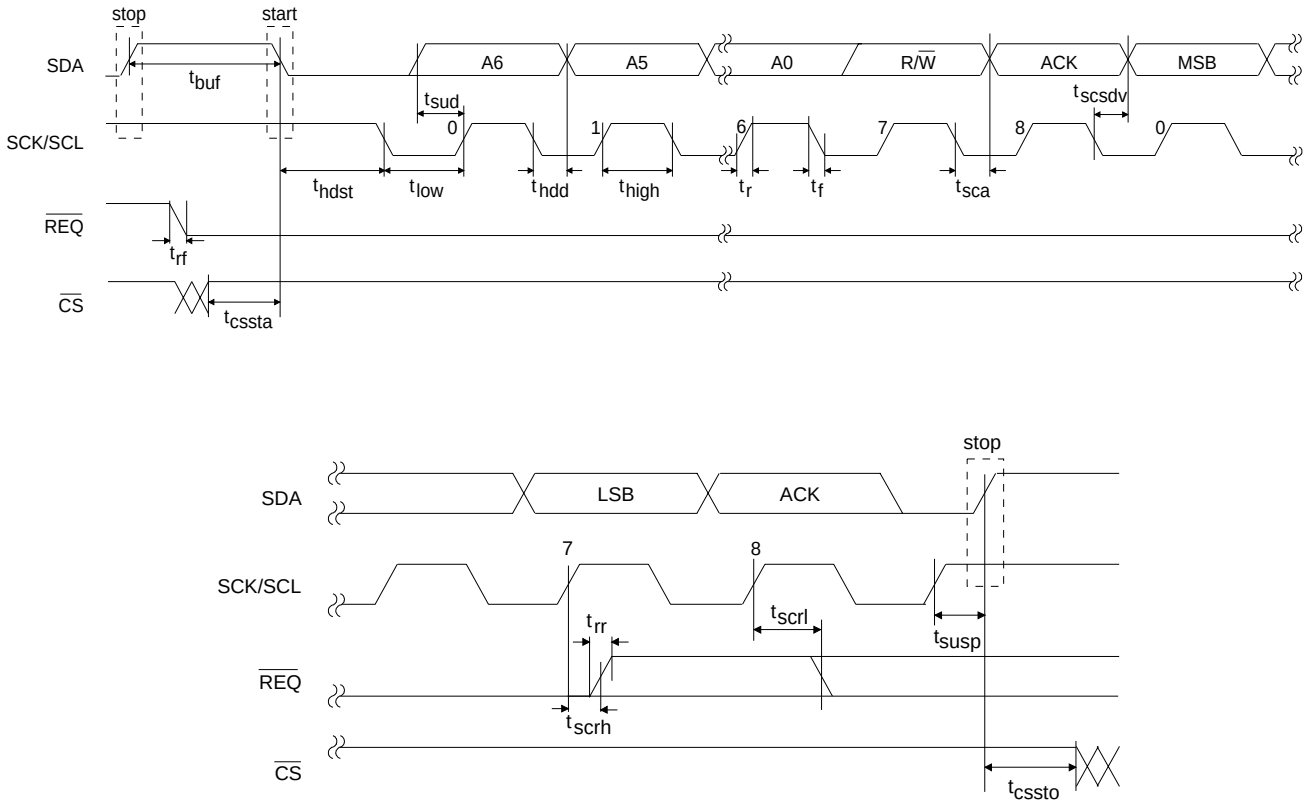


Figure 3. I²C Control Port Timing

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

(T_A = 25 °C; VA+, VD+ = 5 V; Inputs: Logic 0 = GND, Logic 1 = VD+; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
SCLK Frequency			-	-	12.5	MHz
SCLK Pulse Width Low		t_{sckl}	25	-	-	ns
SCLK Pulse Width High		t_{sckh}	25	-	-	ns
SCLK rising to FSYNC edge delay	(Note 10)	t_{sfds}	20	-	-	ns
SCLK rising to FSYNC edge setup	(Note 10)	t_{sfs}	20	-	-	ns
SDATA valid to SCLK rising setup	(Note 10)	t_{sss}	20	-	-	ns
SCLK rising to SDATA hold time	(Note 10)	t_{ssh}	20	-	-	ns
Rise time of SCLK		t_{sclr}	-	-	20	ns

Notes: 10. The Serial Audio Port table above assumes data is output on the falling edge and latched on the rising edge (EDG = 1).

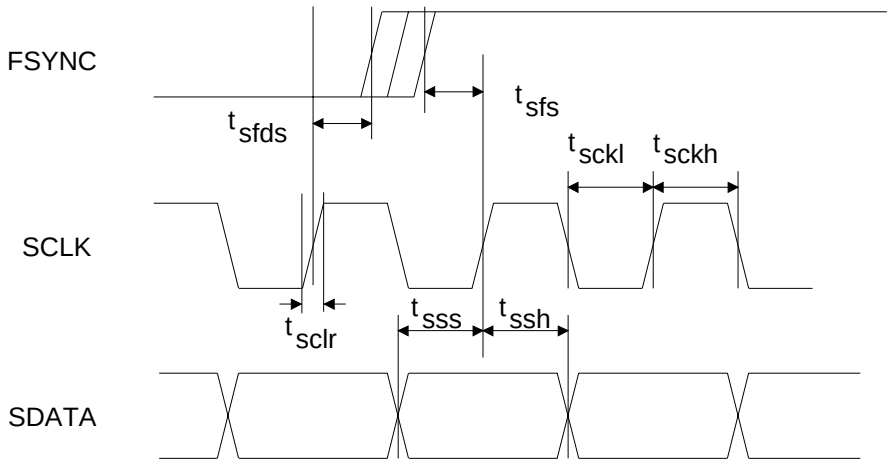


Figure 4. Serial Audio Port Timing

SWITCHING CHARACTERISTICS - AUXILIARY DIGITAL AUDIO PORT

Parameter		Symbol	Min	Typ	Max	Units
Input Sample Rate	(Note 11)	Fs	16	-	48	kHz
AUXCLK Period	(Note 12)	t_{sclk}	- - -	1/(32 Fs) 1/(64 Fs) 1/(128 Fs)	- - -	ns
AUXCLK to AUXLR valid		t_{lrun}	0	-	25	ns
AUXCLK to AUXOUT data valid		t_{doun}	0	-	25	ns
AUXIN data setup time to AUXCLK		t_{disu}	50	-	-	ns
AUXIN data hold time from AUXCLK		t_{diho}	3	-	-	ns

Notes: 11. Fs determined by clock input rate and configuration of on-chip PLL.

12. AUXCLK frequency selectable @ 32, 64, or 128 Fs.

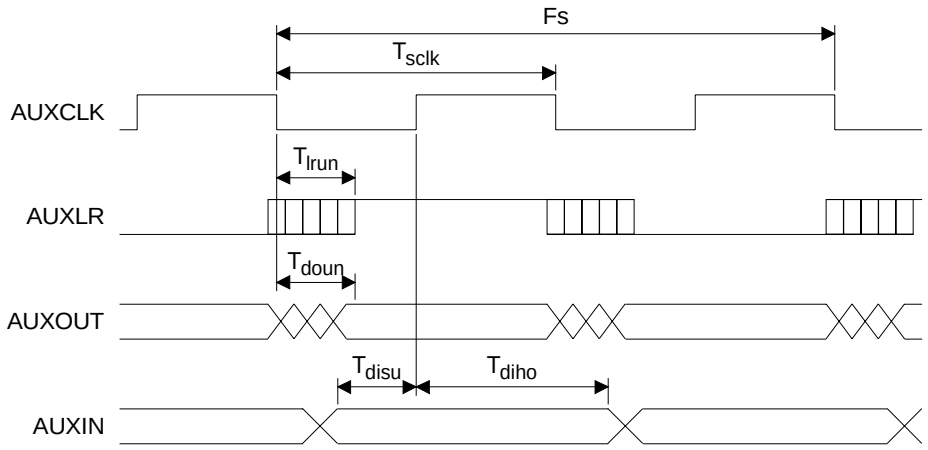


Figure 5. Auxiliary Audio Port Timing

THEORY OF OPERATION

Introduction

The CS4912 is a highly integrated Digital Signal Processor (DSP) system-on-a-chip which is well suited for a number of audio signal processing applications. The large quantity of on-chip RAM and 6 integrated peripherals deliver system functionality and flexibility while reducing system cost. The RAM-based CS4912 may be configured for a number of different audio processing applications by loading DSP code and parameter data into on-chip RAM memories. The CS4912 may be booted via the serial control port from a microcontroller or directly from ROM with a small amount of external logic (see the CRD4912 reference design documentation for details). The serial control port can be configured to operate in either I^2C® or SPI-compatible format. The control port may also be used during run time to communicate with the CS4912 DSP.

DSP application firmware kits are available from Crystal for Dolby Pro Logic/Virtual Surround Decoding applications, a variety of Car Audio Processing applications, and Reverb/Chorus effects processing applications. Contact your local sales representative for details on the latest DSP firmware kits available. Figure 6 shows a typical connection diagram for the CS4912 in which a microcontroller is used for loading the program code. The CRD4912 Reference Design board provides system design and implementation details as well as a flexible platform which can be used to evaluate the performance of the CS4912 device and associated DSP application firmware available from Crystal.

PROCESSOR

The DSP has a fixed-point execution unit with a 24 x 24-bit multiplier, a 48-bit accumulator, and a 24-bit arithmetic logic unit (ALU). Modulo and bit reverse addressing are supported as well as auto post-decrement addressing. Non-branching instructions are executed in a single instruction cycle. For a sample rate (Fs) of 48 kHz, the DSP can execute up to 18 million instructions per second (18 MIPS).

PERIPHERALS

The CS4912 DSP core is integrated with six on-chip peripheral devices: a stereo digital-to-analog converter (DAC), a bidirectional auxiliary serial audio port, an asynchronous serial input port, a digital audio transmitter, a clock generator, and an SPI/I^2C serial control port. Each peripheral has I/O mapped data, control, and status registers. Some of the peripherals have the ability to generate DSP interrupts. The peripheral devices are described in more detail in the following paragraphs.

Digital to Analog Converter

The on-chip stereo DAC utilizes delta-sigma architecture. As shown in Figure 7, digital audio data is interpolated to either 128 Fs or 192 Fs prior to the delta-sigma modulator. The interpolation rate is controlled by the DSP software. The interpolation filter produces images which are attenuated by at least 56 dB from 0.584 Fs to 128 Fs (192 Fs). After interpolation, the audio data is sent to a third order delta-sigma modulator. The modulator output data stream is converted to an analog signal by a 1 bit DAC and then reconstructed by a switched capacitor filter and continuous time filters. The out-of-band quantization noise from the delta-sigma modulator extends from 0.417 Fs to 128 Fs (192 Fs). Out-of-band noise is further attenuated by the switched capacitor filter and the continuous time filters. The DAC's total quantization noise and thermal noise integrated over a 0.417 Fs to 128 Fs (192 Fs) bandwidth is more than 50 dB below full scale power.

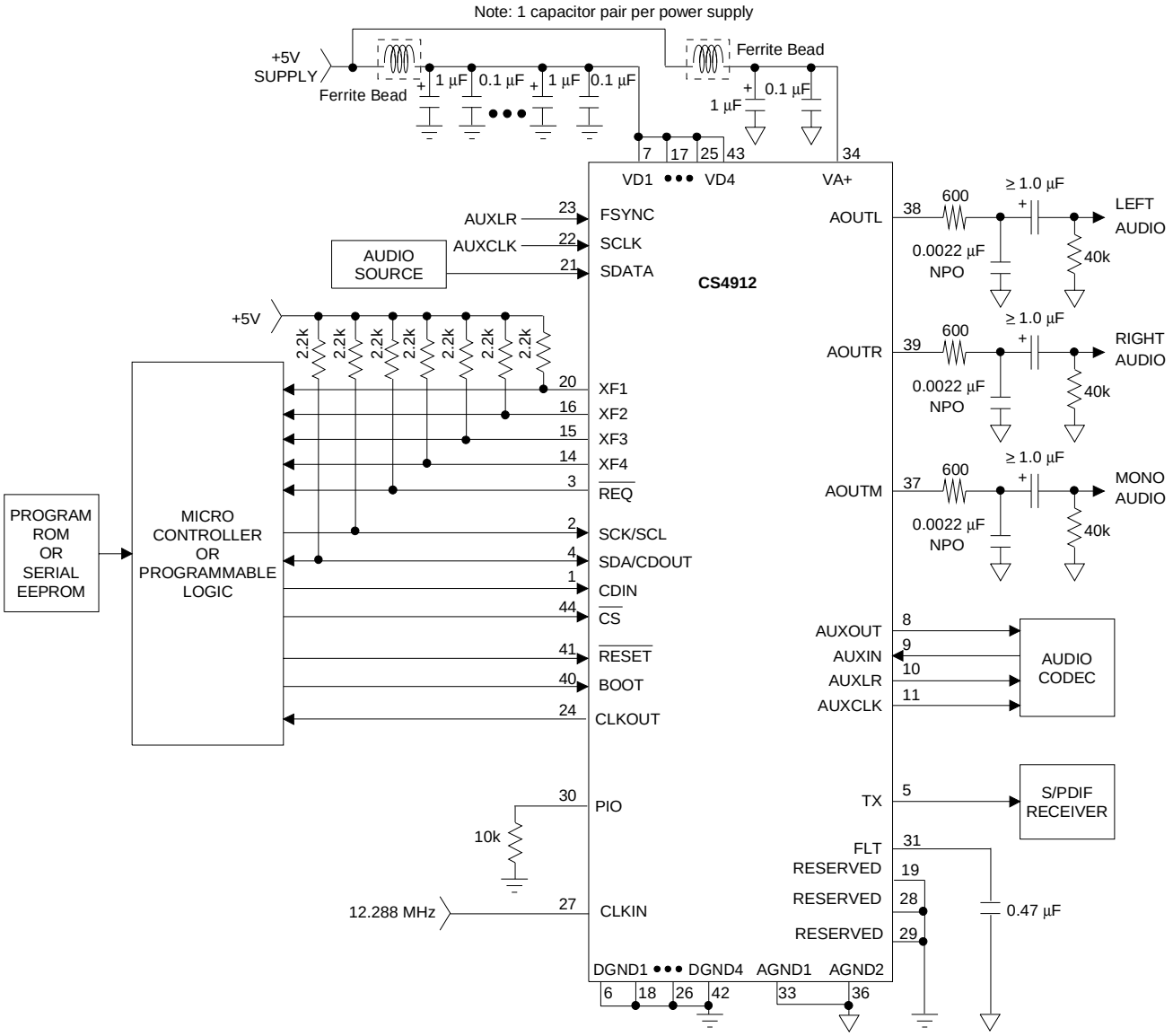


Figure 6. Typical Connection Diagram

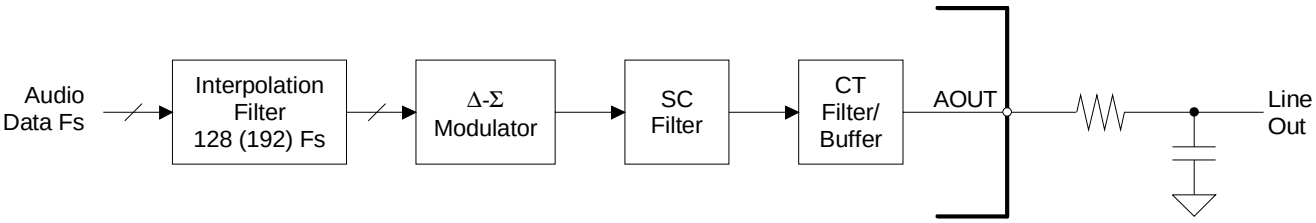


Figure 7. DAC block diagram

An external passive lowpass filter with a single pole at F_c = 5 Fs should be connected to the AOUT pins to further reduce out-of-band noise. The analog outputs are single ended with a drive capability down to 8 kΩ. For more information on delta-sigma DAC architecture, please see Crystal application note AN10, "18-bit Stereo D/A Converter with Integrated Digital and Analog Filters"

Auxiliary Digital Audio Port

The auxiliary (AUX) port provides a full duplex path for the internal DSP core to directly read and write framed PCM digital audio data. The AUX port is typically connected to ADC, DAC, or CODEC devices.

The AUX port is implemented with four device pins; AUXCLK, AUXIN, AUXOUT and AUXLR. AUXCLK is an output pin utilized as the primary synchronous clock. AUXIN is the serial audio data input pin and AUXOUT is the serial audio data output pin. AUXLR is an output pin used for framing the digital audio data, and cycles at the same rate as the on-chip stereo DAC sample rate. The level of AUXLR indicates the current data channel for AUXOUT and AUXIN.

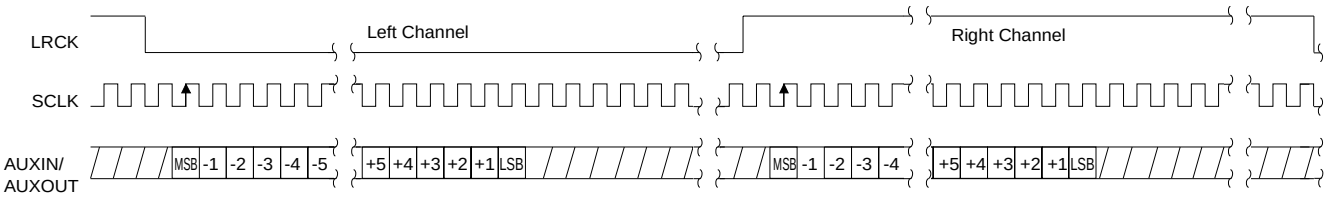
The AUX port has the capability to support multiple digital audio formats, illustrated in Figures 8 through 10. For all modes, AUXLR and AUXOUT transition with the falling edge of AUXCLK. The rising edge of AUXCLK samples AUXIN.

Asynchronous Serial Input Port

The asynchronous serial input (ASI) port is designed to receive compressed serial audio data in audio decoding applications. Typical CS4912 applications use the AUX port for synchronous serial audio data input. However, the ASI port can be synchronized with the AUX port to provide an additional 2 channels of serial audio data input.

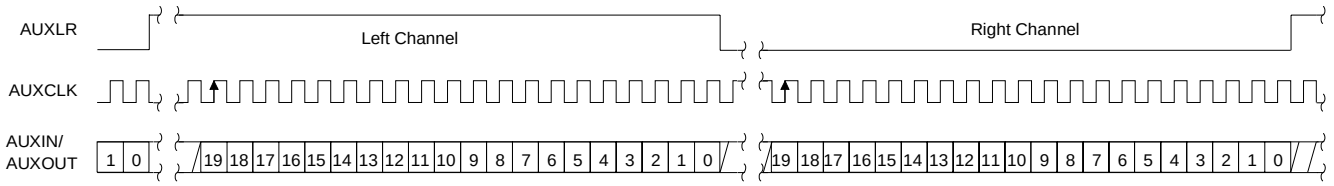
The ASI port is implemented with 3 device pins: SCLK, SDATA, and FSYNC. SCLK clocks the SDATA input into an internal 24 bit shift register. The active edge of SCLK is programmable (EDG), and data is shifted in MSB first. The contents of the shift register are loaded into the ASI input register either by transitions on FSYNC or by a bit counter time out. A DSP interrupt can be generated when the ASI input register is loaded.

FSYNC can clock shift register data into the ASI register on one or both edges. In dual edge mode (PUL = 0), the level of FSYNC indicates left and right channels of stereo audio data. The channel polarity of FSYNC is programmable (POL). The input shift register is clocked on the first 24 SCLK cycles after an FSYNC edge. Additional SCLK



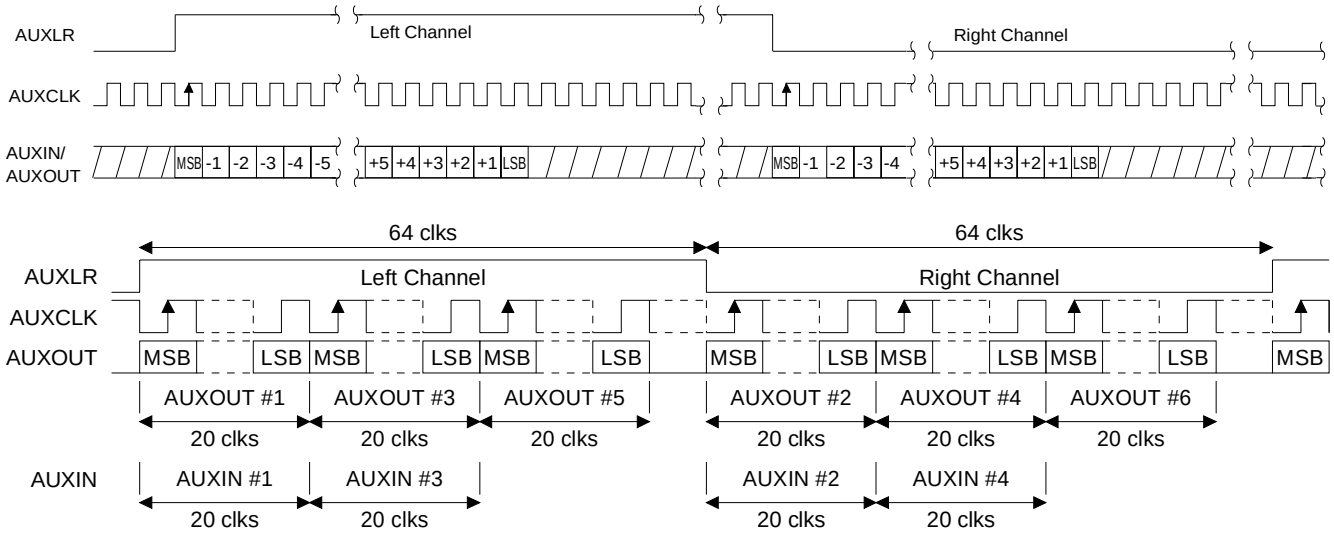
Number of Channels		SCLK Rate	Bit/Sample
Input	Output		
2	2	64 Fs	18
Undefined	2	128 Fs	18

Figure 8. I^2S Formats



Number of Channels		SCLK Rate	Bit/Sample
Input	Output		
Undefined	2	32 Fs	16
Undefined	2	64 Fs	16 or 18
Undefined	2	128 Fs	18

Figure 9. Right Justified Formats



Number of Channels		SCLK Rate	Bit/Sample
Input	Output		
2	Undefined	64 Fs	18
4	6	128 Fs	20

Figure 10. Left Justified Formats

transitions are ignored until the next transition of FSYNC transfers the data to the ASI register and a DSP interrupt is generated.

In single edge (pulse) mode, the data length is programmable to either 16 or 24 bits, and the active edge of FSYNC used to load the ASI register is programmable (POL). The input shift register is loaded into the ASI register when an FSYNC transition occurs, or when the internal bit counter reaches 16 (24). Transitions on FSYNC clear the bit counter. FSYNC can be toggled once to synchronize the bit counter with the incoming data stream, or on each word boundary. The ASI input register will be continuously loaded every 16 (24) SCLK periods. A programmable delay (DEL) can be added to shift the timing between FSYNC and SDATA by one period. Figure 11 shows the timing for the various ASI formats.

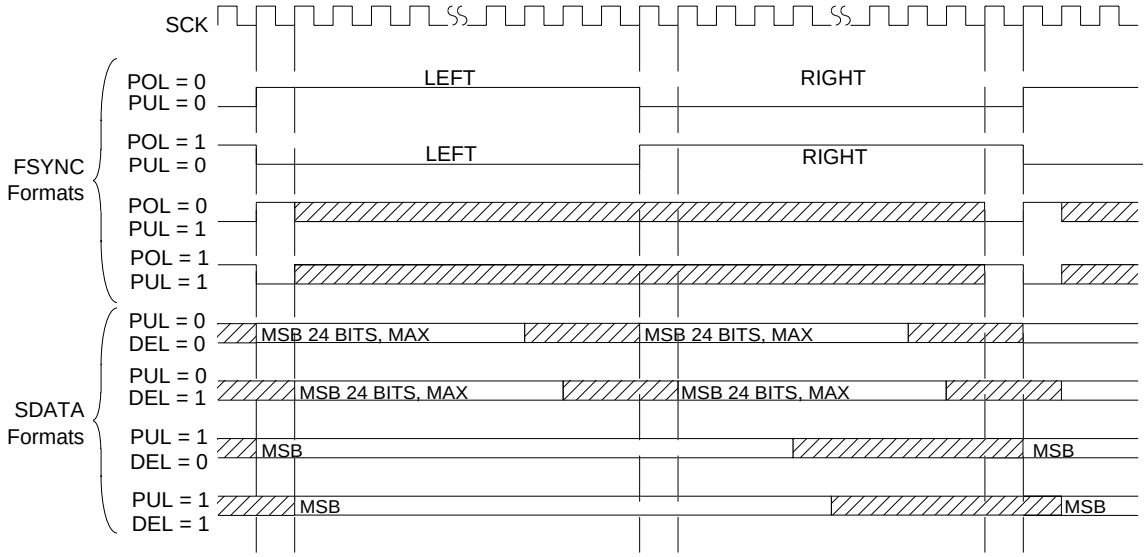


Figure 11. Asynchronous Serial Input Formats

Clock Generator

The clock generator is a phase-locked loop (PLL) based clock multiplier circuit that takes a reference clock input (CLKIN) and produces an internal master clock that has a fixed (but programmable) phase and frequency relationship to the reference. The PLL is configured to produce the appropriate internal master clock for a desired sample rate. All clocks required for the internal peripherals are derived from this master clock.

The PLL requires an external capacitor which is connected to the FLT pin. The typical value of the FLT capacitor is 0.47 µF, which is sufficient for all allowable CLKIN input frequencies. For optimum analog performance, the capacitor must be as close as possible to the FLT pin and layout precautions taken to avoid noise coupling onto the FLT pin.

The clock generator is physically implemented with 2 device pins; CLKIN, and CLKOUT. The CLKIN input pin is used as the reference clock input to the PLL. The CLKOUT output frequency is derived from the DSP clock, and can be used to synchronize external devices. A diagram of the CLKOUT circuit is shown in Figure 12. The value of Q (10 bit) is set by the DSP software.

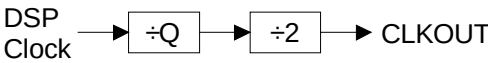


Figure 12. CLKOUT Circuit

Digital Audio Transmitter

The on-chip transmitter encodes digital audio data according to the Sony/Philips Digital Interface Format (S/PDIF). The bi-phase mark encoded data is output on the TX pin MSB first. The TX pin is typically connected to an optical transmitter, or an RS422 transmitter for driving 75 Ω transformer coupled outputs. For more information on S/PDIF, please refer to Crystal application note AN22, "Overview of Digital Audio Interface Data Structures".

Software Configurable Pins

The CS4912 has five pins which can be configured by software for various input/output uses. These pins are the XF1-XF4 pins and the PIO pin. The XF1-XF4 pins are general purpose open-drain output pins. An external pull-up resistor (2.2 kΩ typical) to the digital supply on each XF pin is required for proper operation.

The PIO pin is bidirectional and is capable of generating a DSP interrupt. A pull-down resistor

(10 kΩ typical) to digital ground is required for proper operation.

Serial Control Port

The serial control port (SCP) is an asynchronous serial interface which provides interrupt and handshaking signals between the DSP and an off-chip serial bus master device. The SCP is physically implemented with 5 device pins; SCK/SCL, $\overline{CS}$, SDA/CDOUT, CDIN, and $\overline{REQ}$. The SCP can operate in either I^2C or SPI compatible slave modes. As a slave, the SCP cannot drive the clock signal.

Fast/Slow Mode

Following power-up or reset, the SCP operates in fast mode. Slow mode (programmed in the DSP software) is provided for compatibility with bus masters that can only receive data on the falling edge of SCK/SCL. Slow mode adds additional skew to the output data to provide hold time for these bus masters. In fast mode, the port can be operated at much higher bit rates to facilitate faster downloading of the DSP code. Since the CS4912 is always a slave, fast mode will not affect operation of other devices sharing the same communication bus.

I^2C Mode

For normal I^2C operation, SCK/SCL, SDA, and $\overline{REQ}$ are used; $\overline{CS}$ and CDIN are typically connected to the digital supply. SCK/SCL is the serial clock input which is always driven by an external device. SDA is the bidirectional data pin which requires a pull-up resistor (2.2 kΩ typical) to the digital supply. $\overline{REQ}$ is the active low service request signal, which is driven low when the DSP writes data to the SCP output register. The status of $\overline{CS}$ sets the mode of the SCP during a reset condition. If $\overline{CS}$ is high during a low to high transition on $\overline{RESET}$, the SCP mode is I^2C. It is important to note that $\overline{CS}$ should be high when any reset is issued to ensure the mode remains I^2C.

As an I^2C compatible port, bidirectional data is communicated on the SDA pin MSB first. Input data is sampled on the rising edge of SCK/SCL, and output data transitions after the falling edge of SCK/SCL. During data transmission, SDA should only transition when SCK/SCL is low. Transitions on SDA while SCK/SCL is high are interpreted by the CS4912 as start or stop conditions. A high to low transition on SDA while SCK/SCL is high is a start condition. A low to high transition on SDA while SCK/SCL is high is a stop condition. SCK/SCL should be held low when inactive.

In an I^2C system, each slave device is assigned a unique address. The LSB of the address byte is the read/write bit. When the read/write bit is high, the bus master is reading data from the slave, and low if the bus master is writing data to the slave. The Philips I^2C bus specification provides details of this interface.

Address Checking

Immediately following power up, the CS4912 will respond to any address on the I^2C bus. The SCP can be configured to only respond to an assigned address by initializing an address and enabling address checking via the DSP software. If the CS4912 is the only device other than the bus master on the I^2C bus, address checking is optional. In systems with multiple slave devices on the I^2C bus, the CS4912 should be held in reset until the master is ready to boot the CS4912 with a unique address assignment and enable address checking. The assigned address should be used while downloading DSP code to the CS4912 to avoid conflict with other devices on the bus.

I^2C Write

The flow diagram for a typical I^2C write sequence is shown in Figure 13. Figure 14 shows the relative timing of an I^2C write sequence. A write is initiated with a start condition followed by the address byte with the read/write bit cleared (low). After

each byte, the bus master must release the data line on the falling edge of SCK/SCL on the D0 bit so the CS4912 can drive SDA low during the ninth clock to acknowledge the byte has been received. The SCP will release SDA on the falling edge of the ninth clock. The CS4912 will respond with an ACK following the address byte if address checking is disabled, or if address checking is enabled and the received address is valid. After receiving a valid ACK, the bus master then sends a byte of data. The CS4912 will respond with an ACK after each byte received. To terminate the transaction, the bus master issues a stop condition after the last ACK. If no ACK is received by the bus master, a stop condition should be issued and the transaction restarted. ACK failures on address bytes are an indication of fundamental communications problems at the system level and should be resolved. ACK failures on data bytes can occur if the DSP has not read the previous byte out of the SCP input register before the falling edge of SCK/SCL for the D0 bit.

I²C Read

A flow diagram for a typical I²C read is shown in Figure 15. Figure 16 shows the relative timing diagram of an I²C read. If the DSP needs to send data to an I²C bus master, it writes a data byte to the SCP output register which causes $\overline{\text{REQ}}$ to be asserted low. The bus master must respond by reading the data in the SCP before any subsequent write operations, or the data in the SCP will be lost.

To read from the SCP, the bus master sends a start condition followed by the CS4912 address with the read/write bit set (high). After the address byte is sent, the bus master must release SDA on the falling edge of SCK/SCL on the D0 bit so the CS4912 can drive SDA low during the ninth clock to acknowledge the byte has been received. The CS4912 will respond with an ACK following the address byte if address checking is disabled, or if address checking is enabled and the received address is valid. If no ACK is received by the bus master after the address byte is sent, a stop condition should be issued and the transaction restarted.

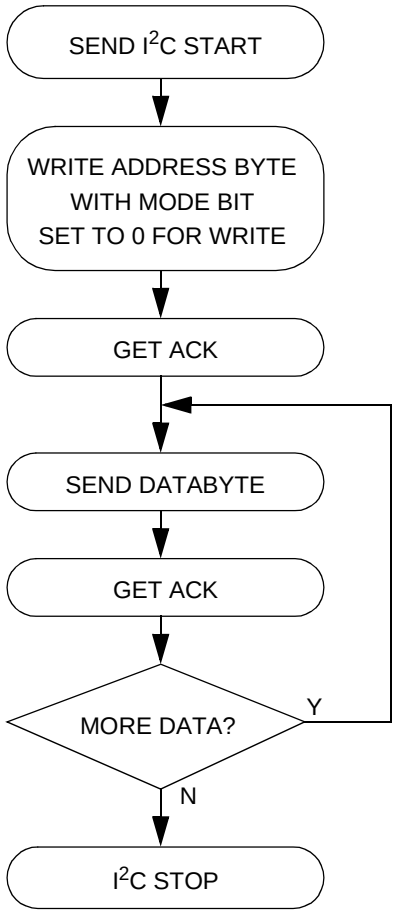


Figure 13. I²C Write Flow Diagram

After sending an ACK for the address byte, the SCP will then clock the contents of the SCP output register into the shift register on the falling edge of the ninth clock and the MSB will be driven onto SDA. After receiving the ACK for the address byte

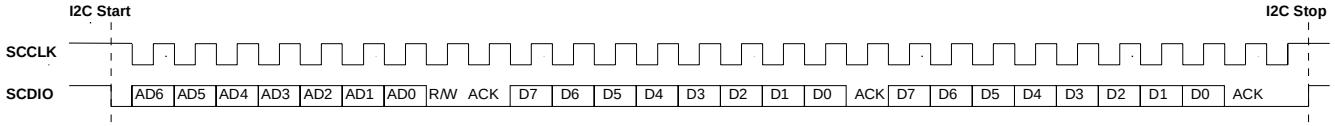


Figure 14. I²C Write Functional Timing Diagram

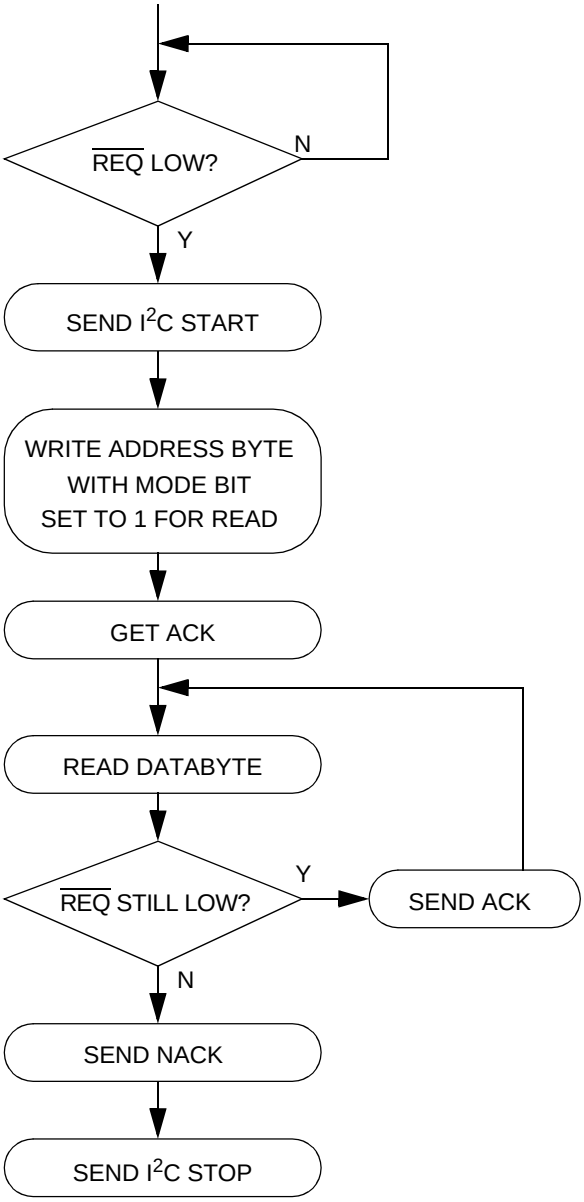


Figure 15. I²C Read Flow Diagram

on the ninth clock, the bus master then clocks 8 bits of data out of the SCP shift register and responds with an ACK after each byte. The bus master must respond with an ACK to each byte received by driving SDA low during the rising edge of the ninth clock cycle. Failure to send an ACK prevents data residing in the SCP output register from being clocked into the SCP shift register.

The behavior of the $\overline{REQ}$ line is dependent on when data is written to the SCP output register in relation to SCK/SCL. There are three cases of $\overline{REQ}$ behavior:

1) The $\overline{REQ}$ line will be de-asserted immediately following the rising edge of SCK/SCL on the D0 bit of the current byte being transferred if there is no data in the SCP output register. The $\overline{REQ}$ line is guaranteed to stay de-asserted (high) until the rising edge of SCK/SCL for the ACK. This signals the host that the transfer is complete and a stop condition should be issued.

2) If data is written to the SCP output register prior to the rising edge of SCK/SCL for the D0 bit, $\overline{REQ}$ will remain asserted (low). Immediately following the falling edge of SCK/SCL for the ACK, the new data byte will be loaded into the serial shift register. The bus master should continue to shift out this new byte.

3) If data is placed in the SCP output register by the DSP between the rising edge of SCK/SCL for the D0 bit, but before the rising edge of SCK/SCL for the ACK, $\overline{REQ}$ will be de-assert-

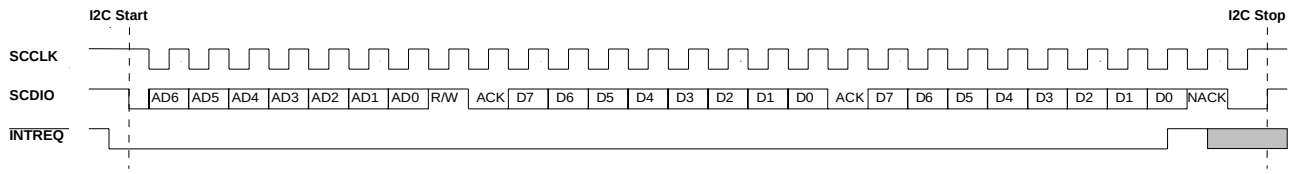


Figure 16. I²C Read Functional Timing Diagram

ed (high) after the rising edge of SCK/SCL for the last data bit, and will not be asserted again until after the rising edge of SCK/SCL for the ACK. Under these conditions, the data in the SCP output register will not be clocked into the shift register on the falling edge of SCK/SCL for the ACK. A new read transaction is required to read this data. The bus master should issue a stop condition before reading the data.

To determine if a read transaction has been completed, the bus master should sample the state of $\overline{\text{REQ}}$ on the falling edge of the last data bit of each byte, or send a stop condition following any rising edge of $\overline{\text{REQ}}$.

Rise Time on SCK/SCL

The Philips I^2C bus specification allows for rise times of the SCK/SCL line up to 1 µs. The CS4912 does not meet this specification. If the I^2C bus master has a rise time in excess of 50 ns the CS4912 will be unable to reliably communicate across the bus. In cases where the CS4912 will be used in a system where a longer rise time on SCK/SCL is expected, a CMOS compatible buffer should be used. Figure 17 shows the necessary connections. Note the buffer is only used for the SCK/SCL connection to the CS4912.

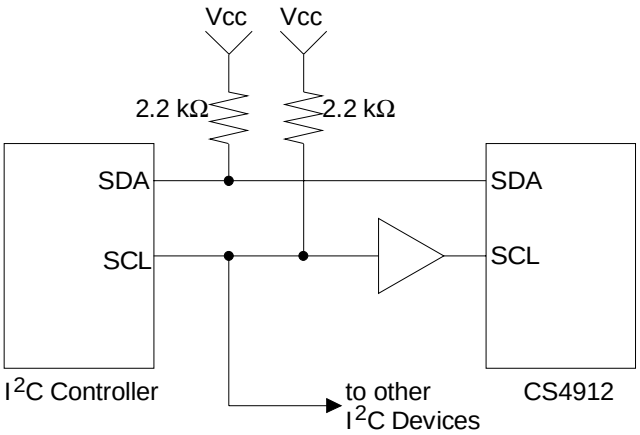


Figure 17. I^2C Connection Diagram

SPI Mode

For normal SPI operation, SCK/SCL, $\overline{\text{CS}}$, CDIN, CDOUT and $\overline{\text{REQ}}$ are used. SCK/SCL is the serial clock input which is always driven by an external device. $\overline{\text{CS}}$ is the active low enable signal. CDIN is the control data input. SDA/CDOUT is the SCP data output. $\overline{\text{REQ}}$ is the active low request signal, which is asserted low when there is data in the SCP output register. The status of $\overline{\text{CS}}$ sets the mode of the SCP during a reset condition. If $\overline{\text{CS}}$ is low during a low to high transition of $\overline{\text{RESET}}$, the SCP mode is SPI. It is important to note that $\overline{\text{CS}}$ should be low when any reset is issued to ensure the mode remains SPI.

As an SPI compatible port, data on CDIN is clocked into the SCP on the rising edge of SCK/SCL. Data is output MSB first onto CDOUT and transitions on the falling edge of SCK/SDA.

SPI Write

An SPI write is initiated by asserting $\overline{\text{CS}}$ low. The bus master then sends the SCP address byte with the read/write bit cleared (low). A data byte is then clocked into the SCP on the CDIN pin. The data byte is transferred to the SCP input register on the falling edge of the D0 bit and a DSP interrupt is generated. Multiple bytes can be clocked into the SCP while is $\overline{\text{CS}}$ asserted. $\overline{\text{CS}}$ is de-asserted (high) following the falling edge of SCK/SCL for the D0 bit of the last byte.

Figure 18 shows the sequence for an SPI write transaction.

Figure 19 shows the relative timing diagram of an SPI write transaction. A ‘write’ is defined as the transfer of data from an SPI bus master to the CS4912 serial control port via CDIN. A read transfers data from the SCP to the bus master via CDOUT. A bus transaction is initiated when $\overline{\text{CS}}$ is asserted low by the bus master. The SCP address byte is then sent to the CS4912. The LSB of the address is the read/write bit that is set (high) if the bus

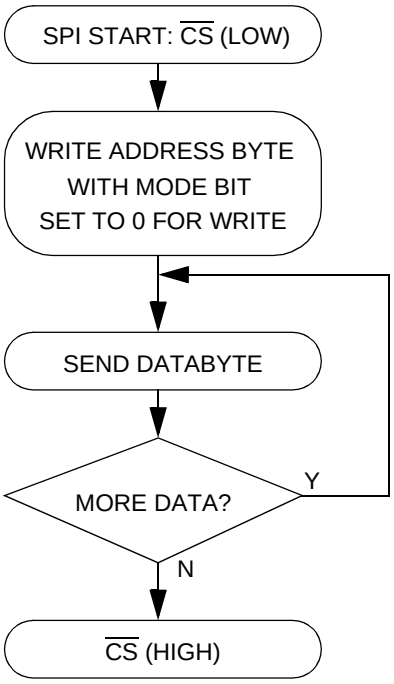


Figure 18. SPI Write Flow Diagram

master is reading data from the slave and cleared (low) if the bus master is writing data to the slave. Although not typical in SPI systems, address checking can be used as described in the I^2C section.

SPI Read

If the DSP is required to send data to an SPI bus master, it writes the data byte to the SCP output register which causes REQ to be asserted low. The bus master must respond by reading the data in the SCP before any subsequent write operations, or the data in the SCP will be lost.

To read from the SCP in SPI mode, the bus master asserts CS (low) and sends the CS4912 address byte to the SCP via CDIN with the read/write bit set (high). The SCP will then load the contents of the SCP output register into the shift register on the falling edge of SCK/SCL for the D0 bit of the address byte and the MSB of the data byte will be driven onto CDOUT. The bus master then reads the contents of the SCP shift register.

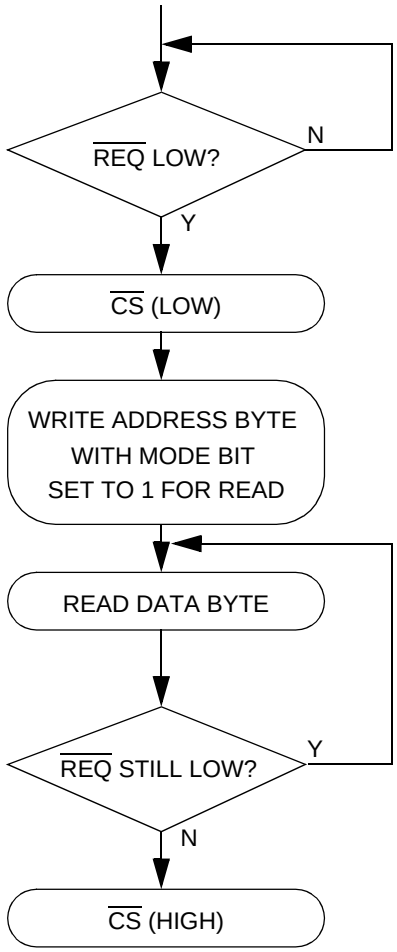


Figure 20. SPI Read Flow Diagram

The behavior of the REQ line is dependent on when data is written to the SCP output register in relation to SCK/SCL. There are three cases of REQ behavior:

1) The REQ line will be de-asserted immediately following the rising edge of the D1 data bit of the current byte being transferred if there is no

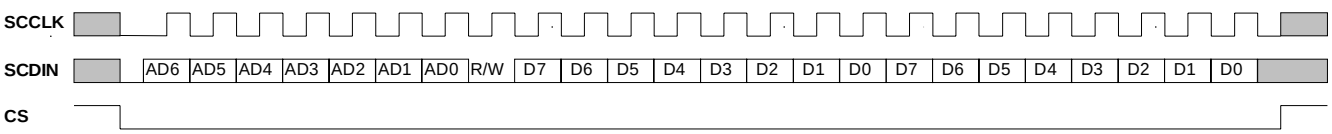


Figure 19. SPI Write Functional Timing Diagram

data in the SCP output register. This indicates to the bus master that the transfer is complete and $\overline{CS}$ should be de-asserted (high). The $\overline{REQ}$ line is guaranteed to stay de-asserted (high) until after the rising edge of SCK/SCL for the D0 bit.

2) If data is written to the SCP output register prior to the rising edge of SCK/SCL for the D1 data bit, $\overline{REQ}$ will remain asserted (low). The new data byte will be loaded into the serial shift register on the falling edge of SCK/SCL for the D0 bit. The bus master should continue to shift out this new byte.

3) If data is placed in the SCP output register by the DSP between the rising edge of SCK/SCL for the D1 data bit, but before the rising edge of SCK/SCL for the D0 data bit, $\overline{REQ}$ will be de-asserted (high) after the rising edge of SCK/SCL for the D1 bit, and will not be asserted again until after the rising edge of SCK/SCL for the D0 bit. Under these conditions, the data in the SCP output register will not be clocked into the shift register on the falling edge of SCK/SCL for the D0 bit. A new read transaction is required to read this data, and the bus master should de-assert $\overline{CS}$ after the falling edge of SCK/SCL for the D0 bit.

To determine if a read transaction has been completed, the bus master should sample the state of $\overline{REQ}$ on the falling edge of the D1 data bit of each byte, or de-assert $\overline{CS}$ following any rising edge of $\overline{REQ}$ after the falling edge of SCK/SCL for the D0 bit.

RESET

The CS4912 provides three reset mechanisms, software reset, hardware reset, and boot reset. Software reset is initiated by the DSP software. On software reset, the digital audio transmitter, the serial control port, and the ALTCLK pin are disabled. The stereo DAC is also muted. All interrupts except the debug interrupt are disabled, all internal registers are cleared, control port address checking is disabled, and software execution is restarted. Internal RAM is not cleared. Normal operation is resumed one internal clock cycle after the rising edge of $\overline{RESET}$.

Hardware reset is initiated by holding the BOOT pin low while the $\overline{RESET}$ pin transitions from low to high. Hardware reset has the same effect as software reset.

Boot reset is initiated by holding the BOOT pin high while the $\overline{RESET}$ pin transitions from low to high. On boot reset, the DACs are muted, the internal registers are cleared, all interrupts except debug are disabled, and the DSP begins execution at the beginning of the internal ROM program. The behavior of the boot ROM program is described in the following section. During power up, boot reset conditions must be met in order to load a program into the DSP.

BOOT PROCEDURE

The boot ROM code transfers data through the SCP to on-chip program and data RAM. After the memory has been loaded, the boot loader program issues a software reset and the new program loaded into RAM begins execution.

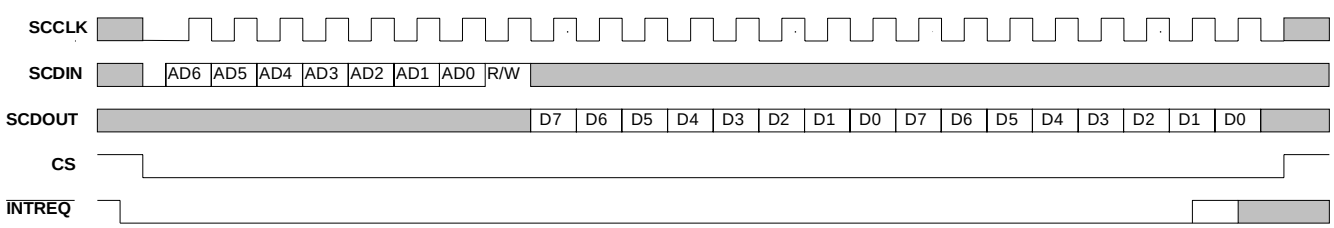


Figure 21. SPI Read Functional Timing Diagram

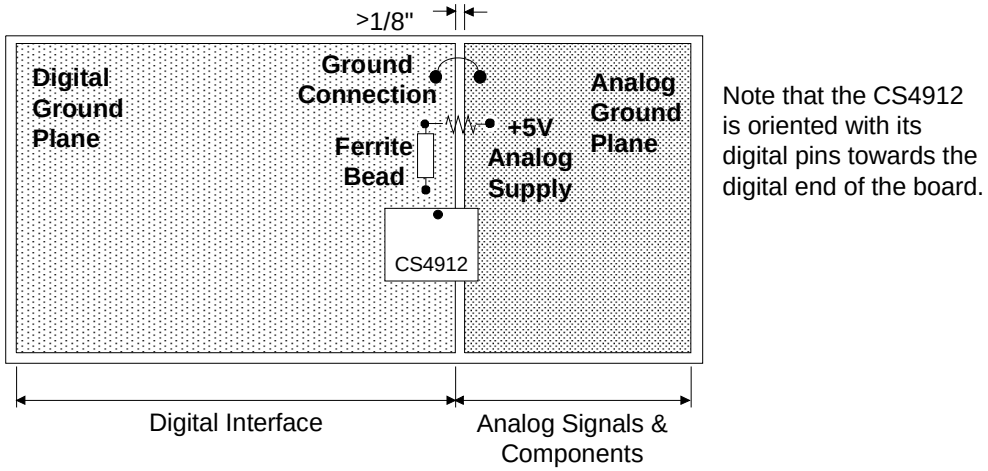


Figure 22. CS4912 Suggested Layout

The boot ROM loads blocks of data into consecutive RAM addresses. The block data format consists of a two byte block start address that contains a data or program RAM identifier, and a two byte data block length. The start address is contained in the 12 LSBs of the start address. The 13th bit of the start address is the data/program RAM identifier. A one in this position indicates a program RAM destination. The upper three bits of the start address are discarded internally. Any number of blocks can be loaded sequentially during boot. A two byte end-of-block identifier (0xFFFF), and a three byte check sum must follow the last data block. The check sum is generated by summing all the previous data, address, and length bytes and truncating to 24 bits. The check sum received by the control port is compared to the value calculated internally. If they do not match, the DSP writes the internally calculated check sum to the SCP output register, and the processor enters an infinite loop. The check sum written to the SCP output register causes $\overline{\text{REQ}}$ to be asserted low, which is a key indicator to the bus master that the boot process was unsuccessful. The SCP shift register is still functional with the DSP in a loop, and the check sum data is available to be read by the bus master.

POWER SUPPLY AND GROUNDING

To minimize noise and optimize system performance, a multilayer board with power and ground planes should be used. The digital and analog power and grounds should be separated on their respective plane layer. All digital circuitry and traces should lie over the digital ground plane, and the digital power and ground planes should not overlap the analog power or ground plane.

To minimize noise on the power bus, digital power should be connected to the CS4912 via a ferrite bead, positioned closer than 1" to the device (see Figure 22). The CS4912 VA+ pin should be derived from the cleanest power source available. If only one supply is available, use the suggested arrangement in Figure 6.

The CS4912 should be positioned such that the analog pins (pins 29-39) are over the analog ground plane, while the rest of the pins lay over the digital ground plane as illustrated in Figures 22 and 23. The analog and digital grounds on the CS4912 are not connected internally; the system designer is required to connect them externally through a point-to-point connection across the ground split as shown in Figure 22. Figure 23 illustrates the optimum ground and decoupling layout for the CS4912 assuming a surface-mount socket and surface mount decoupling capacitors. If the part is to be

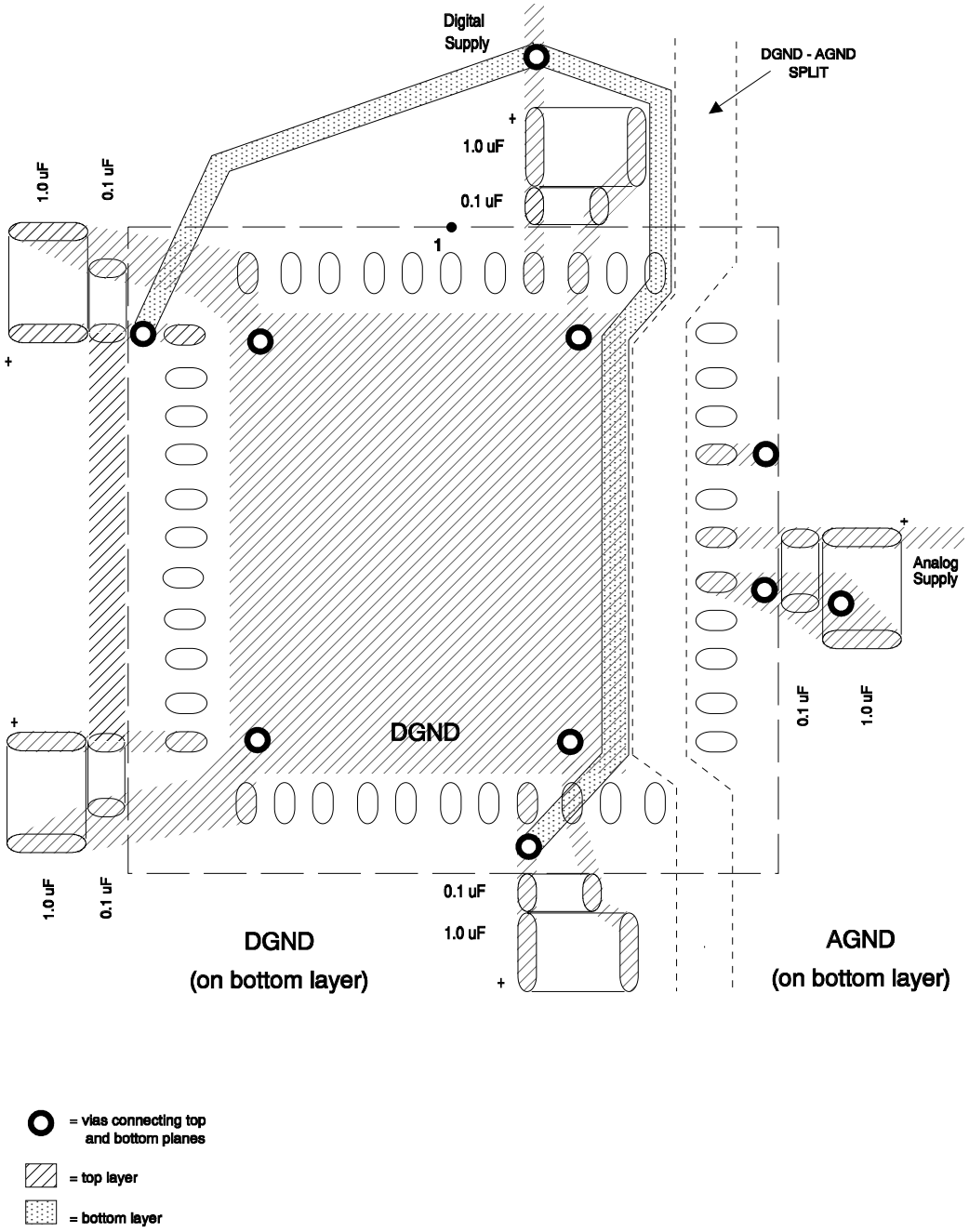


Figure 23. CS4912 Surface Mount Decoupling Layout

socketed, find a socket with the minimum height which will minimize the socket impedance. Decoupling capacitors are placed as close as possible to the device which, in this case, is the socket boundary. Traces bringing the power to the CS4912 should be wide thereby keeping the impedance low.

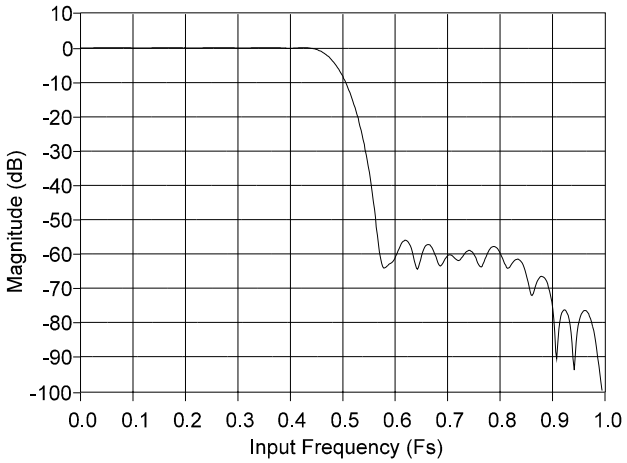


Figure 24. DAC Frequency Response

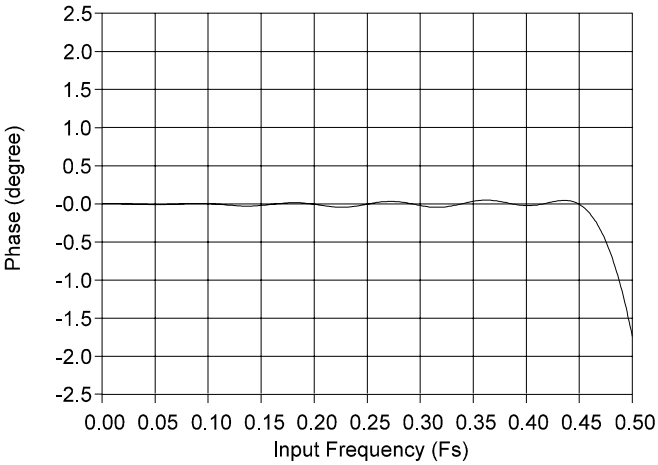


Figure 25. DAC Phase Response

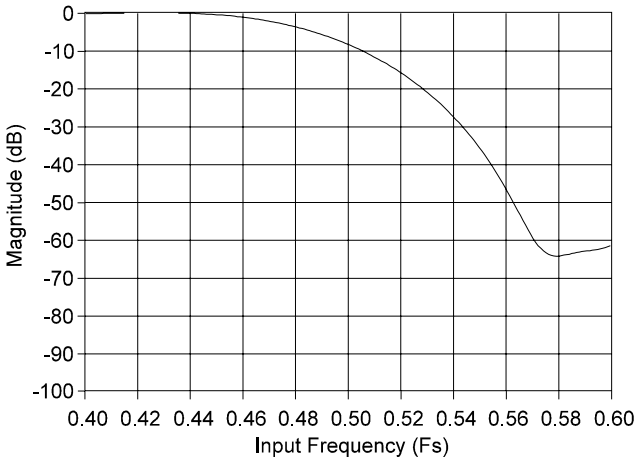


Figure 26. DAC Transition Band

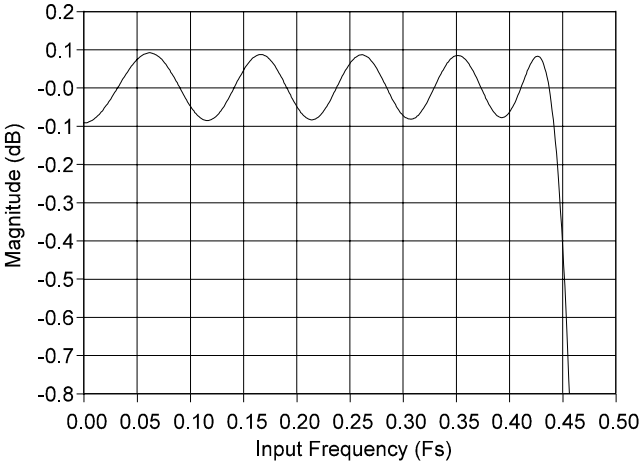
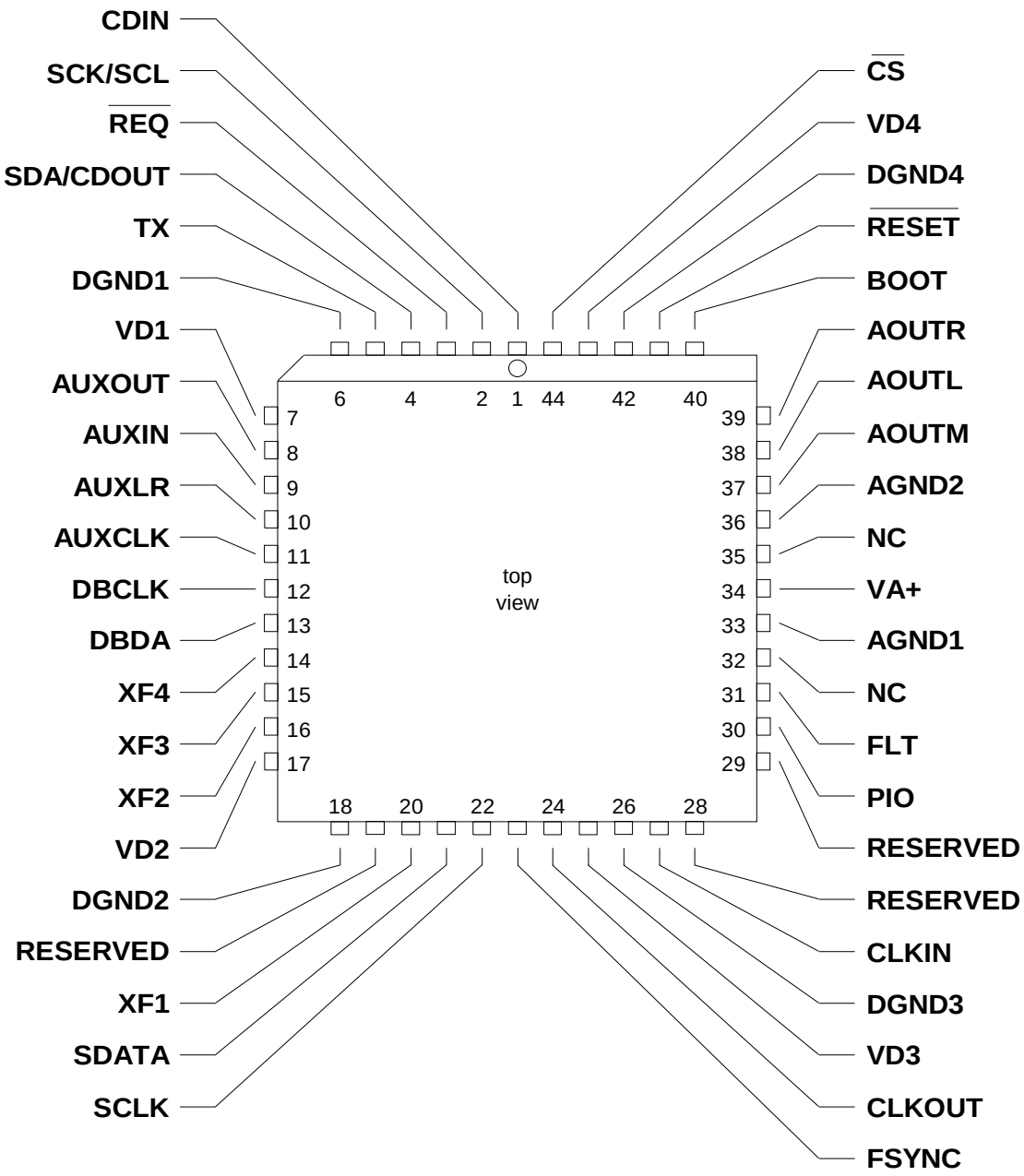


Figure 27. DAC Passband Ripple

PIN DESCRIPTIONS



Power Supplies

VD1, VD2, VD3, VD4 - Positive Digital Power Supply, PINS 7, 17, 25, 43.

The +5 V supply connected to these pins powers the various digital subcircuits on the chip. See the Power Supply and Grounding section in this data sheet for decoupling recommendations.

DGND1, DGND2, DGND3, DGND4 - Digital Ground, PINS 6, 18, 26, 42.

Digital power supply ground.

VA+ - Positive Analog Power Supply, PIN 34.

The +5 V supply connected to these pins powers the DACs and the PLL. Analog performance is highly dependent on the quality of this supply. See the Power Supply and Decoupling section in this data sheet for decoupling recommendations.

AGND1, AGND2 - Analog Ground, PIN 33, 36.

Analog power supply ground.

Digital-to-Analog Converter

AOUTL, AOUTR - Analog Outputs, Left and Right Channels, PINS 38, 39.

The DAC outputs are centered at approximately 2.2 V. An external filter is required to diminish out-of-band noise. See Typical Connection Diagram, Figure 6.

AOUTM - Mono Analog Output, PIN 37.

Mono is the summation of AOUTL and AOUTR. Mono output is 180° out-of-phase with the sum of AOUTL and AOUTR. Mono is centered at approximately 2.2 V. An external filter is required to diminish out-of-band noise. See Typical Connection Diagram, Figure 6.

Digital Audio Transmitter

TX - Transmitter Output, PIN 5.

Biphase mark encoded data is output at logic levels from the TX pin. TX typically connects to the input of an RS-422 or optical transmitter. With additional external circuitry, the port can support either AES/EBU or S/PDIF formats.

Clock Generator

CLKOUT - Clock Output, PIN 24.

CLKOUT is typically used as the master clock input (MCLK) to synchronize external audio converters such as ADCs, DACs or CODECs. CLKOUT can also be used to synchronize digital peripherals such as microcontrollers. The output frequency is determined by a programmable divider in the clock generator.

FLT - PLL Filter, PIN 31.

A capacitor (typically 0.47 µF) connected to this pin filters the control voltage for the on-chip PLL. Trace length between the pin and capacitor should be minimized.

CLKIN - Clock Input, PIN 27.

CLKIN is the reference clock input to the PLL.

Control

DBCLK, DBDA - Debug Port, PINS 12, 13.

DBDA is the bidirectional debug port data pin, and requires a pull-up resistor to the digital supply (typically 2.2 kΩ). DBCLK is the debug port clock input.

$\overline{\text{RESET}}$ - PIN 41.

The CS4912 enters a reset state while $\overline{\text{RESET}}$ is low. $\overline{\text{RESET}}$ is typically provided by a power supply monitor IC.

BOOT - PIN 40.

Boot enable pin. If BOOT is high during a low to high transition of $\overline{\text{RESET}}$, the boot ROM program begins execution.

XF1, XF2, XF3, XF4 - External Flags, PINS 20, 16, 15, 14.

The XF pins are software controllable open drain outputs. An external pull-up resistor to the digital supply is required (typically 2.2 kΩ) for proper operation.

PIO - Programmable Input/Output, PIN 30.

The PIO pin is a software controllable bidirectional pin. A pull-down resistor (typically 10 kΩ) to the digital ground is required for proper operation.

RESERVED - PINS 19, 28, 29

These pins must be tied to ground for proper operation.

Serial Control Port

$\overline{\text{REQ}}$ - Request Output, PIN 3.

The $\overline{\text{REQ}}$ pin is asserted low when the control port needs servicing from an external device. A pull-up resistor (typically 2.2 kΩ) to the digital supply is required for proper operation.

$\overline{\text{CS}}$ - Chip Select Input, PIN 44.

In SPI format, communication between the host and the CS4912 is initiated when the host drives the $\overline{\text{CS}}$ pin low. $\overline{\text{CS}}$ also serves as the communication format select during reset or power up. When $\overline{\text{CS}}$ is high during a reset or power up the SCP will be configured in I^2C mode. When low, it is configured in SPI mode.

SCK/SCL - Serial Clock Input, PIN 2.

The SCK/SCL input clocks data into or out of the serial control port.

SDA/CDOUT - Serial Data I/O / Control Data Output, PIN 4.

In SPI mode, CDOUT is a data output for the serial control data. In I^2C interface mode, SDA is the bidirectional data pin. A pull-up resistor (2.2 kΩ typical in I^2C mode) is required for proper operation.

CDIN - Control Data Input, PIN 1.

In SPI mode, CDIN is the data input for the serial control port. It has no function in I^2C mode, and should be tied to digital power or ground.

Auxiliary Digital Audio Port

AUXLR - Auxiliary Sample Clock Output, PIN 10.

AUXLR determines which channel is currently being input on the AUXIN pin or output on the AUXOUT pin. AUXLR is typically connected to the frame clock (LRCLK or FSYNC) on an external ADC or DAC.

AUXIN - Auxiliary Data Input, PIN 9.

Two's complement MSB first serial audio data is input on this pin. The data is clocked by AUXCLK and the channel is indicated by AUXLR. AUXIN is typically connected to the serial audio data output pin (SDOUT) on an external ADC.

AUXOUT - Auxiliary Data Output, PIN 8.

Two's complement MSB first serial audio data is output on this pin. The data is clocked by AUXCLK and the channel is indicated by AUXLR. AUXOUT is typically connected to the serial audio data input (SDIN) on an external DAC.

AUXCLK - Auxiliary Serial Clock Output, PIN 11.

AUXCLK shifts data into the device on the AUXIN pin and shifts data out of the device on the AUXOUT pin. AUXCLK is typically connected to the serial audio data clock (SCLK) on an external ADC or DAC.

Asynchronous Audio Port

FSYNC - Frame Synchronization Clock Input, PIN 23.

FSYNC transitions delineate left and right audio data, or the start of a data frame. Typically used in compressed audio applications.

SCLK - Serial Clock Input, PIN 22.

SCLK is used to clock serial audio data into the device on SDATA. Typically used in compressed audio applications.

SDATA - Serial Audio Data Input, PIN 21.

Audio data input to SDATA is clocked into the device by SCLK. Typically used in compressed audio applications.

PARAMETER DEFINITIONS

Resolution

The number of bits in the audio input word of the DACs.

Differential Nonlinearity

The worst case deviation from the ideal code width; expressed in LSBs.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the RMS sum of all the in-band harmonics of the test signal.

Instantaneous Dynamic Range

The Signal-to-(Noise + Distortion) ratio (S/(N+D)) with a 1 kHz, -60 dB from full scale DAC input signal, with 60 dB added to compensate for the small signal. Use of a small signal reduces the harmonic distortion components of the noise to insignificant levels. Units are in dB.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel with 1 kHz, 0 dB signal present on the other channel. Units are in dB.

Interchannel Gain Mismatch

The difference in output voltages for each channel with a full scale digital input. Units are in dB.

Frequency Response

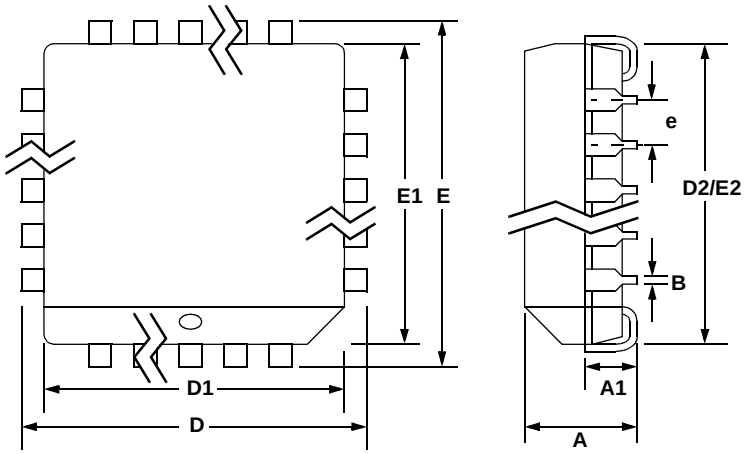
Worst case variation in output signal level versus frequency over 10 Hz to 20 kHz. Units in dB.

Out of Band Energy

The ratio of the RMS sum of the energy from 0.46 Fs to 2.1 Fs compared to the RMS full-scale signal value. Tested with a 48 kHz Fs, giving an out-of-band energy range of 22 kHz to 100 kHz.

PACKAGE DIMENSIONS

44L PLCC PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.165	0.180	4.043	4.572
A1	0.090	0.120	2.205	3.048
B	0.013	0.021	0.319	0.533
D	0.685	0.695	16.783	17.653
D1	0.650	0.656	15.925	16.662
D2	0.590	0.630	14.455	16.002
E	0.685	0.695	16.783	17.653
E1	0.650	0.656	15.925	16.662
E2	0.590	0.630	14.455	16.002
e	0.040	0.060	0.980	1.524

JEDEC # : MS-018

• Notes •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