



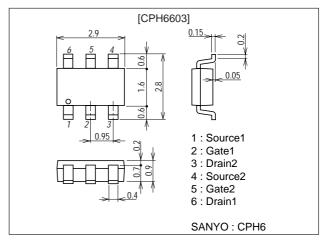
Ultrahigh-Speed Switching Applications

Features

- · Low ON-resistance.
- · Ultrahigh-speed switching.
- 4V drive.

Package Dimensions

unit : mm 2202



Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	VDSS		-30	V
Gate-to-Source Voltage	VGSS		±20	V
Drain Current (DC)	ID		-1.5	Α
Drain Current (Pulse)	IDP	PW≤10μs, duty cycle≤1%	-6.0	А
Allowable Power Dissipation	PD	Mounted on a ceramic board (900mm ² X0.8mm)1unit	0.9	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		-55 to +150	°C

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	Offic
Drain-to-Source Breakdown Voltage	V(BR)DSS	ID=-1mA, VGS=0	-30			V
Zero-Gate Voltage Drain Current	IDSS	V _{DS} =-30V, V _{GS} =0			-1	μΑ
Gate-to-Source Leakage Current	IGSS	V _{GS} =±16V, V _{DS} =0			±10	μΑ
Cutoff Voltage	VGS(off)	V _{DS} =-10V, I _D =-1mA	-1.2		-2.6	V
Forward Transfer Admittance	yfs	V _{DS} =-10V, I _D =-0.8A	1.0	1.5		S
Static Drain-to-Source On-State Resistance	R _{DS} (on)1	I _D =-0.8A, V _G S=-10V		190	250	mΩ
	R _{DS} (on)2	I _D =-0.4A, V _G S=-4V		330	460	mΩ

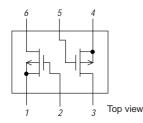
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	Offic
Input Capacitance	Ciss	V _{DS} =-10V, f=1MHz		185		pF
Output Capacitance	Coss	V _{DS} =-10V, f=1MHz		30		pF
Reverse Transfer Capacitance	Crss	V _{DS} =-10V, f=1MHz		20		pF
Turn-ON Delay Time	t _d (on)	See specified Test Circuit.		7		ns
Rise Time	t _r	See specified Test Circuit.		4		ns
Turn-OFF Delay Time	t _d (off)	See specified Test Circuit.		22		ns
Fall Time	tf	See specified Test Circuit.		8		ns
Total Gate Charge	Qg	V _{DS} =-10V, V _{GS} =-10V, I _D =-1.5A		4.7		nC
Gate-to-Source Charge	Qgs	V _{DS} =-10V, V _{GS} =-10V, I _D =-1.5A		0.8		nC
Gate-to-Drain "Miller" Charge	Qgd	V _{DS} =-10V, V _{GS} =-10V, I _D =-1.5A		0.7		nC
Diode Forward Voltage	V _{SD}	I _S =-1.5A, V _G S=0		-0.88	-1.5	V

Electrical Connection

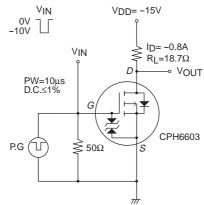


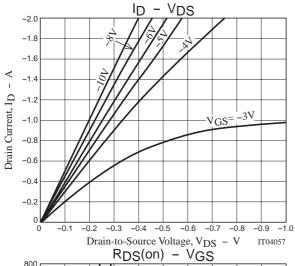
1 : Source1 2 : Gate1

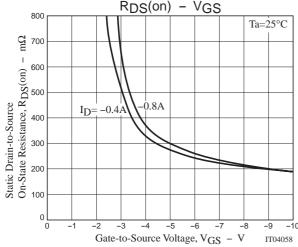
3 : Drain2 4 : Source2

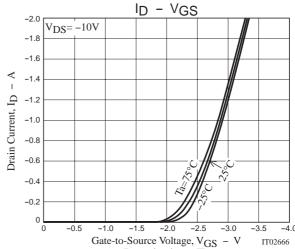
5 : Gate2 6 : Drain1

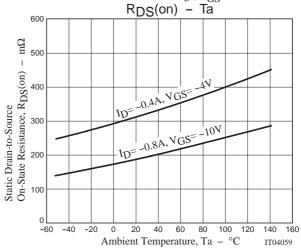
Switching Time Test Circuit

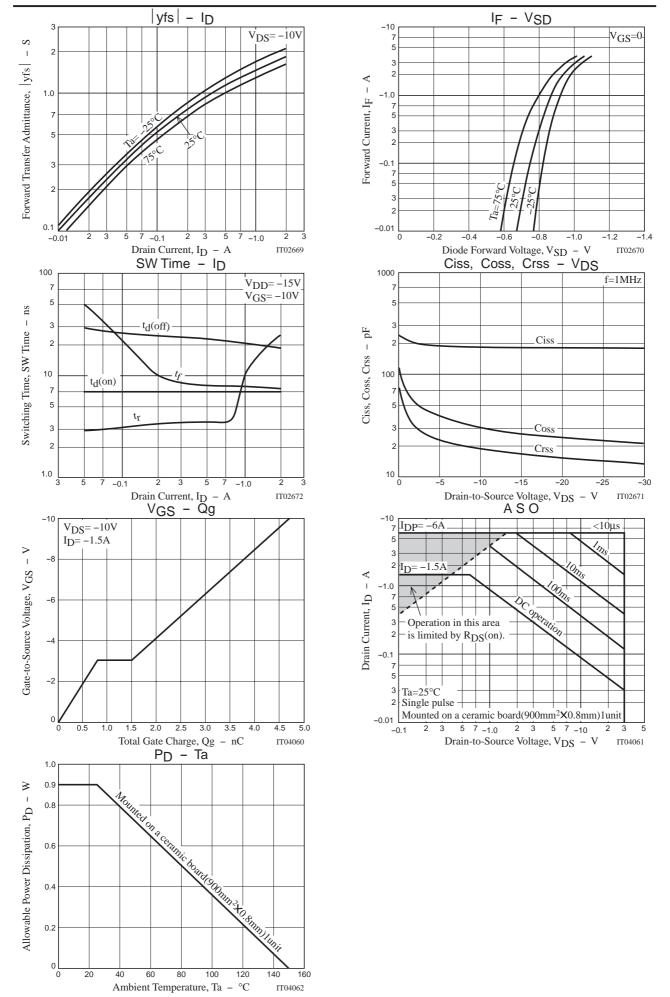












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