CLA80000 SERIES

HIGH DENSITY CMOS GATE ARRAYS

INTRODUCTION

The new CLA80k gate array series from GEC Plessey Semiconductors offers advantages in speed and density over previous array series. The unique architecture allows the efficient implementation of parameterized memory cells. Improvements in design combined with advances in simulation accuracy allow the implementation of complex systems in excess of 260,000 gates.

FEATURES

- 0.7µ (0.8µ drawn) process
- Typical gate delay 210ps
- Accurate simulation delay (multi platform support)
- Support for industry standard workstations
- Comprehensive cell library
- Core cells optimized to implement RAM
- 3V option for low power operation
- Split rail operation (optional 5V I/O, 3V core logic)
- Low skew clock distribution strategy
- Analog phase locked loop (PLL)
- Power and ground distribution grids
- Extensive range of package options

OVERVIEW

The gate array has a comprehensive cell library including RAM and ROM generators as well as JTAG circuits. CLA80k is GEC Plessey Semiconductors' (GPS') seventh generation CMOS gate array product. The family consists of 22 arrays implemented on the latest generation 0.7µ (0.8µ drawn) process. The advanced array architecture in combination with sub micron processing offers a high packaging density of 2000 gates/mm^2 with three layer metal.

GEC Plessey Semiconductors' Design Centres offer support on a variety of design routes customized to individual requirements.

GPS can supply support kits for many major industry ASIC design tools as well as our in-house PDS2 proprietary software. All kits support the advanced delay calculations essential for accurate simulation

Standard Density Pad Arrays are targeted for use in ceramic packaging and for those applications which require assembly in conformance with MIL STD 883

ARRAY SIZES

The CLA80k series comprises 9 base arrays and 22 variants ranging from 2816 to 513,136 array elements. The optimum array for your requirement may be selected from the tables below.

Double Layer Metal Arrays (High Density pads)

Array type	Array elements	Usable gates	PLL	Total Pads
CLA81XXX	2816	1400		64
CLA82XXX	8736	4260		88
CLA83XXX	17920	8400		112
CLA84XXX	30784	13600		136
CLA85XXX	54720	22000	✔	168
CLA86XXX	100048	30000	✔	216
CLA87XXX	157872	48000	✔	264

Triple Layer Metal Arrays (High Density pads)

Array type	Array elements	Usable gates	PLL	Total pads
CLT81XXX	2816	1680		64
CLT82XXX	8736	5200		88
CLT83XXX	17920	10700		112
CLT84XXX	30784	18000		136
CLT85XXX	54720	32500	✔	168
CLT86XXX	100048	58000	✔	216
CLT87XXX	157872	90000	✔	264
CLT88XXX	307568	170000	✔	360
CLT89XXX	513136	260000	✔	456

Standard Density Pad Arrays

Array type	Array elements	Usable gates	PLL	Total pads
MLA85XXX	55440	22000	✔	152
MLA87XXX	158592	48000	✔	232
MLT85XXX	55440	32500	✔	152
MLT87XXX	158592	90000	✔	232
MLT88XXX	312688	170000	✔	312
MLT89XXX	522160	260000	✔	384

ARCHITECTURE

Core cell

- Supports compact SRAM cells
- Allows routing through cells for compact layout

The basic unit from which all library functions are constructed is called an ‘array element’. An array element consists of two P-channel and two N-channel plus a small P-channel transistor that allows the efficient implementation of random access memories (RAM). Two basic cell or array elements are illustrated in Figure 1. To achieve the required circuit function, logic designers utilize a set of cells. Each library component realizes a logic function, ranging in complexity from an inverter to a master-slave ‘D’ flip-flop. A fixed metal interconnection of the transistors from one or more array elements implements the cell function. A design is specified in terms of cells, macros, modules and their interconnections, which are then simulated using PDS or other approved design platforms.

If your design uses only two layers of metal then a set of four masks are required. One for contacts, one for vias (connections between the metal layers) and two for metals. If your design uses three layer metal then six masks are required. One for contacts, two for vias and three for metals.

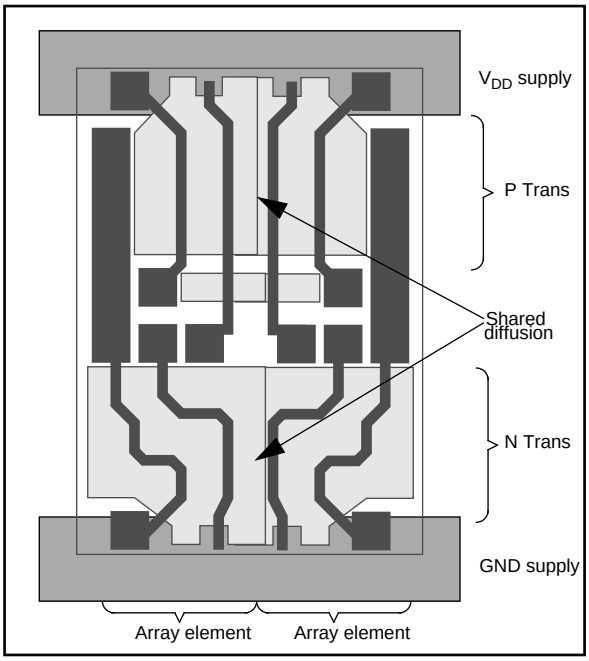

Figure 1 Pair of array elements

I/O ARRANGEMENT

- High density and standard density pads available
- 4KV ESD and latchup immunity
- Programmable slew rate control

Around the outside of the array are I/O blocks and pads placed at the chip periphery. All arrays have wide power bus rings situated over their respective I/O blocks. The partition of the I/O cell is shown in Figure 2. For high density pad arrays three pads are placed every four I/O cells whilst for standard density array pads two pads are placed for every three I/O cells.

Each I/O cell is divided into a number of sections allowing a wide variety of different I/O cells to be constructed. Each I/O block can be customized as an input, output or bi-directional I/O port. In addition any pad location can be utilized as a positive or negative supply pad.

Electrostatic discharge protection (ESD) is built into the I/O cells. This protection can withstand in excess of 4kV. The structure is also highly resistant to latch-up due to the epitaxial substrate used in the process.

Slew rate control is provided within the I/O cell structure to minimizes supply noise transients. This is a useful feature in larger designs where multiple high drive outputs need to be switched simultaneously.

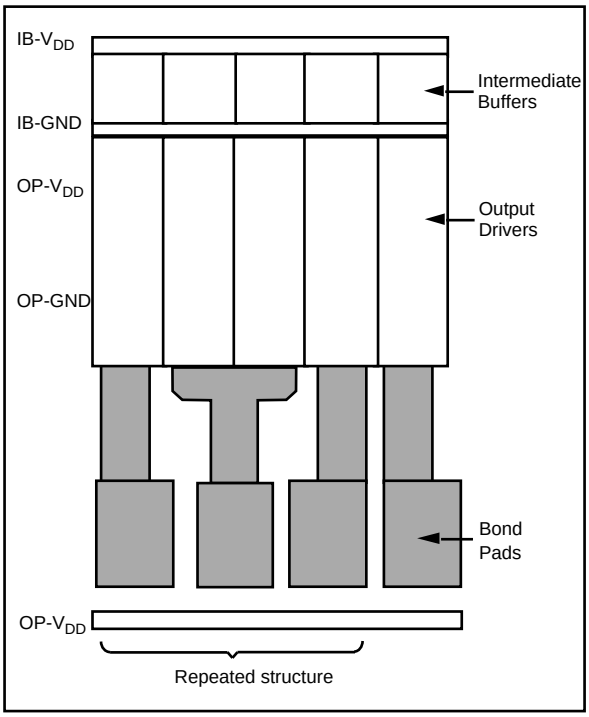

Figure 2 High density pad spacing

CLOCK AND POWER DISTRIBUTION

- Low skew clock distribution strategy
- Power ‘grid’ to minimize voltage drop

In large complex designs working at high-speed on chip clock and power distribution is vital to successful operation of the design. GPS have a number of techniques to minimize potential problems which can occur with clocking and powering the chip.

Clock Distribution

The clock distribution network must ensure that skew is minimized and that long term failure does not occur due to metal migration. The three solutions recommended are as follows:

Large buffer

Balanced Tree

Clock Grid

The clock distribution grid is shown in Figure 3 this overlay allows the use of high powered clock drivers without compromising reliability as a result of clock track electromigration. The clock is driven from a pre-amplifier halfway along the chip edge.A row of large inverters drive from the top and bottom of the chip on vertical metal 2 tracks. Straps run horizontally in metal 3 to form a grid. The grid is overlaid at the top hierarchical level using tracks that are reserved in all subcircuits and macrocells for top level clock and power distribution.

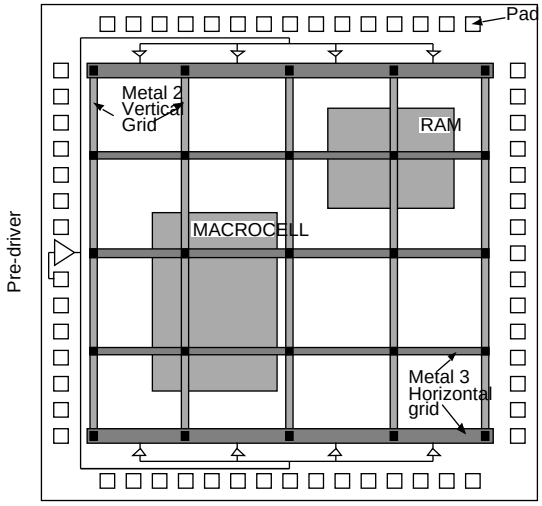

Figure 3 Clock distribution grid

Power Distribution

The power distribution metal in the array must be designed to avoid excessive voltage drops and long term failure due to electromigration.

Metal 1 V_{DD} and V_{SS} tracks pass through all the array cells. At regular intervals across the array the metal 1 supply rails are fed by vertical metal 2 straps. For designs using three layers of metal additional straps can be added in metal 3. Fig 4 shows a representation of the grid arrangement.

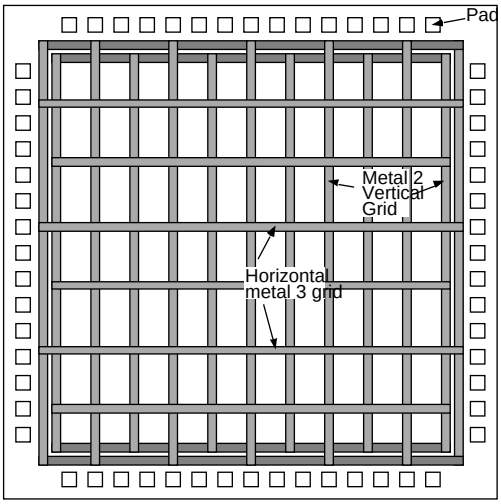

Figure 4 Power grid

MANUFACTURING

- Computer aided manufacturing
- Class 10 or better clean room conditions
- Vibration free for reliable manufacture

The CLA80k product is manufactured near Plymouth England in a purpose built factory for sub-micron process geometry's. The factory uses the latest automated equipment for 6 inch wafers within vibration free class 10 clean room conditions. Computer Aided Manufacture within the above environment ensures production efficiency and the lowest possible defect level. In addition to the world class wafer facility there are excellent probe and final test areas equipped with the latest analog and digital testers. This continued investment demonstrates GEC Plessey Semiconductors commitment to provide state-of-the-art CMOS ASICS.

CELL LIBRARY

- Comprehensive range of cells
- JTAG and Paracell sub libraries

A comprehensive cell library is available for the CLA80k series. It contains libraries that may be used in specific applications areas such JTAG boundary scan.

The library is being continually extended and cells in development are given at the end of the library list.

Buffers and Inverters

Cell Name	Cell Function
BUFX3	Non-inverting driver with x3 drive
BUFX7	Non-inverting driver with x7 drive
DELAY	Timing delay
INVX1	Inverter
INVX2	Inverter with x2 drive
INVX4	Inverter with x4 drive
INVX6	Inverter with x6 drive
INVX8	Inverter with x8 drive

NAND Gates

Cell Name	Cell Function
NAND2	2 input NAND gate
NAND2X2	2 input NAND gate with x2 drive
NAND3	3 input NAND gate
NAND3X2	3 input NAND gate with x2 drive
NAND4	4 input NAND gate
NAND4X2	4 input NAND gate with x2 drive

NOR Gates

Cell Name	Cell Function
NOR2	2 input NOR gate
NOR2X2	2 input NOR gate with x2 drive
NOR3	3 input NOR gate
NOR3X2	3 input NOR gate with x2 drive
NOR4	4 input NOR gate
NOR4X2	4 input NOR gate with x2 drive

AND Gates

Cell Name	Cell Function
AND2	2 input AND gate
AND2X2	2 input AND gate with x2 drive
AND3	3 input AND gate
AND3X2	3 input AND gate with x2 drive
AND4	4 input AND gate

OR Gates

Cell Name	Cell Function
OR2	2 input OR gate
OR2X2	2 input OR gate with x2 drive
OR3	3 input OR gate
OR3X2	3 input OR gate with x2 drive
OR4	4 input OR gate

Complex Gates

Cell Name	Cell Function
A2A2O2I	2 2-IP AND's into 2-IP NOR gate
O2O2A2I	2 2-IP OR's into 2-IP NAND gate
A2O2I	2-IP AND gate into 2-IP NOR gate
O2A2I	2-IP OR gate into 2-IP NAND gate
A2O3I	2-IP AND gate into 3-IP NOR gate
O2A3I	2-IP OR gate into 3-IP NAND gate
A3O2I	3-IP AND gate into 2-IP NOR gate
O3A2I	3-IP OR gate into 2-IP NAND gate
A2O2A2I	2-IP AND gate into 2-IP OR gate into 2-IP NAND gate
O2A2O2I	2-IP OR gate into 2-IP AND gate into 2-IP NOR gate

Exclusive ORs and Adders

Cell Name	Cell Function
EXOR	Exclusive OR gate
EXNOR	Exclusive NOR gate
HADD	Half adder
FADD	1 bit full adder
FADD2	2 bit full adder

Multiplexers

Cell Name	Cell Function
MUX2TO1	2 to 1 multiplexer
MUX4TO1	4 to 1 multiplexer
MUX8TO1	8 to 1 multiplexer

Tristate Drivers

Cell Name	Cell Function
BDRX4	Tristate bus driver with x4 drive
BDRX8	Tristate bus driver with x8 drive
BHOLD	Tristate bus hold

Clock Drivers

Cell Name	Cell Function
CLKP	Positive edge clock driver
CLKPX2	Positive edge clock driver with x2 drive
CLKPX3	Positive edge clock driver with x3 drive
CLKN	Negative edge clock driver
CLKNX2	Negative edge clock driver with x2 drive
CLKNX3	Negative edge clock driver with x3 drive

Clock Grid Drivers

Cell Name	Cell Function
CLKB84	Clock Grid Driver for CLT84000
CLKB85	Clock Grid Driver for CLT85000, MLT85000
CLKB86	Clock Grid Driver for CLT86000
CLKB87	Clock Grid Driver for CLT87000, MLT87000
CLKB88	Clock Grid Driver for CLT88000, MLT88000
CLKB89	Clock Grid Driver for CLT89000, MLT89000

Latches

Cell Name	Cell Function
SRLATCH	Set-Reset latch
DL	Data latch
DLR	Data latch with reset
BDL	Buffered data latch
BDLR	Buffered data latch with reset

Registers

Cell Name	Cell Function
DF	Master-slave D-type flip-flop
DFRS	Master-slave D-type flip-flop with set and reset
MDF	Multiplexed master-slave D-type flip-flop
MDFRS	Multiplexed master-slave D-type flip-flop with set and reset
BDF	Buffered master-slave D-type flip-flop
BDFRS	Buffered master-slave D-type flip-flop with set and reset
BMDF	Buffered multiplexed master-slave D-type flip-flop
BMDFRS	Buffered multiplexed master-slave D-type flip-flop with set and reset

Input Protection Cells

Cell Name	Cell Function
IPNR	Input with no pullup/pulldown resistor
IPR2P	Input with 2KOhms pullup resistor
IPR4P	Input with 100KOhms pullup resistor
IPR2M	Input with 2KOhms pulldown resistor

IPR4M	Input with 100KOhms pulldown resistor

Level Shifter Cells

Cell Name	Cell Function
DRV6	Multiple output driver cell
IBST1	CMOS schmitt trigger, 5 volt supply
IBST2	TTL schmitt trigger, 5 volt supply
IBST3	CMOS & TLL schmitt trigger, 3 volt supply
IBTTL1	TTL input: 5 volt supply
IBTTL2	TTL input: 3 volt supply
IBCMOS1	CMOS input: 5 volt supply
IBLEVELS	3 volt to 5 volt signal interface

Output Driver Controllers

Cell Name	Cell Function
IBCOP	Controller for push-pull, open source, and open drain output driver

IBCOP3	Controller for push-pull, open source, and open drain output driver
IBTRID	Controller for tristate output driver
IBTRID3	Controller for tristate output driver

Output Driver Cells

Cell Name	Cell Function
OPT3	Small output driver
OPT6	Standard output driver
OPT12	Large output driver

CLA8PARA LIBRARY

Cell Name	Cell Function
SPRAM	Single port RAM register file
DPRAM	Dual port RAM register file

CLA8JTAG LIBRARY

Cell Name	Cell Function
GGJTAP	JTAG Interface Controller
GGIDREG	JTAG identification register
GGJTREG	JTAG boundary scan register

CELLS IN DEVELOPMENT

Cell Name	Cell Function
PLLIB1	Phase Locked Loop
HDRAM	High density RAM
ROROM	ROM Paracell

DSP Macrocell Library (In development)

Cell Name	Cell Function
BMA8X8	Mixed Mode multiplier (8 by 8 bits)
BMA16X16	Mixed Mode multiplier (16 by 16 bits)

DESIGN SUPPORT

Design Route

- Flexible design route
- Proven right first time design

Design and layout support for the CLA80k arrays is available from many centers worldwide each of which is connected to our headquarters via high speed data links. A design center engineer is assigned to each customer's circuit to ensure the best assistance, and a smooth and efficient design flow.

GPS offers a variety of formal design routes as illustrated in Figure 5. A choice of routes allow for varying levels of customer involvement in a manner which complements individual customers' design styles, whilst maintaining our responsibility to ensure first time working devices.

The design process incorporates a design audit procedure to verify compliance with customer specification and to ensure manufacturability. The procedure includes four review meetings with the customer held at key stages of the design.

Review 1: Held at the beginning of the design cycle To check and agree on performance, packaging, specifications and design timescales.

Review 2: Held after Logic Simulation but prior to layout to ensure satisfactory functionality, timing performance, and

adequate fault coverage.

Review 3: Held after Layout and Post Layout Simulation Verification of satisfactory design performance after insertion of actual track loads. Final check of all device specifications before prototype manufacture.

Review 4: Held after Prototype Delivery to confirm that devices meet all specifications and are suitable for full scale production.

THIRD PARTY DESIGN TOOLS

- Design Kits for major industry standard ASIC design software tools
- Libraries include Advanced Delay Modelling Capability as appropriate
- EDIF 2.0 interface

GPS supports a wide range of third party design tools including Mentor and Synopsis. **(Please check with our Sales Offices for the most recent additions).** The design kits offer fully detailed timing information for all cell libraries, netlist extraction utilities, and post layout back annotation capability where applicable. An example of a workstation design flow is shown in Figure 6. Please contact your local GEC Plessey Semiconductor's sales office for further information about support of particular tools.

PDS2 - THE GPS ASIC DESIGN SYSTEM

- Behavioral, Functional, and Gate Level Modelling
- Supports Advance Delay Modelling
- Supports Hierarchical Design Techniques
- Autoplace and Route tools available

PDS2 is GPS's own proprietary ASIC design system. It provides a fully-integrated, technology independent VLSI design environment for all GPS CMOS SemiCustom products.

PDS2 runs on SUN and Digital Equipment Computers. It comprises design capture (schematic capture or VHDL), testability analysis, logic simulation, fault simulation, auto place and route, and back annotation. The system offers full support for hierarchical design techniques, maintained from design capture through to layout, as well as advanced design management tools. PDS2 may be used either at a GPS Design Center or under licence at the customer's premises. A three day training course is available for first time users.

Figure 5 CAD SUPPORT - Design Routes

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	THIRD PARTY SOFTWARE	PDS IN-HOUSE SOFTWARE	TURNKEY SERVICE
Design review 1			
Capture	Customer	Customer	GPS
Simulation	Customer	Customer	GPS
Design review 2			
Physical design	GPS	Customer or GPS	GPS
Design review 3			
Prototype manufacturing	GPS		
Prototype evaluation	Customer		
Design review 4			
Production	GPS		

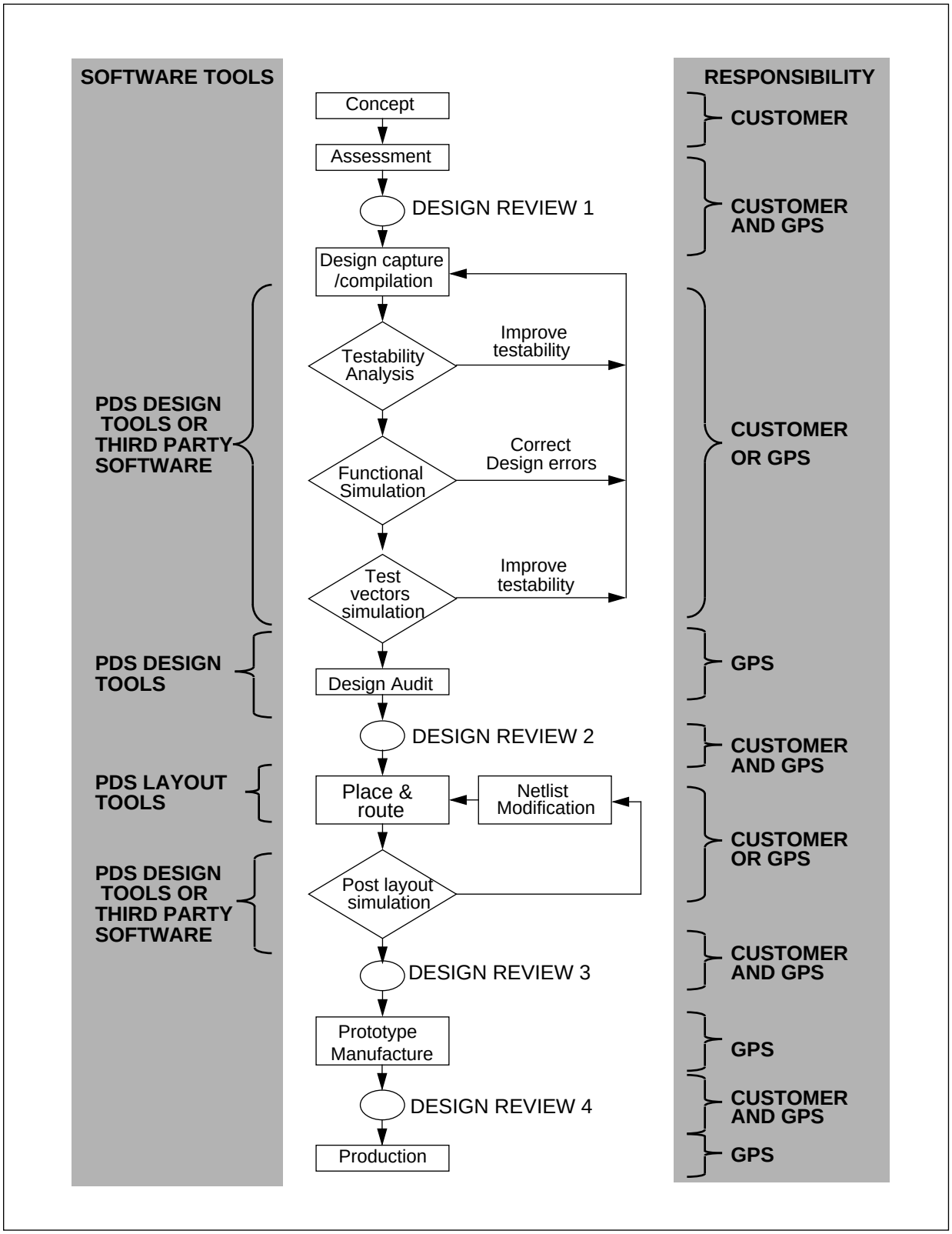


Figure 6 Design Flow

THERMAL MANAGEMENT

- Low power CMOS for better thermal management
- 1.3µW per gate per MHz (3V supply)
- High pinout power packages available

The increase in speed and density available through advanced CMOS processes, results in a corresponding increase in power dissipation. SemiCustom designers now have the ability to design circuits of 260,000 gates and over, and chip power consumption is a very important concern.

The logic core of 260k plus gates is the dominant factor in power dissipation at this complexity. It is essential to offer ultra low power core logic to maintain an acceptable overall chip power budget.

To minimize this problem GPS's CLA80k arrays offer low power factors and a selection of power packages. Dissipation of 1.3µW per gate per MHz (3V supply) is lower than most competitive arrays, with the reduced junction temperatures having the added advantage of improved performance and reliability.

CLA80k POWER DISSIPATION CALCULATION

CLA80k series power dissipation for any array can be estimated by following the example for the CLA87XXX at a typical voltage of 5V.

Number of available gates	157872
Gates used	40%
Gates switching	15%
Power dissipation/gate/MHz (µW) (gate fanout typically 2 loads, at 5V)	4.1
Frequency (MHz)	10
Total core dissipation (mW)	388
Number of I/O pads used as Outputs	122
Outputs switching each cycle	20%
Dissipation/output buffer/MHz/pF (µW)	25
Output loading in pF	50
Output buffer power (mW)	305
Total Power at 10MHz clock rate (W)	0.7

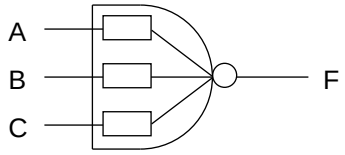
ADVANCED DELAY MODELLING

- Accurate delay calculation
- Edge speed modelling
- Pin to pin timings
- Non-linear delay modelling
- Accurate delay derating

The accuracy of the delay modelling is demonstrated by the results shown in the table over.

Pin to Pin Delays

Delay models use pin to pin times for both rising and falling delays between each input and output pin.



The use of pin to pin delays improves simulation accuracy as there can be considerable variation in delay between different input pins. For complex gates (e.g. AND-NOR gates or adders) the variation is up to 40%. For simple NAND and NOR logic gates the typical variation is 20%.

Non-linear curve fitting

Figure 7 and Figure 8 show the rising and falling delay through an inverter. For fast input edges (0.5ns) delay time increases linearly with the output load. For high output loads delay increases linearly with edge speed. Delay for slow input edges and light input loads do not follow the linear model. A simple linear model cannot represent delay accurately. The following equation is used to model delay for CLA80k

$$Delay = K_1 + K_2 Load + K_3 Edge - \left(e^{\frac{K_4 Edge}{\left(\frac{K_5 Load}{Edge}\right)}} \right)$$

K_1 - Intrinsic delay. The delay with load and input edge speed set to zero.
K_2 - Delay sensitivity to load.
K_3 - Delay sensitivity to input edge speed.
K_4 & K_5 - These coefficients reduce the effect of edge for light output loadings.

Cell	Conditions	CLA80k delay (ps)	CLA70k delay (ps)	Change	SPICE (ps)	Accuracy
8 stage ripple carry adder	Typical process, 5V, 25°C	4872	9608	49%	4679	4.0%
8 stage ripple carry adder	Slow process, 4.5V, 70°C	7696	25076	69%	7455	3.2%
10 NAND2 gates, lightly loaded	Slow process, 4.5V, 70°C	3463	8694	60%	3464	0.0%
10 NAND2 gates mixed heavy then light loading	Slow process, 4.5V, 70°C	12825	21047	39%	12479	2.8%
10 NAND2 gates heavy loading	Slow process, 4.5V, 70°C	27421	34619	21%	28606	4.1%

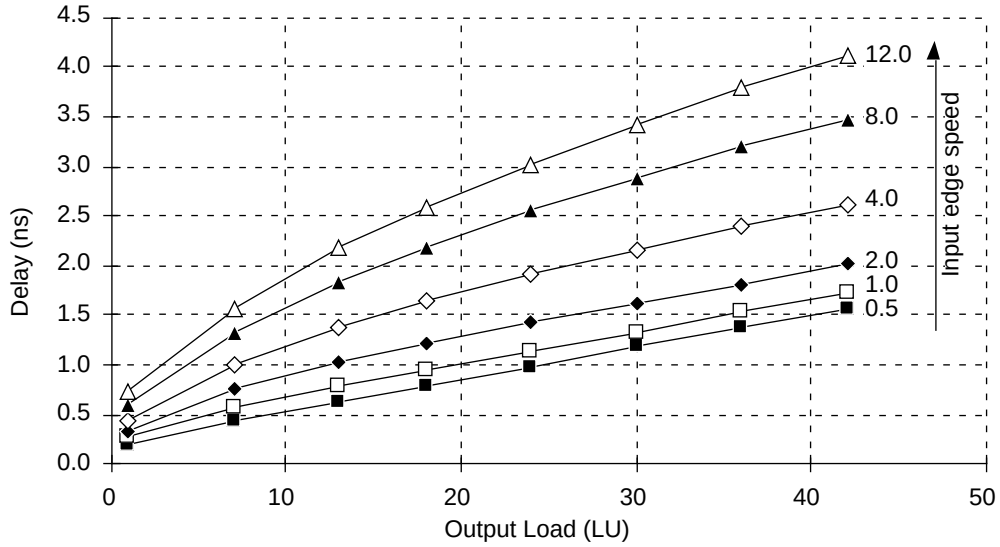


Figure 7 Inverter falling delay

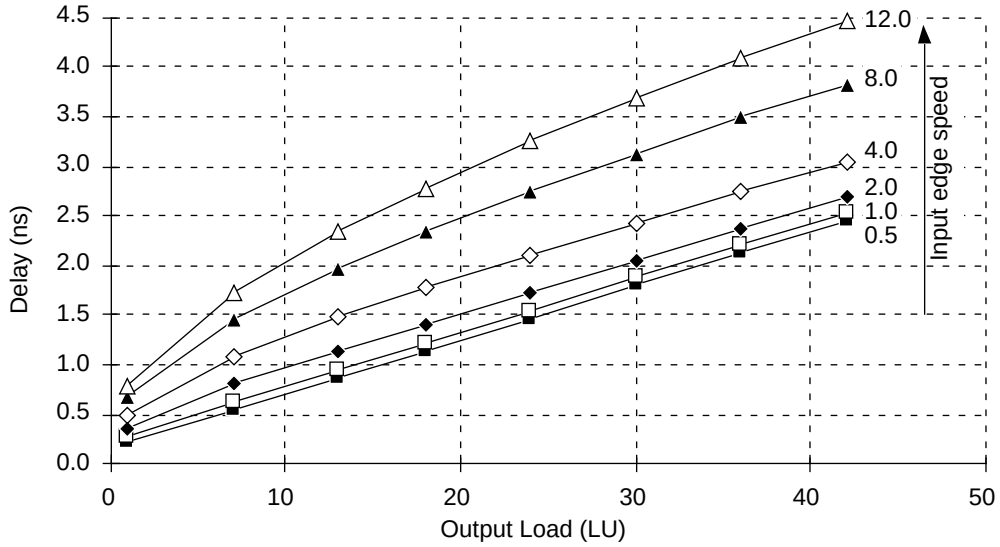


Figure 8 Inverter rising delay

Derating for Supply Voltage

Figure 9 shows the increase in gate delay as supply voltage is reduced.

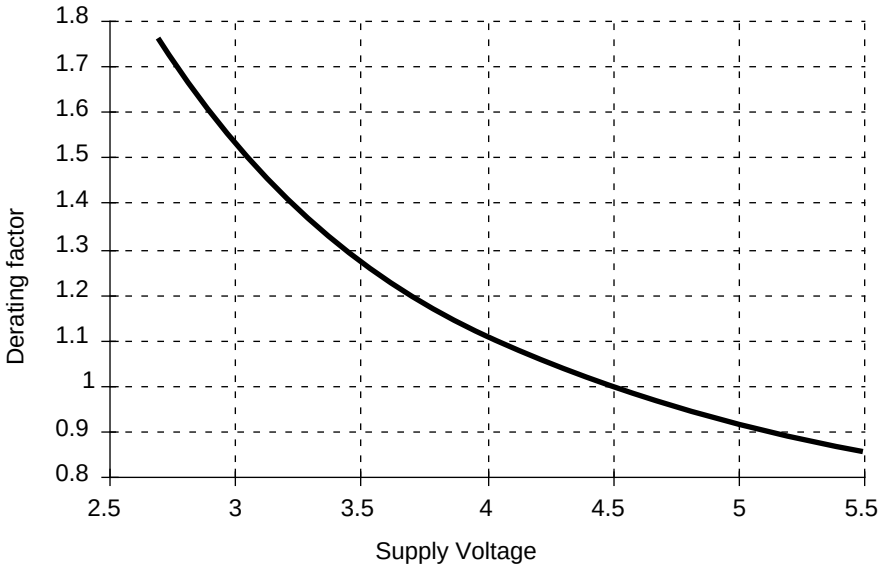


Figure 9 Derating with supply voltage

Derating for Temperature

Figure 10 shows the increase in gate delay as the chip junction temperature is increased. The Table 2.2 below shows the specific derating values for a range of junction temperatures. It is important to use the junction and not the ambient temperature for worst case simulations

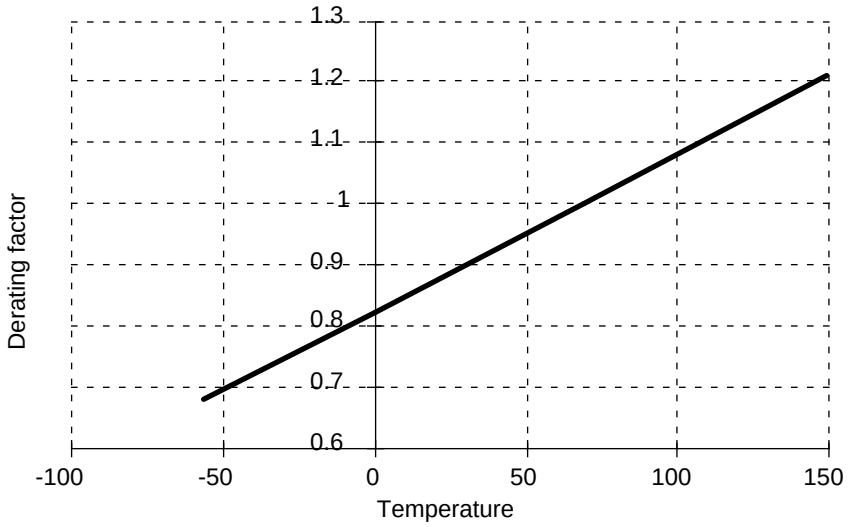


Figure 10 Derating with Temperature

AC ELECTRICAL CHARACTERISTICS

GATES	3V		4.5V	
	2 load units	4 load units	2 load units	4 load units

GATES		3V		4.5V	
INVX1	tpLH	590 ps	889 ps	421 ps	613 ps
	tpHL	283 ps	391 ps	197 ps	272 ps
NAND2X2	tpLH	528 ps	683 ps	392 ps	490 ps
	tpHL	291 ps	398 ps	200 ps	269 ps
NOR2x2	tpLH	752 ps	1065 ps	476 ps	664 ps
	tpHL	249 ps	303 ps	162 ps	205 ps
DF	tpLH	1068 ps	1412 ps	689 ps	910 ps
	tpHL	970 ps	1117 ps	584 ps	685 ps

INPUTS		3V		4.5V	
		2 load units	4 load units	2 load units	4 load units
TTL I/P	tpLH	767 ps	922 ps	708 ps	810 ps
	tpHL	704 ps	761 ps	114 ps	1168 ps
CMOS I/P	tpLH	791 ps	872 ps	547 ps	599 ps
	tpHL	629 ps	659 ps	433 ps	454 ps
CMOS SCHMITT	tpLH	1413 ps	1592 ps	1114 ps	1223 ps
	tpHL	1703 ps	1778 ps	786 ps	831 ps

OUTPUT		3V		4.5V	
		2 load units	4 load units	2 load units	4 load units
6mA BISTATE	tpLH	3615 ps	8811 ps	2320 ps	5700 ps
	tpHL	2472 ps	4549 ps	1538 ps	2886 ps
12mA BISTATE	tpLH	4672 ps	7286 ps	2842 ps	4552 ps
	tpHL	3814 ps	5106 ps	2315 ps	3073 ps
24mA OPENDRAIN	tpLH	5500 ps	6917 ps	3306 ps	4321 ps
	tpHL	5011 ps	6463 ps	2915 ps	3860 ps

Notes: Assumes worst case process, temperature = 70˚C, input edge = 0.5 nS

DC ELECTRICAL CHARACTERISTICS

All characteristics are for temperatures between -55 and 150°C and supply voltages between 2.7 and 5.5V unless otherwise specified.

Absolute Maximum Ratings

PARAMETER	Min.	Max.	Units
Supply Voltage	-0.5	7.0	V
Input Voltage	-0.5	V_{DD}+0.5	V
Output Voltage	-0.5	V_{DD}+0.5	V
Static discharge voltage (HBM)		4	kV
Storage Temperature			
Ceramic	-65	150	°C
Plastic	-40	125	°C

Exceeding the absolute maximum ratings may cause permanent damage to the device. Extended exposure at the maximum ratings will affect device reliability.

HBM stands for Human Body Model.

Normal Operating Conditions

Neither performance nor reliability is guaranteed outside these limits. Extended operation above these limits may affect device reliability.

PARAMETER	Min.	Max.	Units
Supply Voltage	2.7	5.5	V
Input Voltage	V_{SS}	V_{DD}	V
Output Voltage	V_{SS}	V_{DD}	V
Current per pad		100	mA
Junction Temperature	-55	150	°C
Ambient Temperature			
Commercial Grade	0	70	°C
Industrial Grade	-40	85	°C
Military Grade	-55	125	°C

DC Electrical Characteristics

All characteristics are for temperatures between -55 and 150°C and supply voltages between 2.7 and 5.5V unless otherwise specified.The data in the tables below is from simulated information and limited testing of silicon

Characteristic	Sym	Value			Unit	Conditions
		Min.	Typ.	Max.		
TTL input - IBTTL1						$4.5 \le V_{DD} \le 5.5V$
Input low voltage	V_{IL}			0.8	V	
Input high voltage	V_{IH}	2.0			V	
TTL input - IBTTL2						$2.7 \le V_{DD} \le 3.6V$
Input low voltage	V_{IL}			0.8	V	
Input high voltage	V_{IH}	2.0			V	
CMOS input - IBCMOS1						$2.7 \le V_{DD} \le 5.5V$
Input low voltage	V_{IL}					
Input high voltage	V_{IH}	$0.7V_{DD}$				
CMOS Schmitt - IBST1						
Input low voltage	V_{IL}					
Input high voltage	V_{IH}	$0.7V_{DD}$				
Hysteresis	V_H	400				
TTL Schmitt - IBST2						
Input low voltage	V_{IL}					
Input high voltage	V_{IH}	2.0				
Hysteresis	V_H	300				
Low voltage Schmitt - IBST3						
Input low voltage	V_{IL}					
Input high voltage	V_{IH}	$0.7V_{DD}$				
Hysteresis	V_H	80				
Input current or resistance						
No resistor - IPNR	I_{IN}				µA	$V_{IN} = V_{DD}$ or V_{SS}
Pullup - IPR2P	R_1	1	2	4	kΩ	
Pullup - IPR4P	R_2	50	110	220	kΩ	
Pulldown - IPR2M	R_3	1	2	4	kΩ	
Pulldown - IPR4M	R_4	50	110	220	kΩ	

Characteristic	Sym	Value			Unit	Conditions
		Min	Typ.	Max.		
High output voltage						$2.7 \le V_{DD} \le 3.6V$
All outputs	V_{OH}		V_{DD}-0.05		V	I_{OH} = -1µA
OPT3	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -2mA
OPT6	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -4mA
OPT12	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -8mA
Low output voltage						$2.7 \le V_{DD} \le 3.6V$
All outputs	V_{OL}		V_{SS}-0.05		V	I_{OL} = 1µA
OPT3	V_{OL}		0.2	0.4	V	I_{OL} = 3mA
OPT6	V_{OL}		0.2	0.4	V	I_{OL} = 6mA
OPT12	V_{OL}		0.2	0.4	V	I_{OL} = 12mA

High output voltage						$4.5 \le V_{DD} \le 5.5V$
All outputs	V_{OH}		V_{DD}-0.05		V	I_{OH} = -1µA
OPT3	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -6mA
OPT6	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -12mA
OPT12	V_{OH}	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH} = -24mA
Low output voltage						$4.5 \le V_{DD} \le 5.5V$
All outputs	V_{OL}		V_{SS}-0.05		V	I_{OL} = 1µA
OPT3	V_{OL}		0.2	0.4	V	I_{OL} = 6mA
OPT6	V_{OL}		0.2	0.4	V	I_{OL} = 12mA
OPT12	V_{OL}		0.2	0.4	V	I_{OL} = 24mA

Characteristic	Sym	Value			Unit	Conditions
		Min	Typ.	Max.		
Tristate output leakage						-55 to 100°C
OPT3	I_{OZ}	-1		1	µA	$V_{OUT} = V_{SS}$ or V_{DD}
OPT6	I_{OZ}	-1		1	µA	$V_{OUT} = V_{SS}$ or V_{DD}
OPT12	I_{OZ}	-1		1	µA	$V_{OUT} = V_{SS}$ or V_{DD}
Tristate output leakage						-55 to 150°C
OPT3	I_{OZ}	-2		2	µA	$V_{OUT} = V_{SS}$ or V_{DD}
OPT6	I_{OZ}	-2		2	µA	$V_{OUT} = V_{SS}$ or V_{DD}
OPT12	I_{OZ}	-4		4	µA	$V_{OUT} = V_{SS}$ or V_{DD}
Output short circuit current						$4.5 \le V_{DD} \le 5.5V$
OPT3	I_{OS}	41	82	164	mA	V_{DD} = max, $V_O = V_{DD}$
OPT6	I_{OS}	82	164	328	mA	V_{DD} = max, $V_O = V_{DD}$
OPT12	I_{OS}	164	328	656	mA	V_{DD} = max, $V_O = V_{DD}$
Output short circuit current						$4.5 \le V_{DD} \le 5.5V$
OPT3	I_{OS}	19	38	76	mA	V_{DD} = max, $V_O = V_{SS}$
OPT6	I_{OS}	38	76	152	mA	V_{DD} = max, $V_O = V_{SS}$
OPT12	I_{OS}	76	152	304	mA	V_{DD} = max, $V_O = V_{SS}$
Output short circuit current						$2.7 \le V_{DD} \le 3.6V$
OPT3	I_{OS}	16	32	64	mA	V_{DD} = max, $V_O = V_{DD}$
OPT6	I_{OS}	32	64	128	mA	V_{DD} = max, $V_O = V_{DD}$
OPT12	I_{OS}	64	128	256	mA	V_{DD} = max, $V_O = V_{DD}$
Output short circuit current						$2.7 \le V_{DD} \le 3.6V$
OPT3	I_{OS}	7	15	30	mA	V_{DD} = max, $V_O = V_{SS}$
OPT6	I_{OS}	15	30	60	mA	V_{DD} = max, $V_O = V_{SS}$
OPT12	I_{OS}	30	60	120	mA	V_{DD} = max, $V_O = V_{SS}$
Operating Power	P_{DD}		1.3		µW/ MHz	V_{DD} = 3V, note 1
			4.1			V_{DD} = 5V, note 1
Input capacitance	C_I		5		pF	Any input, note 2
Output capacitance	C_{OUT}		6		pF	Any output, note 2
Bidirectional capacitance	C_{BI}		6		pF	Any I/O pin, note 2

Note 1 - For NAND2 with two standard loads.

Note 2 - The capacitance values do not include the package.

Quality and Reliability

- Statistical process control used in manufacture
- Regular sample screening and reliability testing
- Screening to MIL and other recognized standards

At GPS quality and reliability are built into the product by statistical control of all processing operations and by minimizing random uncontrolled effects in all manufacturing operations. Process management involves full documentation of procedures, recording of batch by batch data using traceability procedures. This is performed using the latest equipment to perform sample screening and conformance testing on finished product.

A common information management system is used to monitor the manufacturing of GPS CMOS and Bipolar processes and operations. All product benefit from the use of this integrated monitoring system resulting in the highest quality standards for all technologies.
Further information is contained in the Quality Brochure, available from GPS Sales Offices.

PACKAGING

- Wide range of surface mount and through board packages
- Ceramic equivalents to most plastic packages - for fast prototyping
- Ongoing commitment to new package development

PACKAGING OPTIONS

The package style and pin count information is intended only as a guide. Detailed package specifications are available from GPS Design Centers on request. New packages are being continually introduced, so if a particular package is not listed, please enquire through your GPS Sales Representative.

The tables below indicate the preferred array size to package combinations. A stock is held of the preferred packages to ensure a fast prototype assembly turn around. Alternative array size to package combinations are available, however these packages are not held in stock and extended lead times may affect prototype delivery schedules.

HIGH DENSITY PAD ARRAY PRODUCTION PACKAGING OPTIONS

Metric Quad Flat Pack (MQFP)

Package	Body	Pitch	CLA81	CLA82	CLA83	CLA84	CLA85	CLA86	CLA87	CLA88	CLA89
GPB44	10x10x2.0	0.80	■								
GPB52	10x10x2.0	0.65	■								
GPF64	14x20x2.8	1.00	■	■							
GPF80	14x20x2.8	0.80		■	■						
GPF100	14x20x2.8	0.65		■	■	■					
GPK120	28x28x3.4	0.80			■	■					
GPK128	28x28x3.4	0.80				■					
GPK144	28x28x3.4	0.65					■				
GPK160	28x28x3.4	0.65					■	■			

Fine Pitch Quad Flat Pack (FQFP)

Package	Body	Pitch	CLA81	CLA82	CLA83	CLA84	CLA85	CLA86	CLA87	CLA88	CLA89
FPB100	14x14x2.0	0.50		■	■	■					
FPH208	28x28x3.4	0.50						■	■		
FPJ240	32x32x3.4	0.50							▭		
FPL304	40x40x3.4	0.50							▭	▭	▭

Thin Quad Flat Pack (TQFP)

Package	Body	Pitch	CLA81	CLA82	CLA83	CLA84	CLA85	CLA86	CLA87	CLA88	CLA89
FPM48	7x7x1.4	0.50	■								
FPO64	10x10x1.4	0.50	▭	■							
FPB100	14x14x1.4	0.50		■	■						
FPN144	20x20x1.4	0.50				▭	▭				

In Development ▭

PACKAGING OPTIONS

HIGH DENSITY PAD ARRAY PRODUCTION

Metal Quad Flat Pack (MQUAD)

Package	Body	Pitch	CLA81	CLA82	CLA83	CLA84	CLA85	CLA86	CLA87	CLA88	CLA89
GMP100	14x20x2.7	0.65			▭	▭					
GMP120	28x28x3.4	0.80				▭					

GMP128	28x28x3.4	0.80									
GMP144	28x28x3.4	0.65									
GMP160	28x28x3.4	0.65									
GMP208	28x28x3.4	0.50									
GMP240	32x32x3.4	0.50									
GMP304	40x40x3.4	0.50									

Plastic 'J' Leaded Chip Carrier (PLCC)

Package	CLA81	CLA82	CLA83	CLA84	CLA85	CLA86	CLA87	CLA88	CLA89
HPA28									
HPA44									
HPA68									
HPA84									

Small Outline (SO)

Package	CLA81	CLA82	CLA83	CLA84	CLA85	CLA86	CLA87	CLA88	CLA89
MPE16									
MPE20									
MPE24									
MPE28									

Prototypes for MQFP and MQUAD (Ceramic Quad Flat Pack)

Package	Body	Pitch	CLA81	CLA82	CLA83	CLA84	CLA85	CLA86	CLA87	CLA88	CLA89
GGA44	10x10x3.2	0.80	■								
GGA52	10x10x3.2	0.65	■								
GGC64	14x20x2.8	1.00	■	■							
GGC80	14x20x2.8	0.80		■	■						
GGC100	14x20x2.8	0.65		■	■	■					
GGD120	28x28x3.6	0.80			■	■					
GGD128	28x28x3.6	0.80				■					
GGD144	28x28x3.6	0.65					■				
GGD160	28x28x3.6	0.65						■			

Prototypes for FQFP and MQUAD (Ceramic Quad Flat Pack)

Package	Body	Pitch	CLA81	CLA82	CLA83	CLA84	CLA85	CLA86	CLA87	CLA88	CLA89
FGB100	14x14x2.8	0.50		■	■	■					
FGD208	28x28x3.6	0.50							▒	▒	▒
FGF240	32x32x3.6	0.50								▒	▒
FGF304	40x40x3.6	0.50									▒

Prototypes for TQFP (Ceramic Quad Flat Pack)

Package	Body	Pitch	CLA81	CLA82	CLA83	CLA84	CLA85	CLA86	CLA87	CLA88	CLA89
GGA52	10x10x3.2	0.65	■	■							
FGO64	14x20x2.8	0.50	■	■							
FGB100	14x14x2.8	0.50		■	■						
FGN144	20x20x2.8	0.50				■	■				

Prototypes for PLCC (Ceramic 'J' Leaded Chip Carrier)

Package	CLA81	CLA82	CLA83	CLA84	CLA85	CLA86	CLA87	CLA88	CLA89
HCA28	■								
HCA44	■								
HCA68	▒	■							
HCA84		▒	■						

Prototypes for SO (Ceramic Small Outline)

Package	CLA81	CLA82	CLA83	CLA84	CLA85	CLA86	CLA87	CLA88	CLA89
MCA16	■								
MCA20	■								
MCA24	■								
MCA28	■								

STANDARD DENSITY PAD ARRAY OPTIONS

Ceramic 'J' Leaded Chip Carrier

Package	MLA85	MLA87	MLA88	MLA89
HCA68	■			
HCA84	■			

Ceramic Leaded Chip Carrier

Package	MLA85	MLA87	MLA88	MLA89
GCA132	■	■		
GCA172		■	■	
GCA196		■	■	■

Power Ceramic Leaded Chip Carrier

Package	MLA85	MLA87	MLA88	MLA89
GCP132		■		
GCP172		■	■	
GCP196		■	■	■
GCP256			■	■
GCP304				

Ceramic Pin Grid Array (PGA)

Package	MLA85	MLA87	MLA88	MLA89
ACA84	■			
ACA100	■			
ACA120	■	■		
ACA144		■		
ACA180		■	■	
ACA257			■	

Power Ceramic Pin Grid Array

Package	MLA85	MLA87	MLA88	MLA89
ACB84		■		
ACB144		■	■	
ACB208		■	■	

The package matrices shown above where correct at the time of publication please consult your local design centre for the latest information.

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