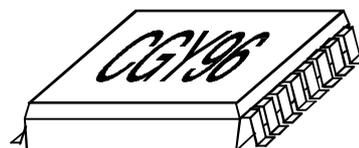


*Preliminary Datasheet*

- \*Power amplifier for GSM class 4 phones
- \*3.2 W (35dBm) output power at 3.5 V
- \*Overall power added efficiency 50 %
- \*Fully integrated 3 stage amplifier
- \*Single supply operation
- \*Power ramp control
- \*Input matched to 50 ohms, simple output match



ESD: **E**lectrostatic **d**ischarge sensitive device,  
observe handling precautions!

Type	Marking	Ordering code (taped)	Package
CGY 96	CGY 96	tbd	MW 16

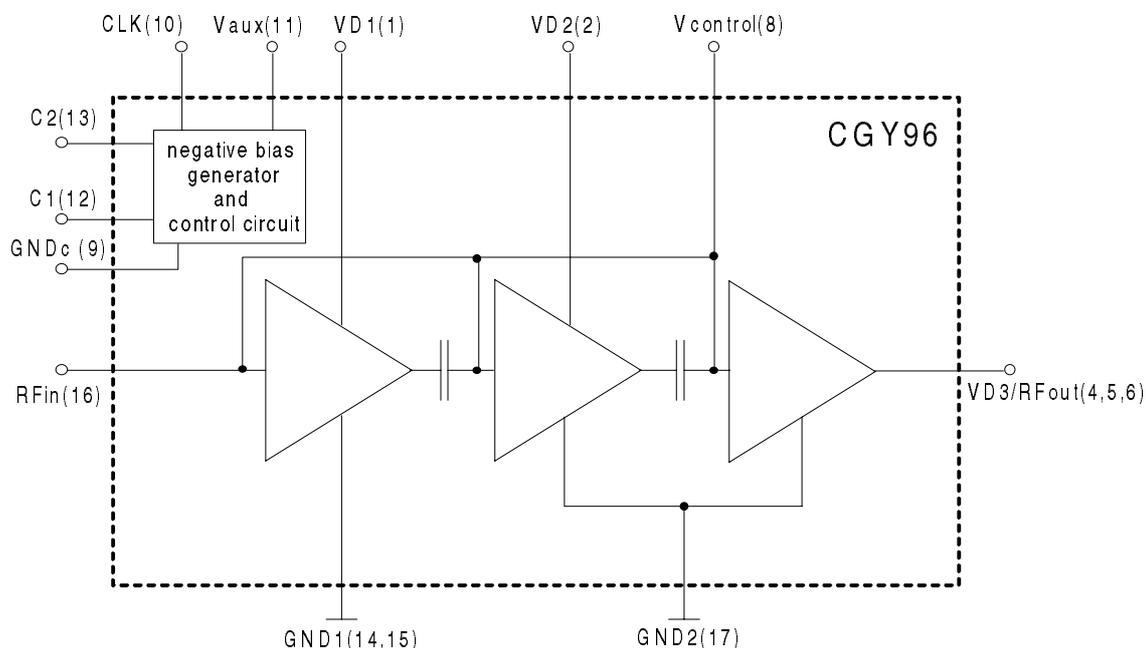
**Maximum ratings**

Characteristics	Symbol	max. Value	Unit
Positive supply voltage	$V_D$	9	V
Supply current	$I_D$	4	A
Channel temperature	$T_{Ch}$	150	°C
Storage temperature	$T_{stg}$	-55...+150	°C
Pulse peak power dissipation <i>duty cycle 12.5%, <math>t_{on}=0.577ms</math></i>	$P_{Pulse}$	tbd	W
Total power dissipation ( $T_s \leq 80\text{ °C}$ ) <i><math>T_s</math>: Temperature at soldering point</i>	$P_{tot}$	tbd	W

**Thermal Resistance**

Channel-soldering point	$R_{thChS}$	tbd	K/W
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Functional block diagramm:



Pin #		Configuration
1	<b>VD1</b>	Drain voltage 1st stage
2	<b>VD2</b>	Drain voltage 2nd stage
3	<b>n.c.</b>	-
4,5,6	<b>VD3 / RFout</b>	Drain 3rd stage and rf-output
7	<b>n.c.</b>	-
8	<b>Vcontrol</b>	Control voltage for power ramping
9	<b>GNDc</b>	Ground negative voltage generator
10	<b>Clk</b>	Clock input
11	<b>Vaux</b>	Supply voltage neegative voltage generator
12	<b>C1</b>	Coupling capacitor negative voltage generator
13	<b>C2</b>	Block capacitor negativ voltage generator
14,15	<b>Gnd1</b>	Ground pin 1st stage
16	<b>RFin</b>	RF Input
(17)	<b>GND2</b>	Ground (backside of MW16 housing)

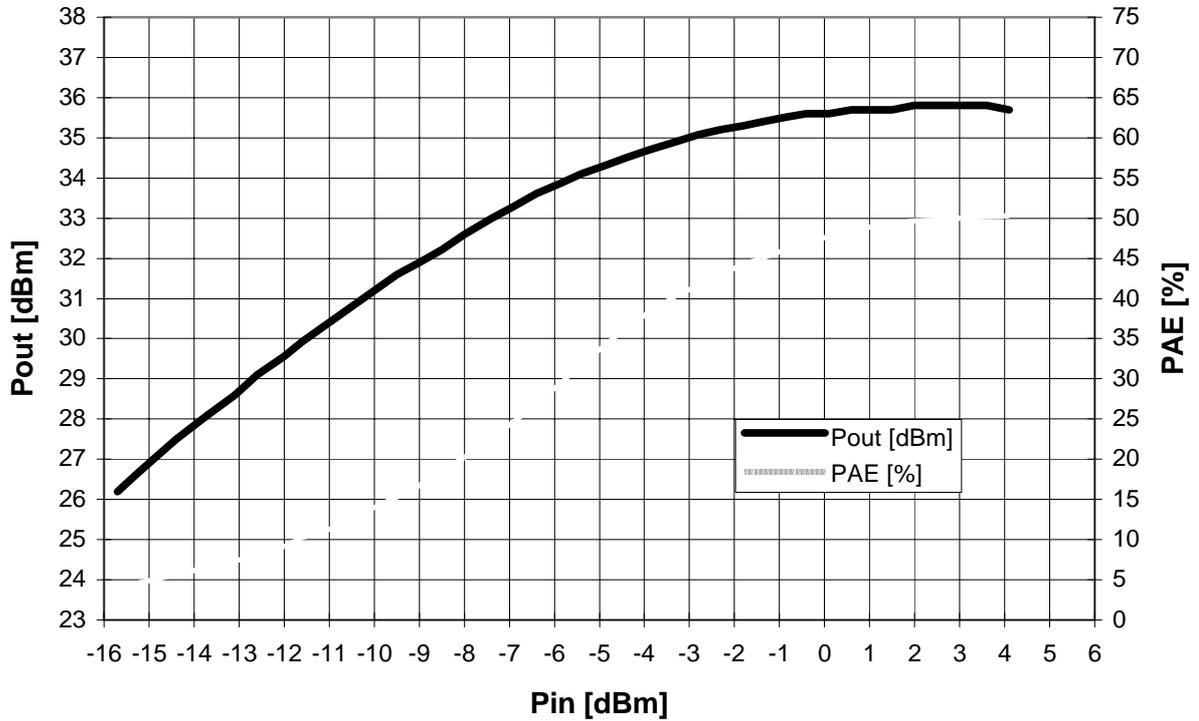
## Electrical characteristics

( $T_A = 25^\circ\text{C}$ ,  $f=0.9\text{ GHz}$ ,  $Z_S=Z_L=50\text{ Ohm}$ ,  $V_D=3.5\text{V}$ ,  $V_{aux}=3.5\text{V}$ ,  $V_{control}=2.2\text{V}$ ;  
pulsed with a duty cycle of 12.5%,  $t_{on}=577\mu\text{sec}$ )

Characteristics	Symbol	min	typ	max	Unit
Supply current <i>P<sub>in</sub>=0dBm</i>	$I_D$	-	2.0	-	A
Supply current neg. voltage gener. <i>V<sub>aux</sub>=3.5V</i>	$I_{AUX}$	-	10	-	mA
Gain (small signal)	$G$	-	40	-	dB
Power gain <i>P<sub>in</sub>=0dBm</i>	$G_P$	-	35	-	dB
Output Power <i>P<sub>in</sub>=0dBm</i>	$P_{OUT}$	-	35	-	dBm
Overall Power added Efficiency <i>P<sub>in</sub>=0dBm</i>	$\eta$	-	50	-	%
Dynamic range output power <i>V<sub>control</sub> = 0.2...2.2V</i>		-	80	-	dB
Harmonics <i>P<sub>in</sub>=0dBm</i>	$H(2f_0)$	-	-40	-	dBc
	$H(3f_0)$	-	-43	-	dBc
	$H(4f_0)$	-	-44	-	dBc
Noise Power in RX (935-960MHz) <i>P<sub>in</sub>=0dBm, P<sub>out</sub>=35dBm, 100kHz RBW</i>	$N_{RX}$	-	-81	-	dBm
Stability <i>all spurious outputs &lt; -60dBc, VSWR load, all phase angles</i>		-	10 : 1	-	-
Input VSWR		-	1.7 : 1	-	-

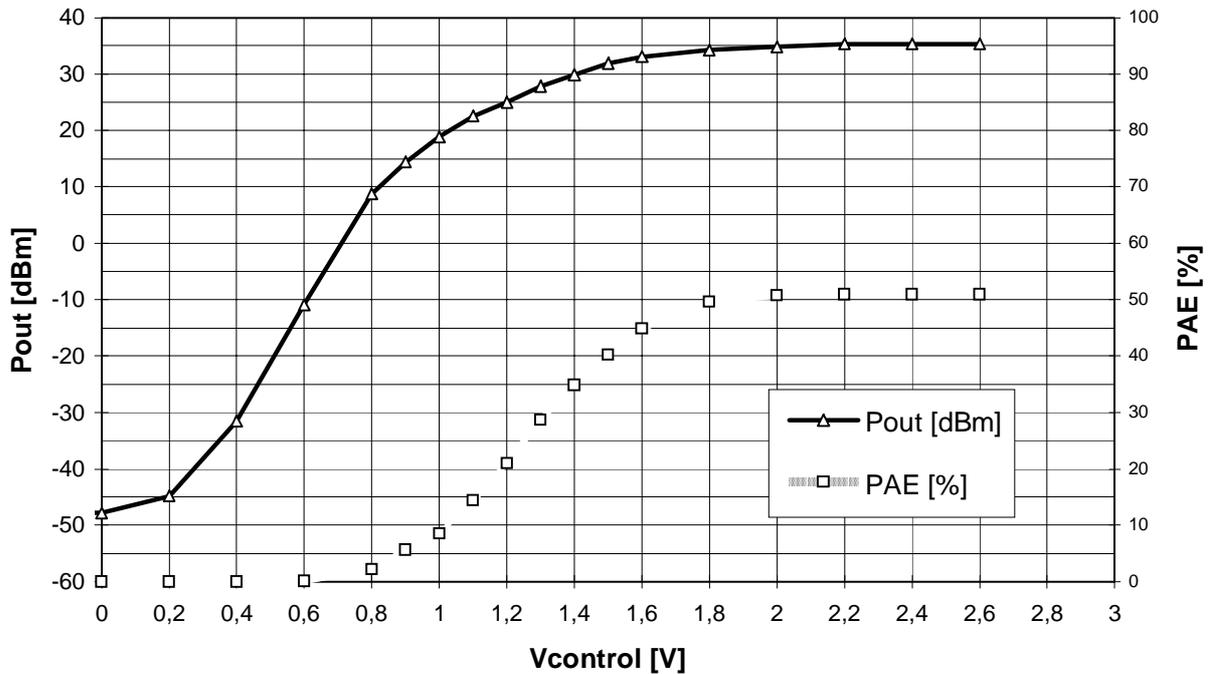
Output Power and PAE vs. Input Power

(Vd=3.5V, Vcontrol=2.2V, f=900MHz, duty cycle 12.5%, ton=577µs)



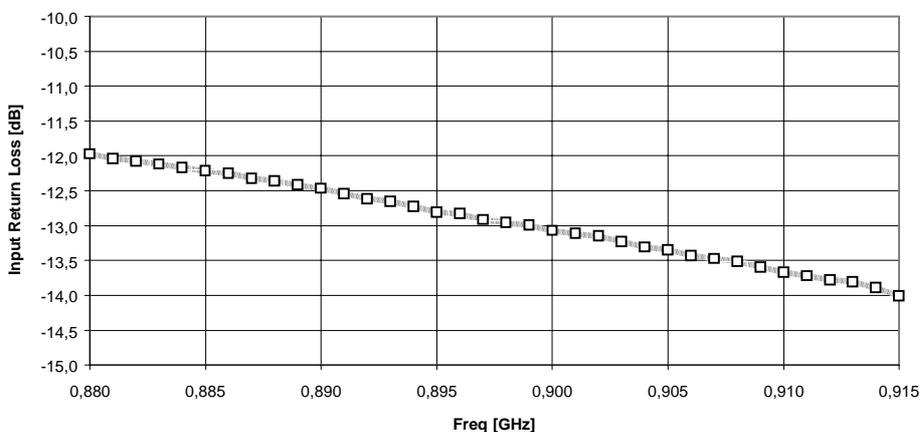
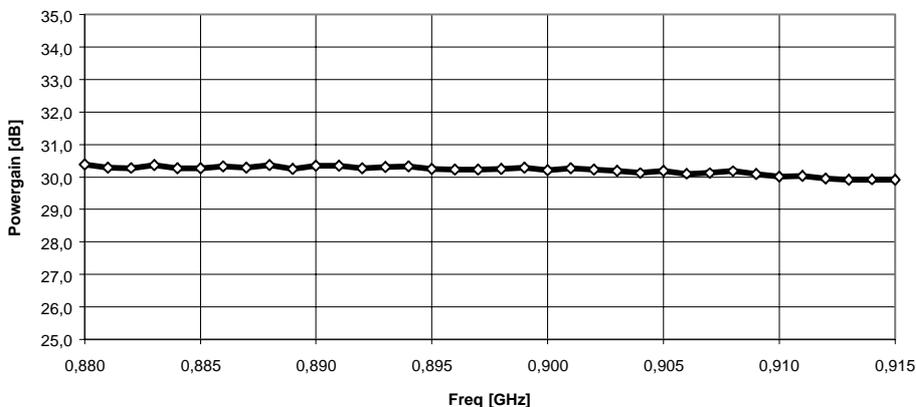
Output Power and PAE vs. Control Voltage:

(Vd=3.5V, Pin=0dBm, f=900MHz, duty cycle 12.5%, ton=577µs)



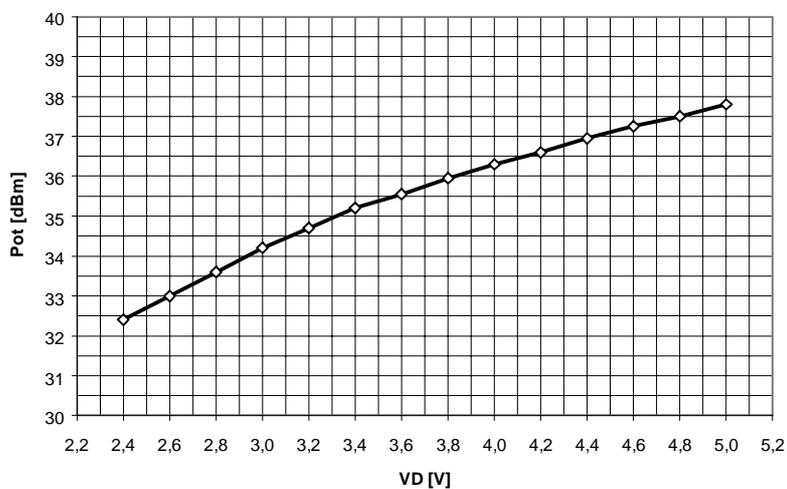
### Power Gain and Input Return Loss vs. Frequency

( $V_d=3.5V$ ,  $V_{control}=2.2V$ ,  $P_{in}=5dBm$ , duty cycle 12.5%,  $t_{on}=577\mu s$ )



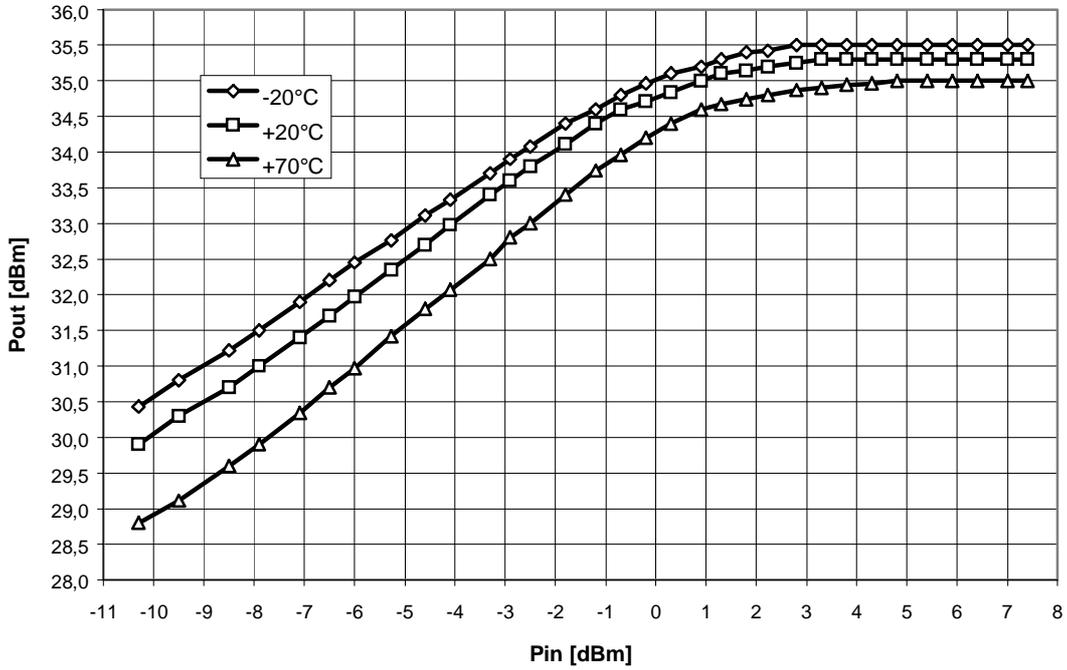
### Output Power vs. Drain Voltage

(matched for  $V_D=3.5V$ ,  $V_{control}=2.2V$ ,  $P_{in}=0dBm$ , duty cycle 12.5%,  $t_{on}=577\mu s$ )



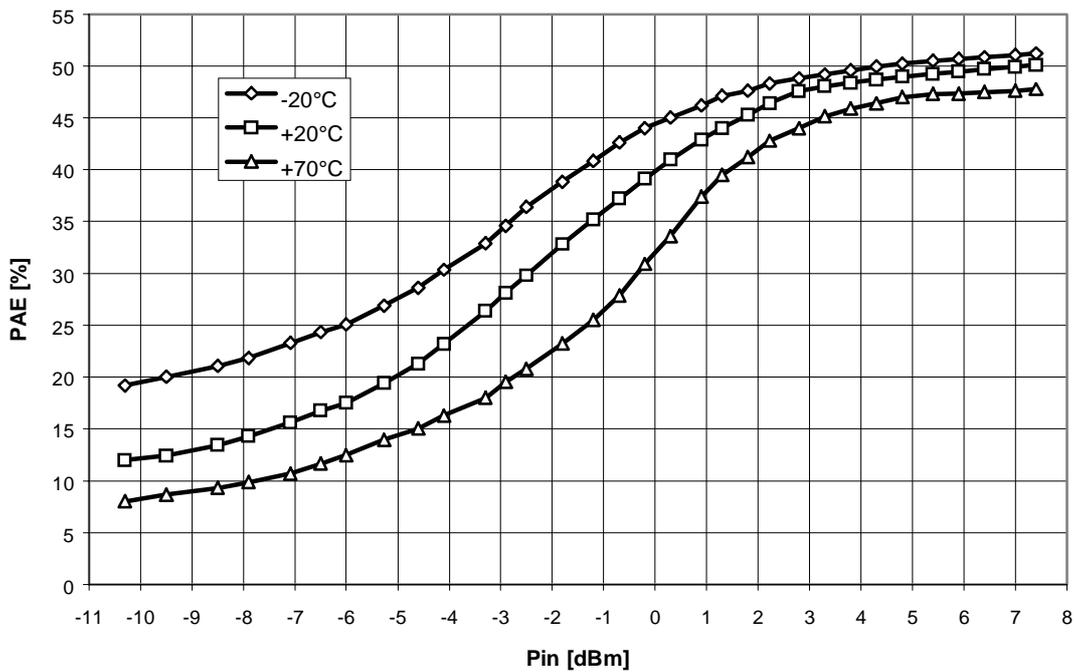
### Output Power at different Temperatures

( $V_d=3.5V$ ,  $V_{control}=2.2V$ ,  $f=900MHz$ , duty cycle 12.5%,  $t_{on}=577\mu s$ )

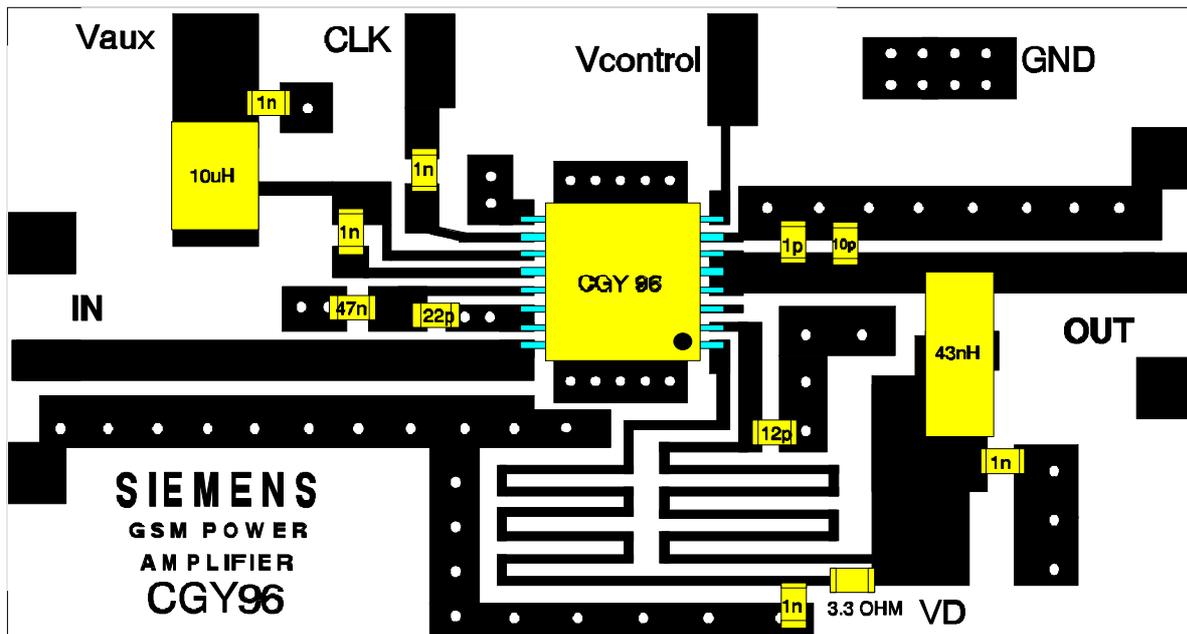


### PAE at different Temperatures

( $V_d=3.5V$ ,  $V_{control}=2.2V$ ,  $f=900MHz$ , duty cycle 12.5%,  $t_{on}=577\mu s$ )



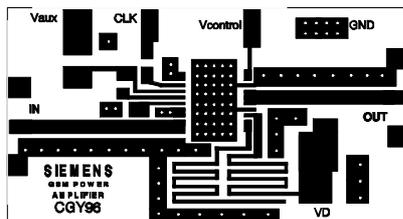
## CGY 96 Evaluation Board



(Size 53.0mm x 28.5mm)

**Notes:** -For maximum efficiency use high quality capacitors for the output matching: Part Number ACCU-P0603 distribution by  
AVX GmbH, 85757 Karlsfeld, Germany  
Phone-No ..8131/9004-0

-33nH SMD-Inductor for drain3: Part Number BV1250 distribution by  
Horst David GmbH, 85375 Neufarn, Germany  
Phone-No ..8165/9548-0 , Fax-No ..8165/9548-28

**Connections:**

- Vd 2.7 to 6VDC, pulsed (GSM: 12,5% duty cycle,  $t_{on}=0.577ms$ )
- Vaux 2.7 to 6VDC
- Vcontrol 0.2 to 2.2 VDC (0.2V: min Pout, 2.2V: max Pout)
- CLK 5 MHz to 15 MHz (with a 10uH inductor)  
or 150 kHz to 250 kHz (with a 100uH inductor instead of the 10uH)  
(rectangular signal, 50% duty, 0 Volt to Vd voltage level)

**Power on sequence:**

1. continuous clock (CLK) on
2. turn on Vaux ==> check negative voltage at pin#13 (-4.....-10V)
3. turn on Vcontrol (may be at the same time as 2)  
turn on Drainvoltage Vd  
turn on Input Power

**Operation without using the negative voltage generator:**

If you don't want to use the internal negative voltage generator, you can also apply -4....-6 V at pin#13 (C2-Pin). In this case the passive devices at the pins 9, 10, 11, 12 and 13 are not necessary (1 inductor and 5 capacitors).

