FAIRCHILD
SEMICONDUCTOR™

October 1987
Revised January 1999

CD4014BC
8-Stage Static Shift Register

General Description

The CD4014BC is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual JAM inputs to each of 8 stages. Q outputs are available from the sixth, seventh and eighth stages. All outputs have equal source and sink current capabilities and conform to standard "B" series output drive.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control input is in the logical "1" state, data is jammed into each stage of the register synchronously with the positive transition of the clock.

All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage:
  1 µA at 15V over full temperature range

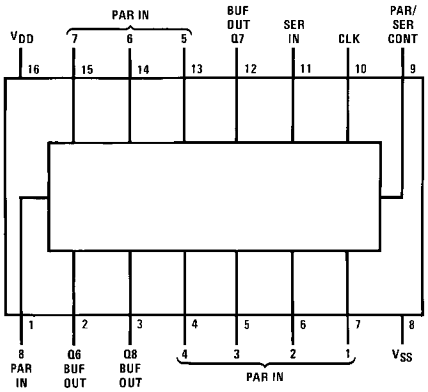
Ordering Code:

Order Number	Package Number	Package Description
CD4014BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4014BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "x" to the ordering code.

Connection Diagram

Pin Assignments for DIP



Top View

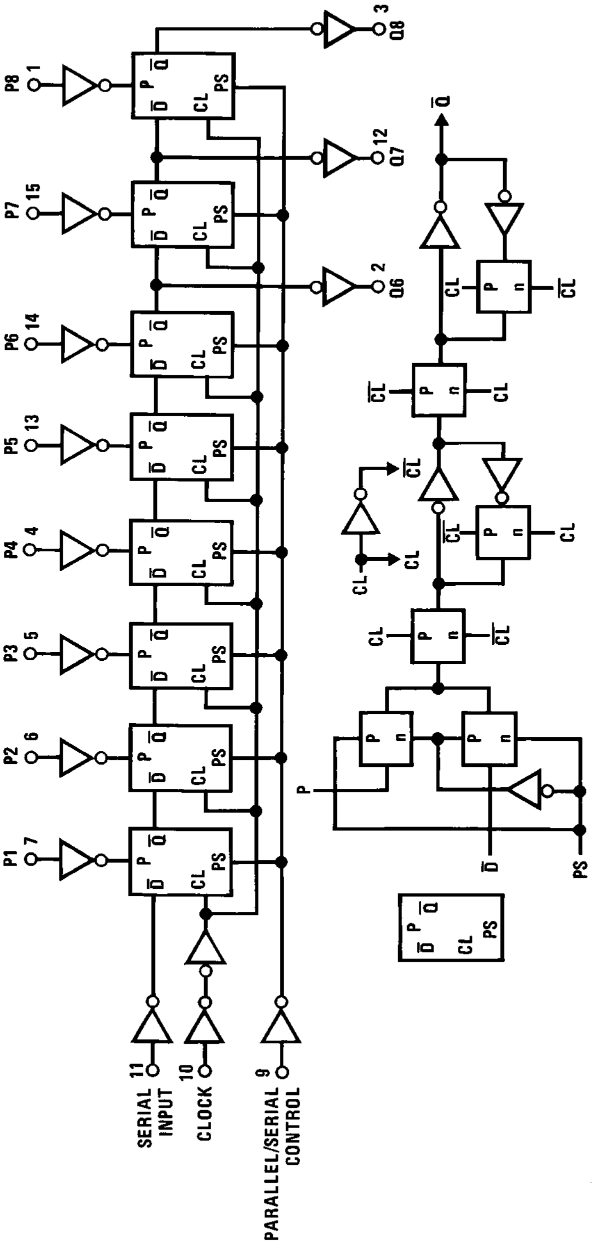
Truth Table

CL (Note 1)	Serial Input	Parallel/ Serial Control	PI 1	PI n	Q1 (Internal)	Q_n
↗	X	1	0	0	0	0
↗	X	1	1	0	1	0
↗	X	1	0	1	0	1
↗	X	1	1	1	1	1
↗	0	0	X	X	0	Q_{n-1}
↗	1	0	X	X	1	Q_{n-1}
↘	X	X	X	X	Q1	Q_n

X = Don't care case
No Change

Note 1: Level change

Logic Diagram



Absolute Maximum Ratings(Note 2)

(Note 3)

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5 to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 3)

Supply Voltage (V_{DD})	3.0V to 15V
Input Voltage (V_{IN})	0 to V_{DD}
Operating Temperature Range (T_A)	−40°C to +85°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 3: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions		−40°C		+25°C			+85°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}			20		0.1	20		150	µA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}			40		0.2	40		300	µA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}			80		0.3	80		600	µA
V_{OL}	LOW Level Output Voltage	V_{DD} = 5V	$\lvert I_O \rvert < 1$ µA		0.05		0	0.05		0.05	V
		V_{DD} = 10V			0.05		0	0.05		0.05	V
		V_{DD} = 15V			0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	V_{DD} = 5V	$\lvert I_O \rvert < 1$ µA	4.95		4.95	5		4.95		V
		V_{DD} = 10V		9.95		9.95	10		9.95		V
		V_{DD} = 15V		14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V			1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V			3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V			4.0		6	4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		11.0		11.0	9		11.0		V
I_{OL}	LOW Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V		0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V		1.3		1.1	2.2		0.9		mA
		V_{DD} = 15V, V_O = 1.5V		3.6		3.0	8		2.4		mA
I_{OH}	HIGH Level Output Current (Note 4)	V_{DD} = 5V, V_O = 4.6V		−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V		−1.3		−1.1	−2.2		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V		−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V			−0.3		-10^{-5}	−0.3		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V			0.3		10^{-5}	0.3		1.0	µA

Note 4: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics (Note 5)

$T_A = 25°C$, input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		200	320	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		60	120	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Input Frequency	$V_{DD} = 5V$	2.8	4		MHz
		$V_{DD} = 10V$	6	12		MHz
		$V_{DD} = 15V$	8	16		MHz
t_W	Minimum Clock Pulse Width	$V_{DD} = 5V$		90	180	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		25	50	ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time (Note 6)	$V_{DD} = 5V$			15	µs
		$V_{DD} = 10V$			15	µs
		$V_{DD} = 15V$			15	µs
t_S	Minimum Set-Up Time (Note 7) Serial Input $t_H \geq 200$ ns	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		30	60	ns
	Parallel Inputs $t_H \geq 200$ ns	$V_{DD} = 5V$		80	160	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		30	60	ns
	Parallel/Serial Control $t_H \geq 200$ ns	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_H	Minimum Hold Time Serial In, Parallel In, $t_S \geq 400$ ns Parallel/Serial Control	$V_{DD} = 5V$			0	ns
		$V_{DD} = 10V$			10	ns
		$V_{DD} = 15V$			15	ns
C_I	Average Input Capacitance (Note 8)	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 8)			110		pF

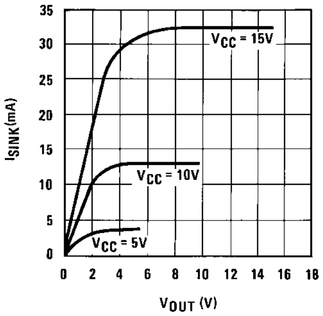
Note 5: AC Parameters are guaranteed by DC correlated testing.

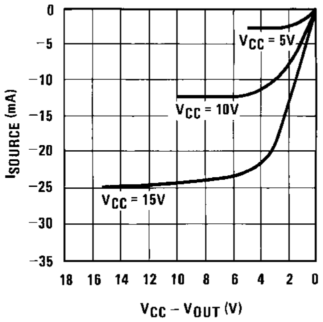
Note 6: If more than one unit is cascaded t_{rCL} should be made less than or equal to the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

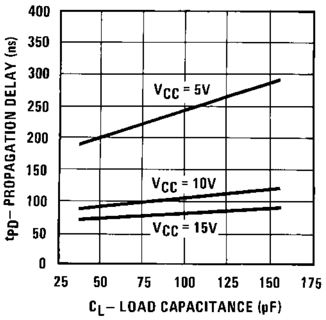
Note 7: Setup times are measured with reference to clock and a fixed hold time (t_H) as specified.

Note 8: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 74C family characteristics application note AN-90.

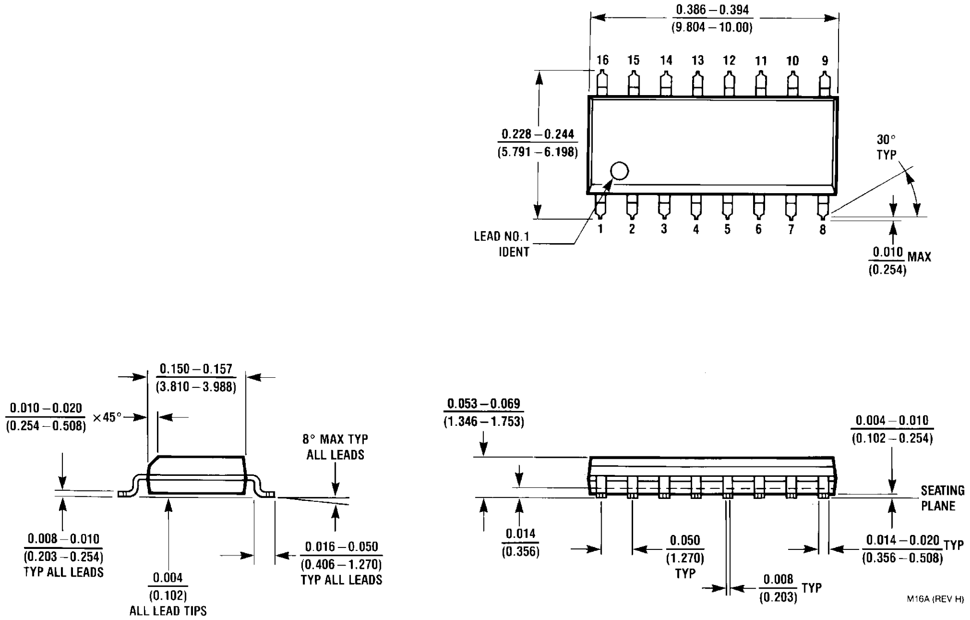
Typical Performance Characteristics





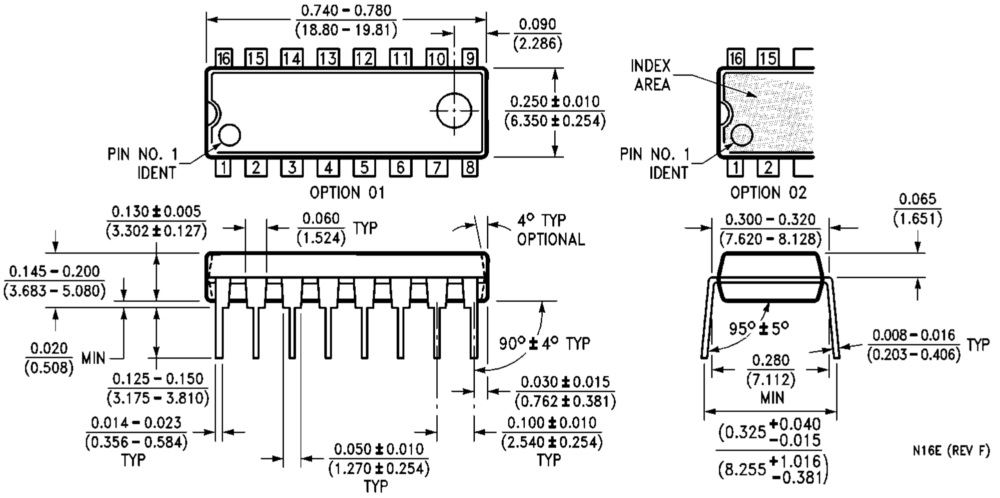


Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
Package Number N16E

LIFE SUPPORT POLICY

FAIRCHILD’S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com