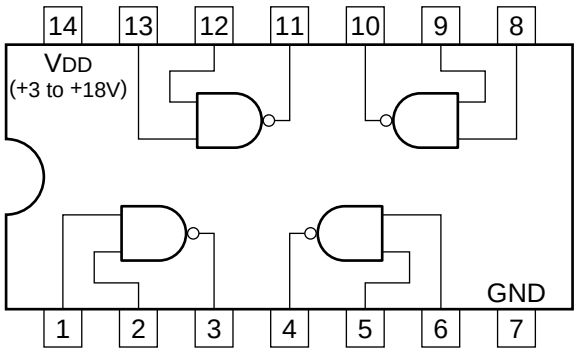
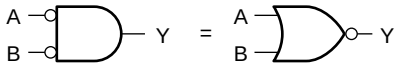
****

C-MOS 2-INPUT NAND GATE

-TOP VIEW-





$Y = \overline{A \cdot B} = \overline{A} + \overline{B}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

0 ; LOW LEVEL
1 ; HIGH LEVEL