

## CAT35C116/CAT35C116I

16K-Bit SERIAL E<sup>2</sup>PROM

### FEATURES

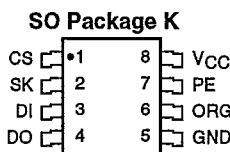
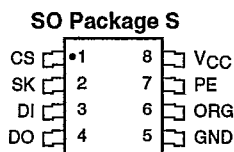
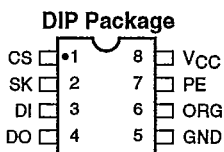
- High Speed Operation: 3MHz
- Low Power CMOS Technology
- Single 5V Supply
- 1024 x 16 or 2048 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Sequential Read
- Program Enable (PE) Pin
- Fast Nonvolatile Write Cycle: 5ms Max
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

### DESCRIPTION

The CAT35C116 and CAT35C116I are 16K bit Serial E<sup>2</sup>PROM memory devices which can be configured as either 1024 registers by 16 bits (ORG pin at V<sub>CC</sub>) or 2048 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C116/CAT35C116I is manufactured using

Catalyst's advanced CMOS E<sup>2</sup>PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

### PIN CONFIGURATION



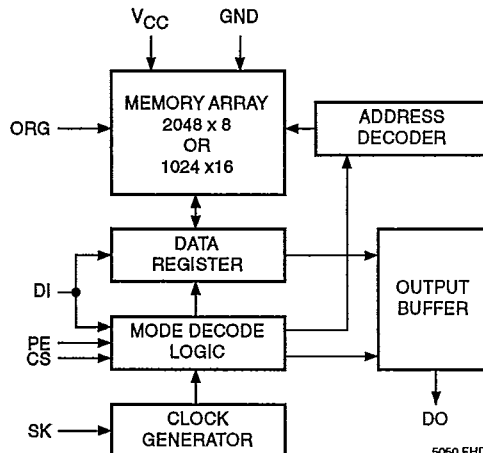
5050 FHD F01

### PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V <sub>CC</sub>	+5V Power Supply
GND	Ground
PE	Program Enable
ORG	Memory Organization

Note: When the ORG pin is connected to V<sub>CC</sub>, the 1024 x 16 organization is selected. When it is connected to ground, the 2048 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 1024 x 16 organization.

### BLOCK DIAGRAM



5050 FHD F02

TD 5050

## CAT35C116/CAT35C116I

## CATALYST SEMICONDUCTOR

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with Respect to Ground <sup>(1)</sup> .....	-2.0V to +V <sub>CC</sub> +2.0V
V <sub>CC</sub> with Respect to Ground .....	-2.0V to +7.0V
Package Power Dissipation Capability (T <sub>a</sub> = 25°C) .....	1.0W
Lead Soldering Temperature (10 secs) .....	300°C
Output Short Circuit Current <sup>(2)</sup> .....	100 mA

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

## RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
NEND <sup>(3)</sup>	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T <sub>DR</sub> <sup>(3)</sup>	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V <sub>ZAP</sub> <sup>(3)</sup>	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I <sub>LTH</sub> <sup>(3)(4)</sup>	Latch-Up	100		mA	JEDEC Standard 17

## D.C. OPERATING CHARACTERISTICS

CAT35C116 T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = +5V±10%, unless otherwise specified.

CAT35C116I T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = +5V±10%, unless otherwise specified.

Symbol	Parameter		Limits			Units	Test Conditions
			Min.	Typ.	Max.		
I <sub>CC1</sub>	Power Supply Current (Operating)	Comm.			3	mA	DI = 0.0V, SK = 5.0V V <sub>CC</sub> = 5.0V, CS = 5.0V, Output Open
		Ind.			4	mA	
I <sub>CC2</sub>	Power Supply Current (Standby)				10	μA	V <sub>CC</sub> = 5.5V, CS = 0V DI = 0V SK = 0V
I <sub>LI</sub> <sup>(5)</sup>	Input Leakage Current				1	μA	V <sub>IN</sub> = 0V to 5.5V
I <sub>LO</sub> <sup>(5)</sup>	Output Leakage Current				1	μA	V <sub>OUT</sub> = 0V to 5.5V, CS = 0V
V <sub>IH</sub>	High Level Input Voltage		2.0		V <sub>CC</sub> + 1	V	
V <sub>IL</sub>	Low Level Input Voltage		-0.1		0.8	V	
V <sub>OH</sub>	High Level Output Voltage		2.4			V	I <sub>OH</sub> = -400μA
V <sub>OL</sub>	Low Level Output Voltage				0.4	V	I <sub>OL</sub> = 2.1mA

## Note:

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> + 0.5V, which may overshoot to V<sub>CC</sub> + 2.0V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V<sub>CC</sub> + 1V.
- (5) PE and ORG pin leakage current (I<sub>LI</sub> and I<sub>LO</sub>) = 15 μA max. (at V<sub>IL</sub>), 10 μA otherwise.

## CATALYST SEMICONDUCTOR

## INSTRUCTION SET (6)

Inst.	Start Bit	Opcode	Address		Data		PE	Comments
			2048 x 8	1024 x 16	2048 x 8	1024 x 16		
READ	1	1 0	A10-A0	A9-A0			X	Start Address AN-A0
ERASE	1	1 1	A10-A0	A9-A0			1	Clear Address AN-A0
WRITE	1	0 1	A10-A0	A9-A0	D7-D0	D15-D0	1	Write Address AN-A0
EWEN	1	0 0	11XXXXXXXX	11XXXXXXXX			X	Write Enable
EWDS	1	0 0	00XXXXXXXX	00XXXXXXXX			X	Write Disable
ERAL	1	0 0	10XXXXXXXX	10XXXXXXXX			1	Clear All Addresses
WRAL	1	0 0	01XXXXXXXX	01XXXXXXXX	D7-D0	D15-D0	1	Write All Addresses

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## A.C. CHARACTERISTICS

CAT35C116  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.CAT35C116I  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{CSS}$	CS Setup Time	50			ns	$C_L = 100\text{pF}$ $V_{OL} = 0.8\text{V}, V_{OH} = 2.0\text{V}$ $V_L = 0.45\text{V}, V_{IH} = 2.4\text{V}$
$t_{CSH}$	CS Hold Time	0			ns	
$t_{DIS}$	DI Setup Time	50			ns	
$t_{DIH}$	DI Hold Time	50			ns	
$t_{PD1}$	Output Delay to 1			100	ns	
$t_{PD0}$	Output Delay to 0			100	ns	
$t_{HZ}^{(3)}$	Output Delay to High-Z			100	ns	
$t_{EW}^{(7)}$	Program/Erase Pulse Width			5	ms	
$t_{CSMIN}$	Minimum CS Low Time	100			ns	
$t_{SKHI}$	Minimum SK High Time	100			ns	
$t_{SKLOW}$	Minimum SK Low time	100			ns	
$t_{SV}$	Output Delay to Status Valid			100	ns	$C_L = 100\text{pF}$
$SK_{MAX}$	Maximum Clock Frequency	DC		3	MHz	

Note:

(3) This parameter is tested initially and after a design or process change that affects the parameter.

(6) X indicates a "Don't Care" input (either 0 or 1).

(7) ERAL and WRAL instructions = 10 ms max.

## DEVICE OPERATION

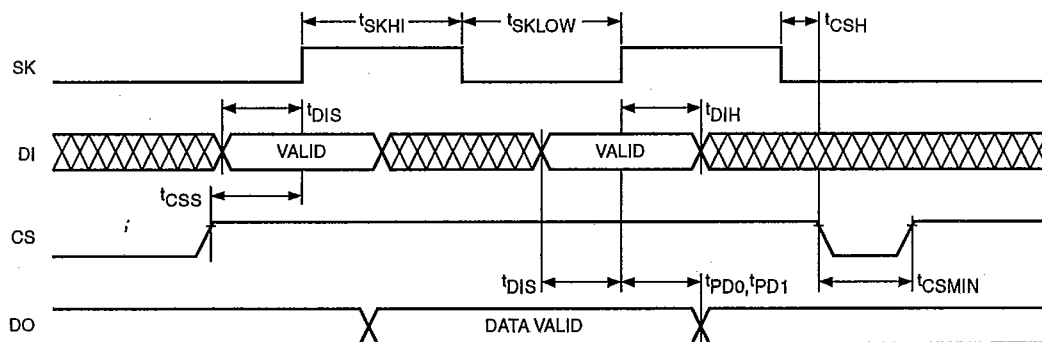
The CAT35C116/CAT35C116I is a 16,384 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT35C116/CAT35C116I can be organized as either 1024 registers by 16 bits, or as 2048 registers by 8 bits. Seven 13 bit instructions (14 bit instruction in 2048 by 8 organization) control the reading, writing and erase operations of the device. The CAT35C116/CAT35C116I operates on a single 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

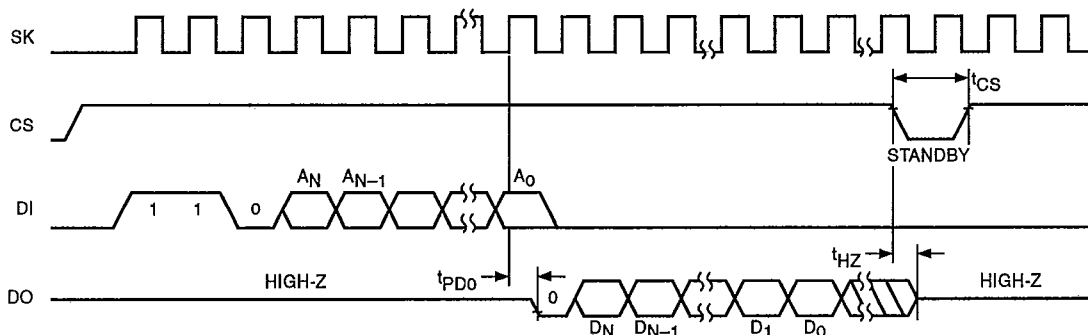
The format for all instructions sent to the CAT35C116/CAT35C116I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 10 bit address (11 bit address when organized as 2048 x 8), and for write operations a 16 bit data field

Figure 1. Synchronous Data Timing (8)



5041 FHD F03

Figure 2. Read Instruction Timing (8) (9)



5041 FHD F04

Note:

(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A10 and DN = D7. When x16 organization is selected, AN = A9 and DN = D15.

(9) PE = "Don't Care".

## CATALYST SEMICONDUCTOR

(8 bit data field when organized as 2048 x 8). All program/erase cycles are enabled only when pin 7 (PE) is held high.

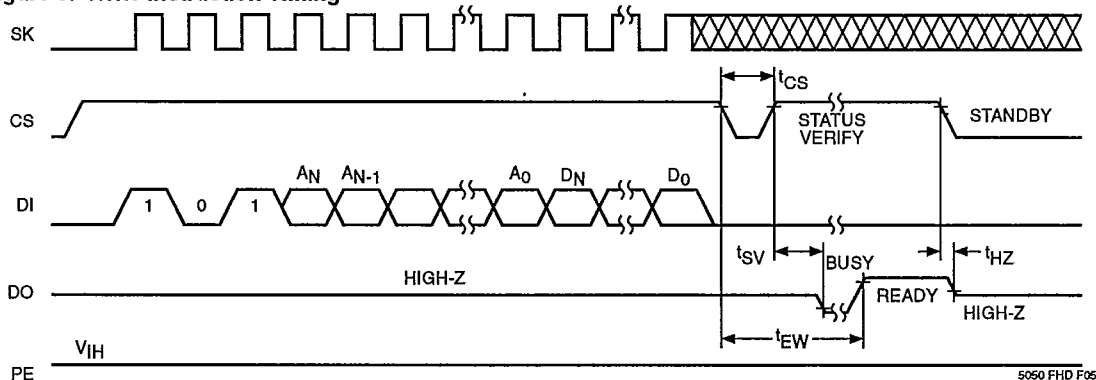
**Read**

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT35C116/CAT35C116I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ( $t_{PD0}$  or  $t_{PD1}$ ). The data output is sequential with the data from address N followed by the data from address N+1. The data output continues to the highest address and will wrap around to the first address if the clock continues to run. Bringing CS low at any time will stop the data output. The dummy

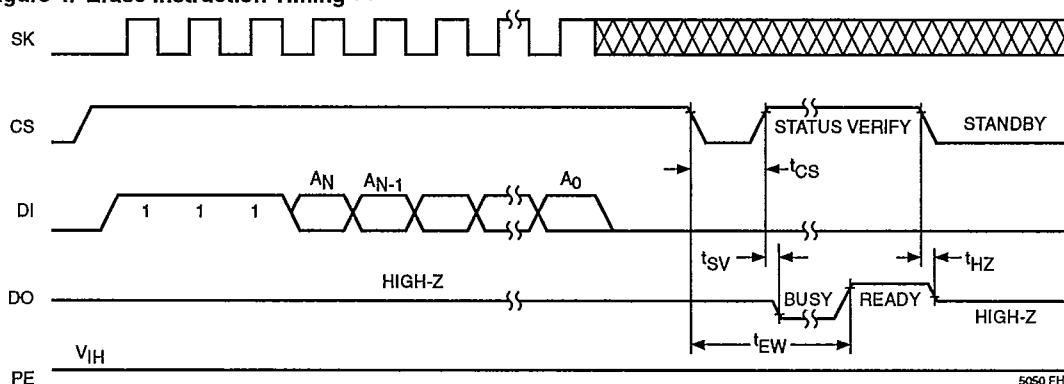
bit is suppressed in the sequential read mode (except for the very first address) and a continuous stream of data results.

**Write**

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 100ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C116/CAT35C116I can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent. The Write instruction requires that PE = 1.

**Figure 3. Write Instruction Timing (8)**

5050 FHD F05

**Figure 4. Erase Instruction Timing (8)**

5050 FHD F07

Note:

- (8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A10 and DN = D7. When x16 organization is selected, AN = A9 and DN = D15.

## CATALYST SEMICONDUCTOR

**Erase**

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 100ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C116/CAT35C116I can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state. The Erase instruction requires that PE = 1.

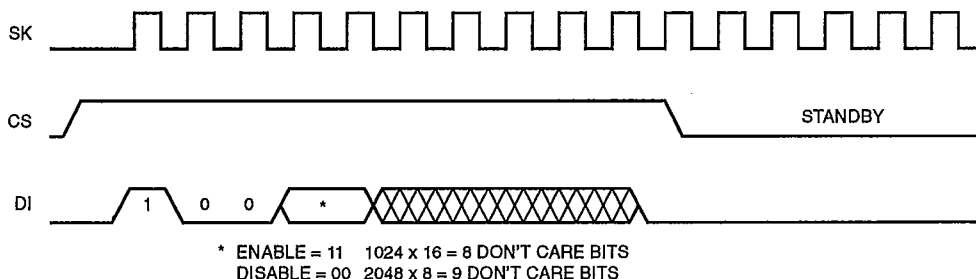
**Erase/Write Enable and Disable**

The CAT35C116/CAT35C116I powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write

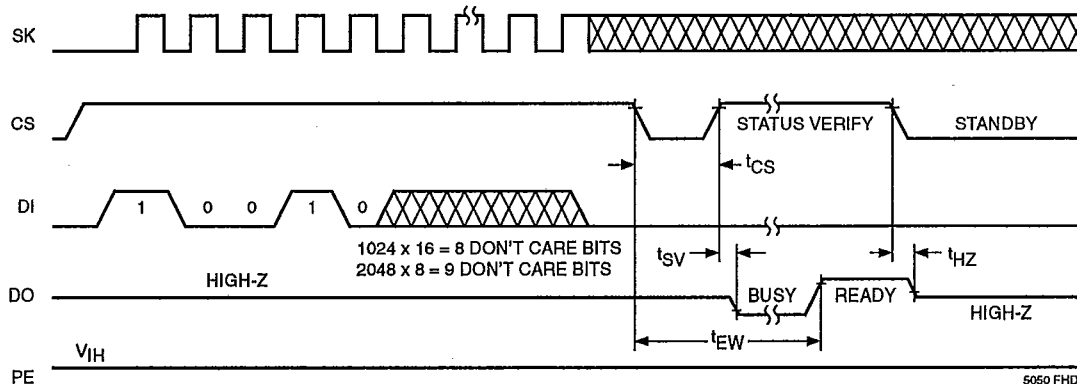
instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT35C116/CAT35C116I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

**Erase All**

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 100ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C116/CAT35C116I can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state. The Erase All instruction requires that PE = 1.

**Figure 5. EWEN/EWDS Instruction Timing (8) (9)**

5050 FHD F06

**Figure 6. ERAL Instruction Timing (8)**

5050 FHD F06

**Note:**

(8) The ORG pin is used to configure the device for x8 or x16 operation.

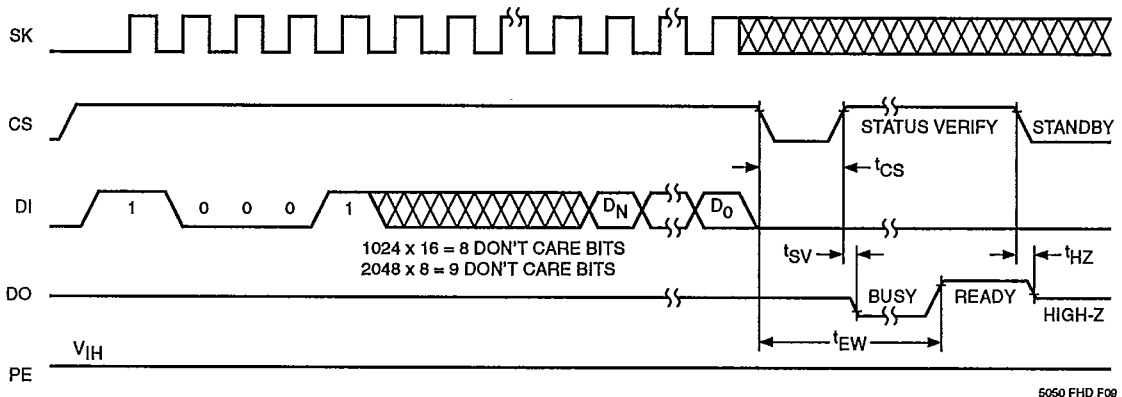
(9) PE = "Don't Care".

## Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 100ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the

device has entered the self clocking mode. The ready/busy status of the CAT35C116/CAT35C116I can be determined by selecting the device and polling the DO pin. It IS NOT necessary for all memory locations to be cleared before the WRAL command is executed. The Write All instruction requires that PE = 1.

Figure 7. WRAL Instruction Timing (8)



5050 FHD F09

### Note:

- (8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, DN = D7.  
When x16 organization is selected, DN = D15.