CAT24C163(16K), CAT24C083(8K)
CAT24C043(4K), CAT24C023(2K)

Supervisory Circuits with I²C Serial CMOS E²PROM, Precision Reset Controller and Watchdog Timer

FEATURES

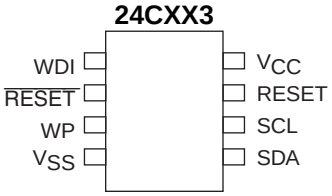
- **Watchdog Timer Input (WDI)**
- **Programmable Reset Threshold**
- **400 KHz I²C Bus Compatible**
- **2.7 to 6 Volt Operation**
- **Low Power CMOS Technology**
- **16 - Byte Page Write Buffer**
- **Built-in inadvertent write protection**
  - **— V_{CC} Lock Out**
- **Active High or Low Reset Outputs**
  - **— Precision Power Supply Voltage Monitoring**
  - **— 5V, 3.3V and 3V options**
- **1,000,000 Program/Erase Cycles**
- **100 Year Data Retention**
- **8-Pin DIP or 8-Pin SOIC**
- **Commercial, Industrial and Automotive Temperature Ranges**

DESCRIPTION

The CAT24CXX3 is a single chip solution to three popular functions of EEPROM memory, precision reset controller and watchdog timer. The 24C163(16K), 24C083(8K), 24C043(4K) and 24C023(2K) feature a I²C Serial CMOS EEPROM Catalyst advanced CMOS technology substantially reduces device power requirements. The 24CXX3 features a 16-byte page and is available in 8-pin DIP or 8-pin SOIC packages.

The reset function of the 24CXX3 protects the system during brown out and power up/down conditions. During system failure the watchdog timer feature protects the microcontroller with a reset signal. 24CXX3 features active low reset on pin 2 and active high reset on pin 7. 24CXX3 features watchdog timer on the WDI input pin (pin 1).

PIN CONFIGURATION

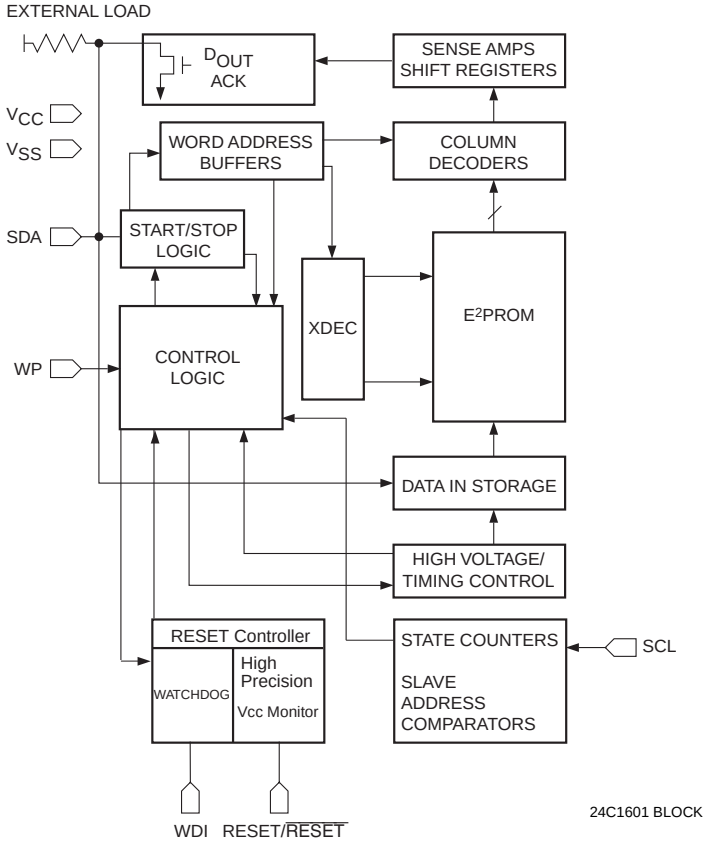


*All products offered in P and J packages

PIN FUNCITONS

Pin Name	Function
SDA	Serial Data/Address
RESET/$\overline{\text{RESET}}$	Reset I/O
SCL	Clock Input
Vcc	Power Supply
NC	No Connect
V_{SS}	Ground
WDI	Watchdog Timer Input
WP	Write Protect

BLOCK DIAGRAM



24C1601 BLOCK

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias.....–55°C to +125°C

Storage Temperature..... –65°C to +150°C

Voltage on Any Pin with
Respect to Ground(1) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground.....–2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C)1.0W.....1.0W

Lead Soldering Temperature (10 secs).....300°C

Output Short Circuit Current(2) 100mA

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +2.7V to +6.0V, unless otherwise specified.

		Limits				
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
Isb	Standby Current			40	µA	Vcc=3.3V
				50	µA	Vcc=5
I_{LI}	Input Leakage Current			2	µA	V_{IN}=G_{ND} or V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{IN}=G_{ND} or V_{CC}
V_{IL}	Input Low Voltage	–1		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (SDA)			0.4	V	I_{OL} = 3 mA, V_{CC} = 3.0V

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

A.C. CHARACTERISTICS

V_{CC}=2.7V to 6.0V unless otherwise specified.
Output Load is 1 TTL Gate and 100pF

Read & Write Cycle Limits

Symbol	Parameter	V_{CC}=2.7V - 6V		V_{CC}=4.5V - 5.5V		
		Min.	Max.	Min.	Max.	Units
F_{SCL}	Clock Frequency		100		400	kHz
T_I(1)	Noise Suppression Time Constant at SCL, SDA Inputs		200		200	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5		1	µs
t_{BUF}(1)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.2		µs
$t_{HD:STA}$	Start Condition Hold Time	4		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.2		µs
t_{HIGH}	Clock High Period	4		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		ns
$t_{SU:DAT}$	Data In Setup Time	50		50		ns
t_R(1)	SDA and SCL Rise Time		1		0.3	µs
t_F(1)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4		0.6		µs
t_{DH}	Data Out Hold Time	100		100		ns

Power-Up Timing(1)(2)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

RESET CIRCUIT CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units
t_{GLITCH}	Glitch Reject Pulse Width		100	ns
V_{RT}	Reset Threshold Hystersis	15		mV
V_{OLRS}	Reset Output Low Voltage (I_{OLRS}=1mA)		0.4	V
V_{OHRS}	Reset Output High Voltage	Vcc-0.75		V
V_{TH}	Reset Threshold (Vcc=5V) (24CXXX-45)	4.50	4.75	V
	Reset Threshold (Vcc=5V) (24CXXX-42)	4.25	4.50	
	Reset Threshold (Vcc=3.3V) (24CXXX-30)	3.00	3.15	
	Reset Threshold (Vcc=3.3V) (24CXXX-28)	2.85	3.00	
	Reset Threshold (Vcc=3V) (24CXXX-25)	2.55	2.70	
t_{PURST}	Power-Up Reset Timeout	130	270	ms
t_{RPD}	V_{TH} to RESET Output Delay		5	µs
V_{RVALID}	RESET Output Valid	1		V

PIN DESCRIPTIONS

WDI: WATCHDOG INPUT
If there is no transition on the WDI for more than 1.6 seconds, the watchdog timer times out.

WP: WRITE PROTECT
If the pin is tied to V_{CC} the entire memory array becomes Write Protected (READ only). When the pin is tied to V_{SS} or left floating normal read/write operations are allowed to the device.

SCL: SERIAL CLOCK
The serial clock input clocks all data transferred into or out of the device.

RESET/$\overline{\text{RESET}}$: RESET I/O
These are open drain pins and can be used as reset trigger inputs. By forcing a reset condition on the pins the device will initiate and maintain a reset condition. RESET pin must be connected through a pull-down and $\overline{\text{RESET}}$ pin must be connected through a pull-up device.

SDA: SERIAL DATA/ADDRESS
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

DEVICE OPERATION

Reset Controller Description

The CAT24CXXX provides a precision RESET controller that ensures correct system operation during brown-out and power up/down conditions. It is configured with open drain RESET outputs. During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TH} threshold and will continue driving the outputs for approximately 200ms (t_{PURST}) after reaching $V_{TH.}$ After the t_{PURST} timeout interval, the device will cease to drive reset outputs. At this point the reset outputs will be pulled up or down by their respective pull up/pull down devices. During power-down, the RESET outputs will begin driving active when V_{CC} falls below $V_{TH.}$ The RESET outputs will be valid so long as V_{CC} is >1.0V (V_{RVALID}).

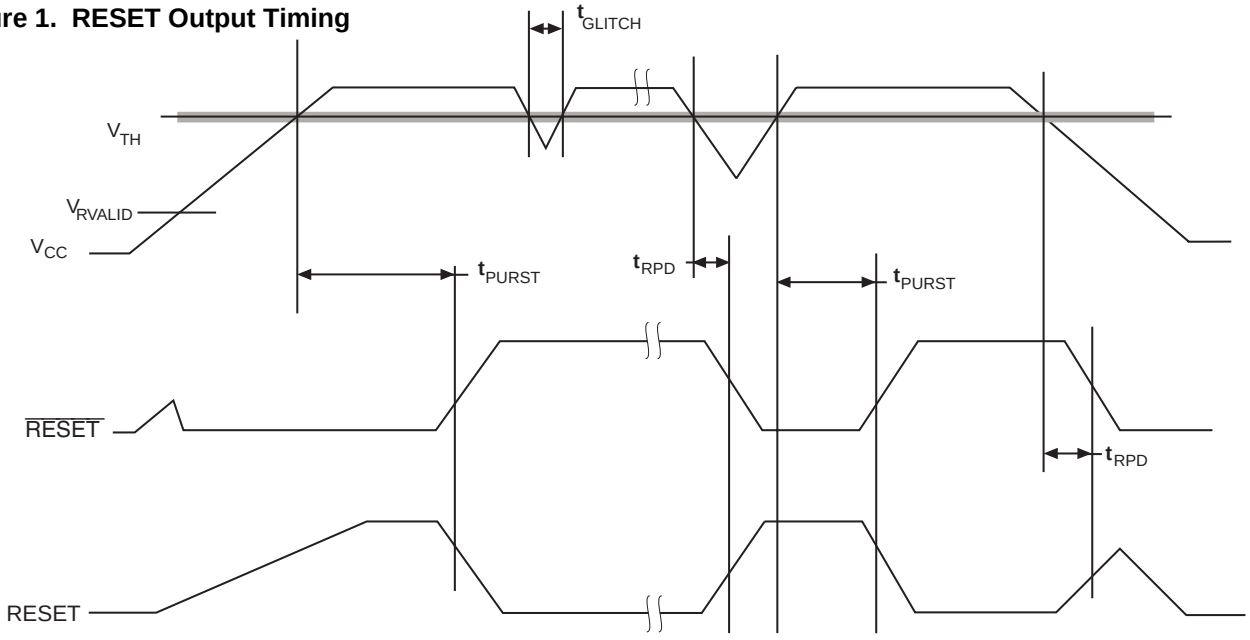
The RESET pins are I/Os; therefore, the CAT24CXXX can act as a signal conditioning circuit for an externally applied reset. The inputs are level triggered; that is, the RESET input in the 24CXXX will initiate a reset timeout after detecting a high and the $\overline{\text{RESET}}$ input in the 24CXXX will initiate a reset timeout after detecting a low.

Watchdog Timer

The Watchdog Timer provides an independent protection for microcontrollers. During a system failure, the CAT24CXXX will respond with a reset signal after a time-out interval of 1.6 seconds for a lack of activity. The 24CXX3 is designed with a WDI input pin for the Watchdog Timer function. For the 24CXX3, if the microcontroller does not toggle the WDI input pin within 1.6 seconds, the Watchdog Timer times out. This will generate a reset condition on reset outputs. The Watchdog Timer is cleared by any transition on WDI.

As long as the reset signal is asserted, the Watchdog Timer will not count and will stay cleared.

Figure 1. RESET Output Timing



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Hardware Data Protection

The 24CXXX is designed with the following hardware data protection features to provide a high degree of data integrity.

(1) The 24CXXX features a WP pin. When WP pin is tied high the entire memory array becomes write protected (read only).

(2) The V_{CC} sense provides write protection when V_{CC} falls below the reset threshold value (V_{TH}). The V_{CC} lock out inhibits writes to the serial EEPROM whenever V_{CC} falls below (power down) V_{TH} or until V_{CC} reaches the reset threshold (power up) V_{TH}.

Reset Threshold Voltage

From the factory the 24CXXX is offered in five different variations of reset threshold voltages. They are 4.50-4.75V, 4.25-4.50V, 3.00-3.15V, 2.85-3.00V and 2.55-2.70V. To provide added flexibility to design engineers using this product, the 24CXXX is designed with an additional feature of programming the reset threshold voltage. This allows the user to change the existing reset threshold voltage to one of the other four reset threshold voltages. Once the reset threshold voltage is selected it will not change even after cycling the power, unless the user uses the programmer to change the reset threshold voltage. However, the programming function is available only through third party programmer manufacturers. Please call Catalyst for a list of programmer manufacturers who support this function.

Figure 2. Bus Timing

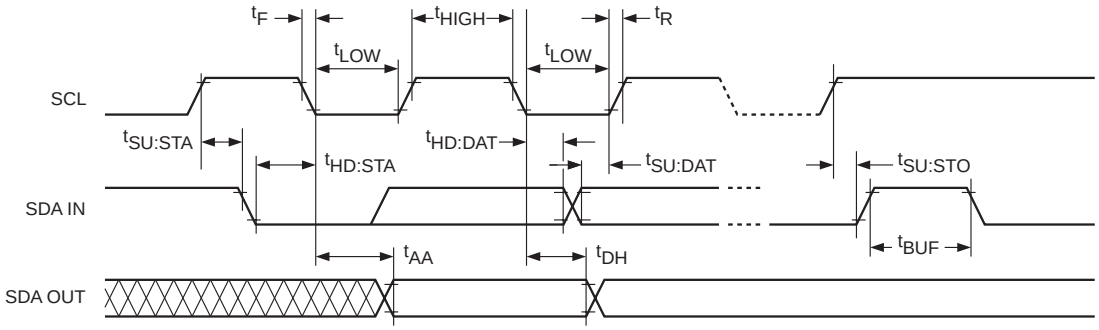


Figure 3. Write Cycle Timing

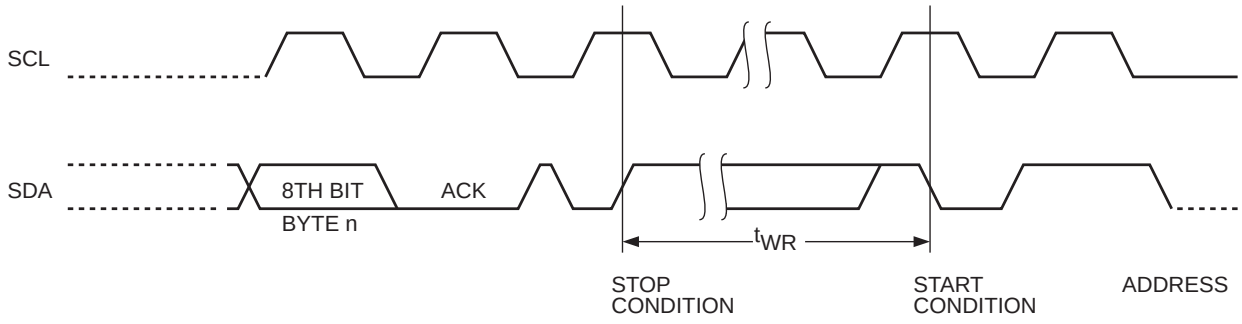
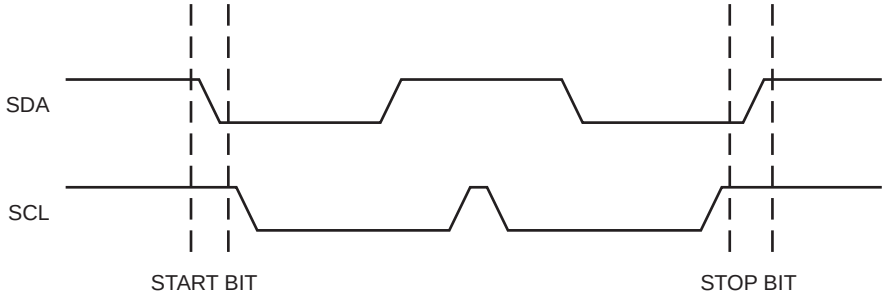


Figure 4. Start/Stop Timing



FUNCTIONAL DESCRIPTION

The CAT24CXXX supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24CXXX operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^2C BUS PROTOCOL

The features of the I^2C bus protocol are defined as follows:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24CXXX monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The Master begins a transmission by sending a START condition. The Master sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010.

The next three bits (Fig. 6) define memory addressing. For the 24C023, the three bits are don't care. For the 24C043, the next two bits are don't care and the third bit is the high order address bit. For the 24C083, the next bit is don't care and the successive bits define the higher order address bits. For the 24C163 the three bits define higher order bits.

The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT24CXXX monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24CXXX then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

Figure 5. Acknowledge Timing

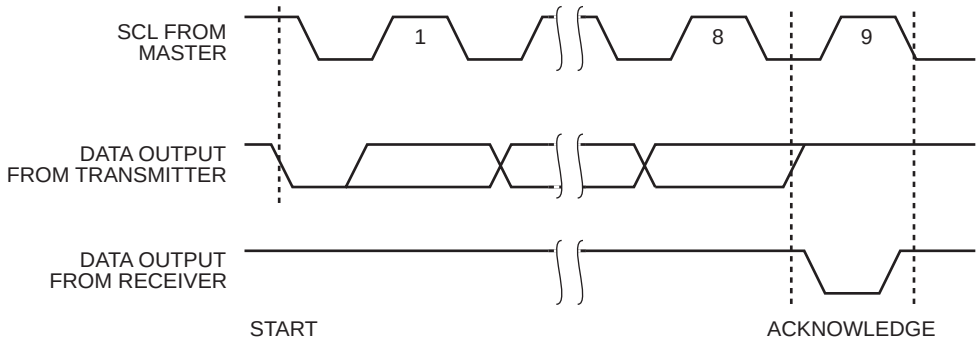


Figure 6. Slave Address Bits

24C023	1	0	1	0	X	X	X	R/$\overline{W}$
24C043	1	0	1	0	X	X	a8	R/$\overline{W}$
24C083	1	0	1	0	X	a9	a8	R/$\overline{W}$
24C163	1	0	1	0	a10	a9	a8	R/$\overline{W}$

* 'X' Corresponds to Don't Care Bits (can be a zero or a one)
** a8, a9 and a10 correspond to the address of the memory array address word.

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ACKNOWLEDGE

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT24CXXX responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT24CXXX begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24CXXX will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After t he Slave generates an acknowledge, the Master sends a 8-bit address that is to be written into the address pointers of the CAT24CXXX. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT24CXXX acknowledges once more and the Master generates the STOP condition. At this time, the device begins an internal programming cycle to nonvolatile memory. While the cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The 24CXXX writes up to 16 bytes of data in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted, CAT24CXXX will respond with an acknowledge, and internally increment the lower order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 16 bytes before sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

When all 16 bytes are received, and the STOP condi tion has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the CAT24CXXX in a single write cycle.

Figure 7. Byte Write Timing

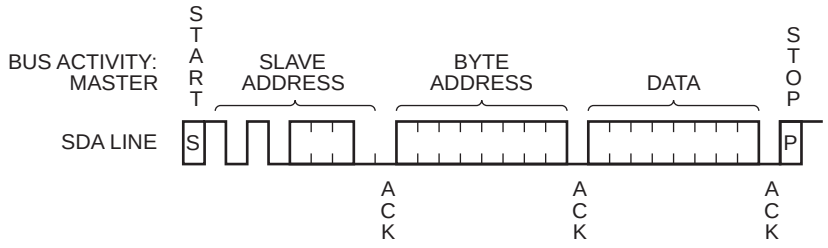
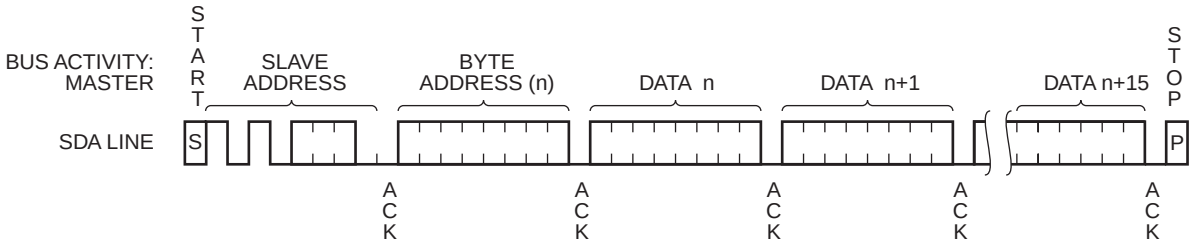


Figure 8. Page Write Timing



Acknowledge Polling

Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, CAT24CXXX initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If CAT24CXXX is still busy with the write operation, no ACK will be returned. If CAT24CXXX has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

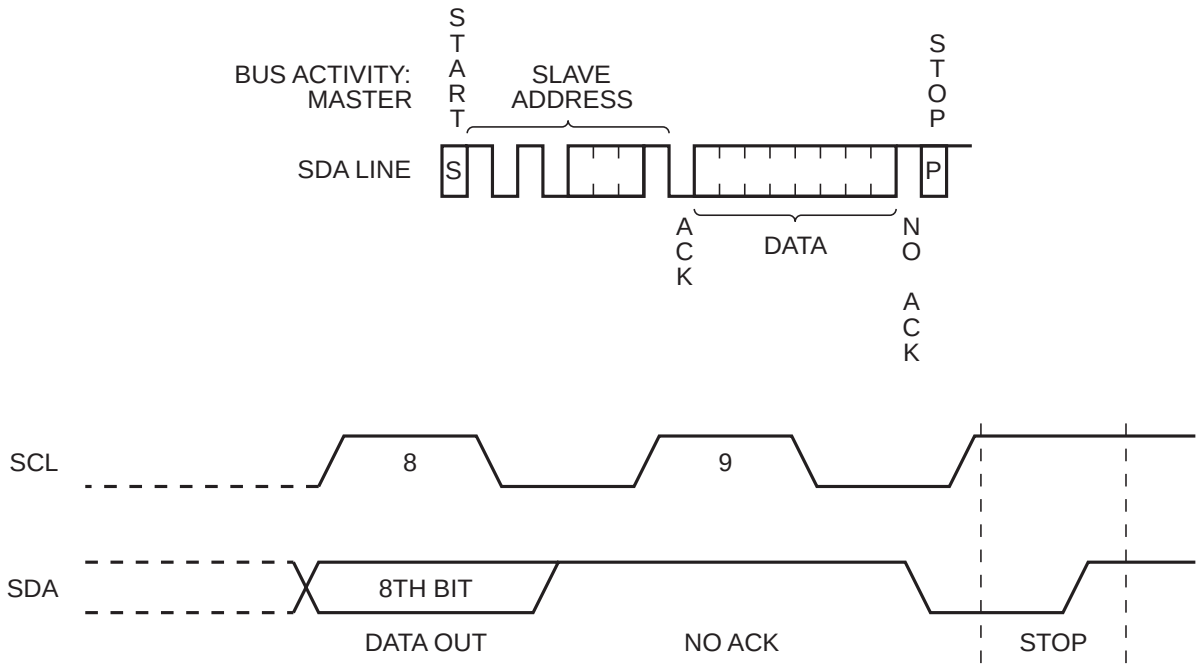
WRITE PROTECTION

The Write Protection feature allows the user to protect against inadvertent programming of the memory array. If the WP pin is tied to V_{CC}, the entire memory array is protected and becomes read only. The CAT24CXXX will accept both slave and byte addresses, but the memory location accessed is protected from programming by the device's failure to send an acknowledge after the first byte of data is received.

READ OPERATIONS

The READ operation for the CAT24CXXX is initiated in the same manner as the write operation with one exception, that R/$\overline{W}$ bit is set to one. Three different READ operations are possible: Immediate/Current Address READ, Selective/Random READ and Sequential READ.

Figure 9. Immediate Address Read Timing



24C1601Fig.8

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Immediate/Current Address Read

The CAT24CXXX's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=E (where E= 255 for 24C023, E=511 for 24C043, E=1023 for 24C083 and E=2047 for 24C163) then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24CXXX receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8-bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

Selective/Random Read

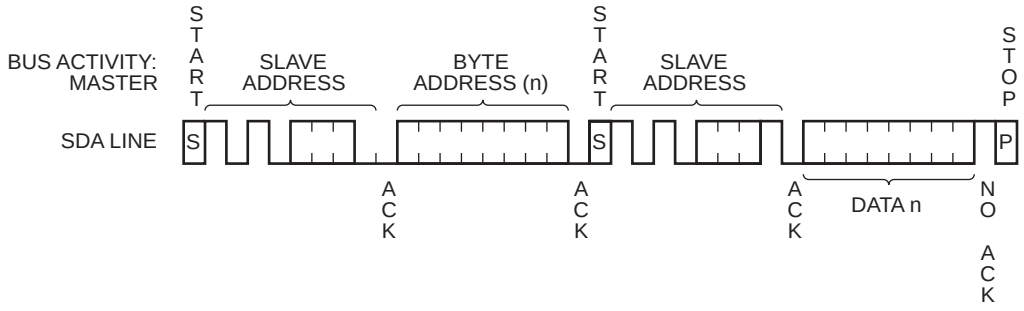
Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After CAT24CXXX acknowledges, the Master device sends the START condition and the slave address again, this time with the R/$\overline{W}$ bit set to one. The CAT24CXXX then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24CXXX sends the initial 8-bit byte requested, the Master will respond with an ac knowledge which tells the device it requires more data. The CAT24CXXX will continue to output an 8-bit byte for each acknowledge sent by the Master. The operation will terminate when the Master fails to respond with an acknowledge, thus sending the STOP condition.

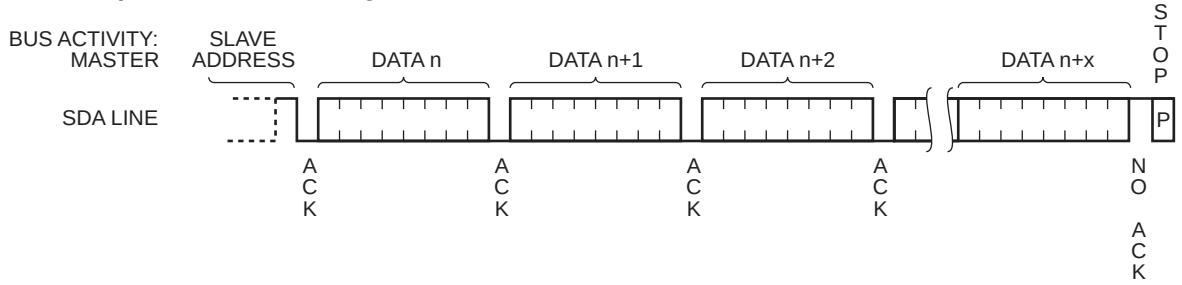
The data being transmitted from CAT24CXXX is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24CXXX address bits so that the entire memory array can be read during one operation. If more than E (where E= 255 for 24C023, E=511 for 24C043, E=1023 for 24C083 and E=2047 for 24C163) bytes are read out, the counter will 'wrap around' and continue to clock out data bytes.

Figure 10. Selective Read Timing



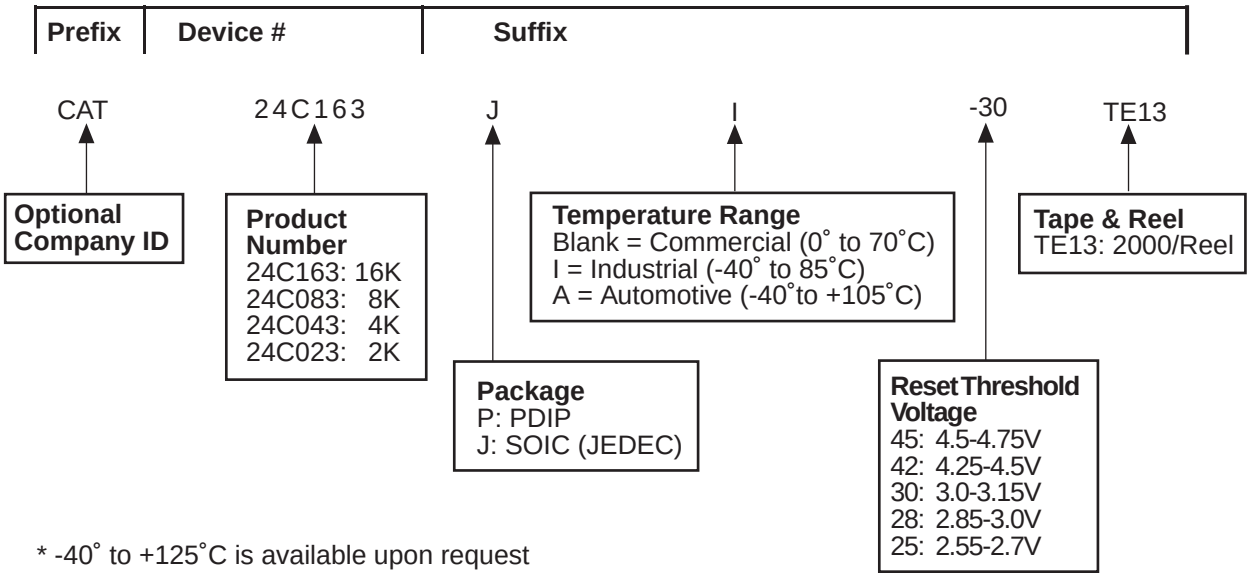
24C1601Fig.9

Figure 11. Sequential Read Timing



24C1601Fig.10

Ordering Information



Note:

(1) The device used in the above example is a CAT24C163JI-30TE13 (16K I²C Memory, SOIC, Industrial Temperature, 3.0-3.15V Reset Threshold Voltage, Tape and Reel)