HARRIS SEMICONDUCTOR

CA3018

March 1993

General Purpose Transistor Arrays

Features

- **Matched Monolithic General Purpose Transistors**
- **h_{FE} Matched** . . . . . **±10%**
- **V_{BE} Matched**
  - **CA3018A** . . . . . **±2mV**
  - **CA3018** . . . . . **±5mV**
- **Operation From DC to 120MHz**
- **Wide Operating Current Range**
- **CA3018A Performance Characteristics Controlled from 10μA to 10mA**
- **Low Noise Figure . . . . . 3.2dB Typical at 1kHz**
- **Full Military Temperature Range . . . . -55°C to +125°C**

Applications

- **Two Isolated Transistors and a Darlington Connected Transistor Pair for Low Power Applications at Frequencies from DC through the VHF Range**
- **Custom Designed Differential Amplifiers**
- **Temperature Compensated Amplifiers**
- **See Application Note, AN5296 "Application of the CA3018 Integrated Circuit Transistor Array" for Suggested Applications**

Description

The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

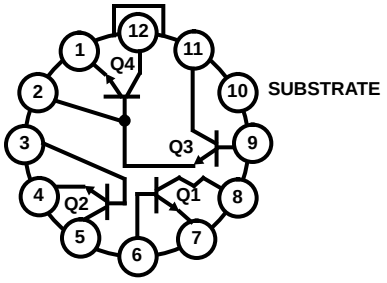
The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3018	-55°C to +125°C	12 Pin CAN
CA3018A	-55°C to +125°C	12 Pin CAN

Pinout

CA3018, CA3018A
(TO-5 CAN)
TOP VIEW



File Number **338.2**

Absolute Maximum Ratings (T_A = +25°C)

	CA3018	CA3018A
Collector-to-Emitter Voltage, V_{CEO}	15V	15V
Collector-to-Base Voltage, V_{CBO}	20V	30V
Collector-to-Substrate Voltage, V_{CIO} (Note 1)	20V	40V
Emitter-to-Base Voltage, V_{EBO}	5V	5V
Collector Current, I_C	50mA	50mA
Power Dissipation		
Any One Transistor	300mW	
Total Package	450mW	
T_A > +85°C	Derate at 5mW/°C	
Junction Temperature	+175°C	
Lead Temperature (Soldering 10 Sec.)	+300°C	

Operating Conditions

Operating Temperature Range . . . . . -55°C ≤ T_A ≤ +125°C
Storage Temperature Range . . . . . -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS						UNITS
				CA3018			CA3018A			
				MIN	TYP	MAX	MIN	TYP	MAX	
STATIC CHARACTERISTICS										
Collector Cutoff Current (Figure 1)	I_{CBO}	V_{CB} = 10V, I_E = 0		-	0.002	100	-	0.002	40	nA
Collector Cutoff Current (Figure 2)	I_{CEO}	V_{CE} = 10V, I_B = 0		-	See Fig. 2	5	-	See Fig. 2	0.5	µA
Collector Cutoff Current Darlington Pair	I_{CEOD}	V_{CE} = 10V, I_B = 0		-	-	-	-	-	5	µA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		15	24	-	15	24	-	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10µA, I_E = 0		20	60	-	30	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10µA, I_C = 0		5	7	-	5	7	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10µA, I_{CI} = 0		20	60	-	40	60	-	V
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1mA, I_C = 10mA		-	0.23	-	-	0.23	0.5	V
Static Forward Current Transfer Ratio (Note 2) (Figure 3)	h_{FE}	V_{CE} = 3V	I_C = 10mA	-	100	-	50	100	-	-
			I_C = 1mA	30	100	200	60	100	200	-
			I_C = 10µA	-	54	-	30	54	-	-
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2) (Figure 3)		V_{CE} = 3V, I_{C1} = I_{C2} = 1mA		0.9	0.97	-	0.9	0.97	-	-
Static Forward Current Transfer Ratio Darlington Pair (Q3 and Q4) (Figure 4)	h_{FED}	V_{CE} = 3V	I_C = 1mA	1500	5400	-	2000	5400	-	-
			I_C = 100µA	-	-	-	1000	2800	-	-
Base-to-Emitter Voltage (Figure 5)	V_{BE}	V_{CE} = 3V	I_E = 1mA	-	0.715	-	0.600	0.715	0.800	V
			I_E = 10mA	-	0.800	-	-	0.800	0.900	V
Input Offset Voltage (Figures 5, 7)	$\lvert V_{BE1} \rvert$ $\lvert -V_{BE2} \rvert$	V_{CE} = 3V, I_E = 1mA		-	0.48	5	-	0.48	2	mV

Electrical Specifications $T_A = +25^oC$ (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS CA3018 MIN	CA3018 TYP	CA3018 MAX	CA3018A MIN	CA3018A TYP	CA3018A MAX	UNITS
Temperature Coefficient: Base-to-Emitter Voltage Q_1, Q_2 (Figure 6)	$\frac{\lvert\Delta V_{BE}\rvert}{\Delta T}$	V_{CE} = 3V, I_E = 1mA	-	-1.9	-	-	-1.9	-	mV/°C
Base (Q3)-to-Emitter (Q4) Voltage Darlington Pair (Figure 8)	V_{BED} (V_{9-1})	V_{CE} = 3V, I_E = 10mA	-	1.46	-	-	1.46	1.60	V
		I_E = 1mA	-	1.32	-	1.10	1.32	1.50	V
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair (Q3 and Q4) (Figure 9)	$\frac{\lvert\Delta V_{BED}\rvert}{\Delta T}$	V_{CE} = 3V, I_E = 1mA	-	4.4	-	-	4.4	-	mV/°C
Temperature Coefficient: Magnitude of Input Offset Voltage	$\frac{\lvert V_{BE1} - V_{BE2}\rvert}{\Delta T}$	V_{CC} = 6V, V_{EE} = -6V, $I_{C1} = I_{C2}$ = 1mA	-	10	-	-	10	-	µV/°C
DYNAMIC CHARACTERISTICS									
Low Frequency Noise Figure (Figures 10 - 12)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100µA, Source Resistance = 1kΩ	-	3.25	-	-	3.25	-	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics									
Forward Current Transfer Ratio (Figure 13)	h_{FE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	110	-	-	110	-	-
Short Circuit Input Impedance (Figure 13)	h_{IE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	3.5	-	-	3.5	-	kΩ
Open Circuit Output Impedance (Figure 13)	h_{OE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	15.6	-	-	15.6	-	µmho
Open Circuit Reverse Voltage Transfer Ratio (Figure 13)	h_{RE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	1.8×10^{-4}	-	-	1.8×10^{-4}	-	-
Admittance Characteristics									
Forward Transfer Admittance (Figure 14)	Y_{FE}	f = 1MHz, V_{CE} = 3V, I_C = 1mA	-	31 - j1.5	-	-	31 - j1.5	-	mmho
Input Admittance (Figure 15)	Y_{IE}	f = 1MHz, V_{CE} = 3V, I_C = 1mA	-	0.3 + j0.04	-	-	0.3 + j0.04	-	mmho
Output Admittance (Figure 16)	Y_{OE}	f = 1MHz, V_{CE} = 3V, I_C = 1mA	-	0.001 + j0.03	-	-	0.001 + j0.03	-	mmho
Reverse Transfer Admittance (Figure 17)	Y_{RE}	f = 1MHz, V_{CE} = 3V, I_C = 1mA	See Figure 17						mmho
Gain Bandwidth Product (Figure 18)	f_T	V_{CE} = 3V, I_C = 3mA	300	500	-	300	500	-	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3V, I_E = 0	-	0.6	-	-	0.6	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3V, I_C = 0	-	0.58	-	-	0.58	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 3V, I_C = 0	-	2.8	-	-	2.8	-	pF

NOTE:

1. The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. The substrate (Terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. Actual forcing current is via the emitter for this test.

Typical Performance Curves

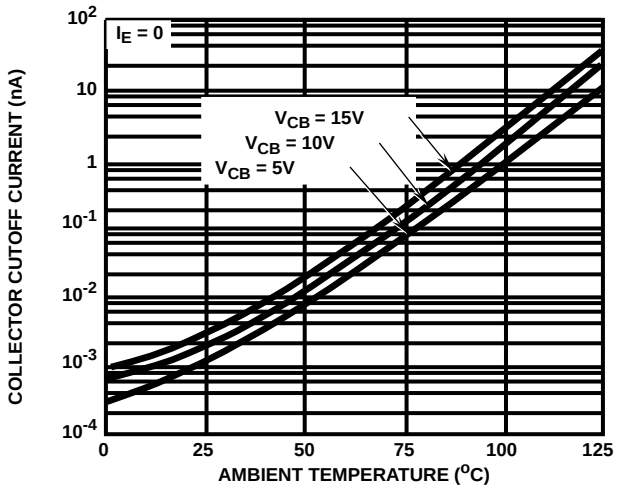


FIGURE 1. TYPICAL COLLECTOR-TO-BASE CUTOFF CURRENT vs TEMPERATURE

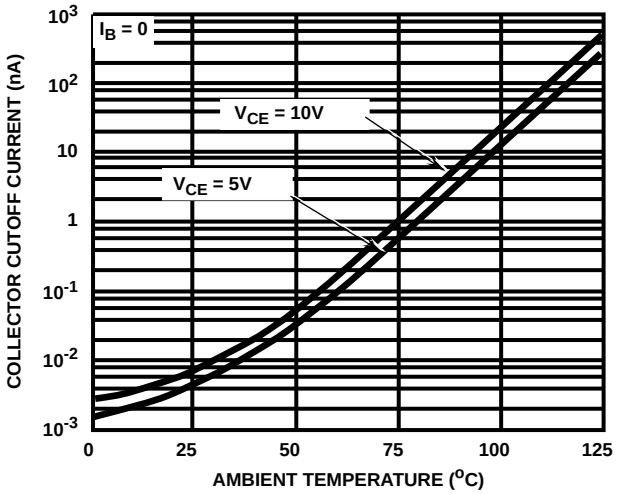


FIGURE 2. TYPICAL COLLECTOR-TO-EMITTER CUTOFF CURRENT vs TEMPERATURE

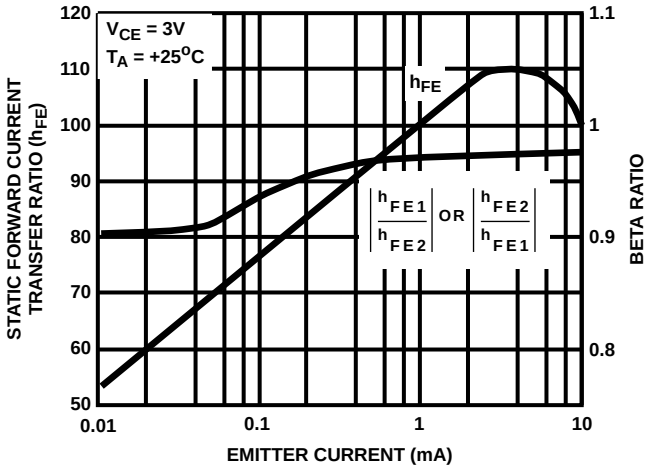


FIGURE 3. TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO AND BETA RATIO FOR TRANSISTORS Q_1 AND Q_2 vs EMITTER CURRENT

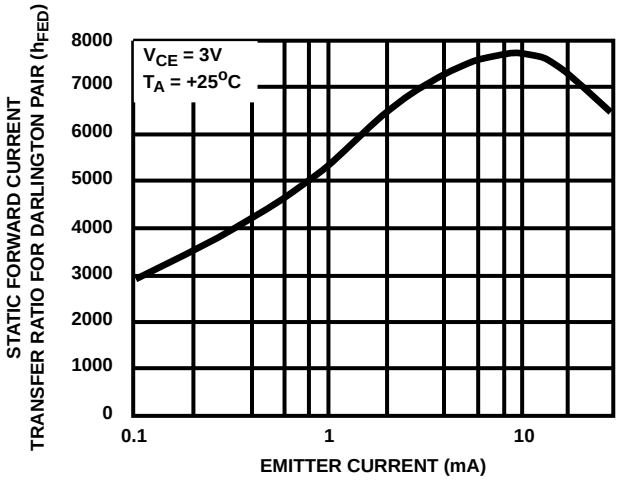


FIGURE 4. TYPICAL STATIC FORWARD CURRENT - TRANSFER RATIO FOR DARLINGTON CONNECTED TRANSISTORS Q_3 AND Q_4 vs EMITTER CURRENT

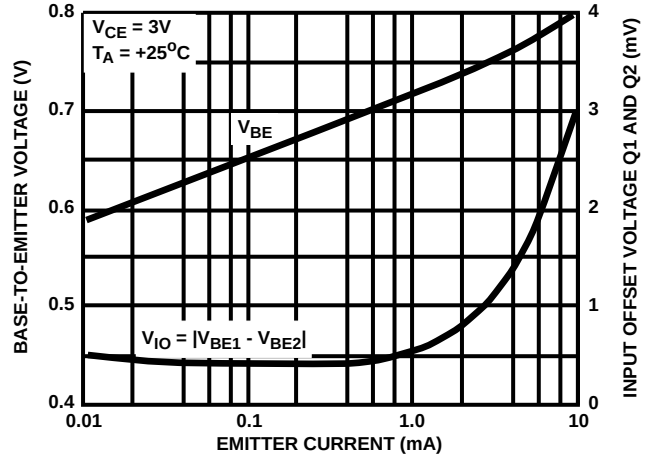


FIGURE 5. TYPICAL STATIC BASE-TO-EMITTER VOLTAGE CHARACTERISTIC AND INPUT OFFSET VOLTAGE FOR Q_1 AND Q_2 vs EMITTER CURRENT

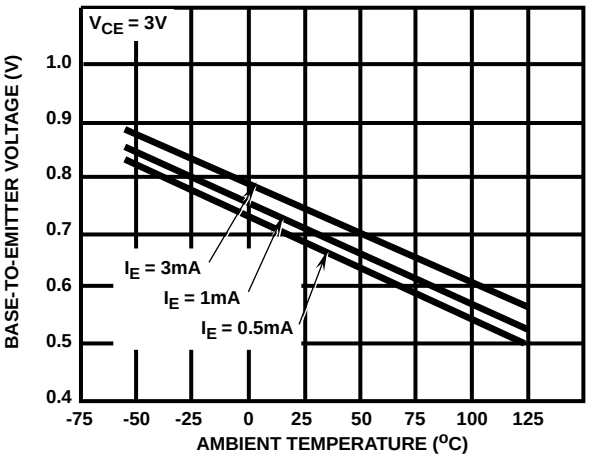


FIGURE 6. TYPICAL BASE-TO-EMITTER VOLTAGE CHARACTERISTIC FOR EACH TRANSISTOR vs TEMPERATURE

Typical Performance Curves (Continued)

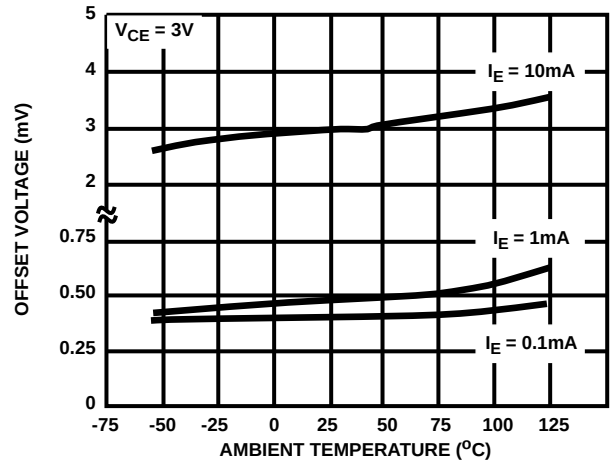


FIGURE 7. TYPICAL OFFSET VOLTAGE CHARACTERISTIC vs TEMPERATURE

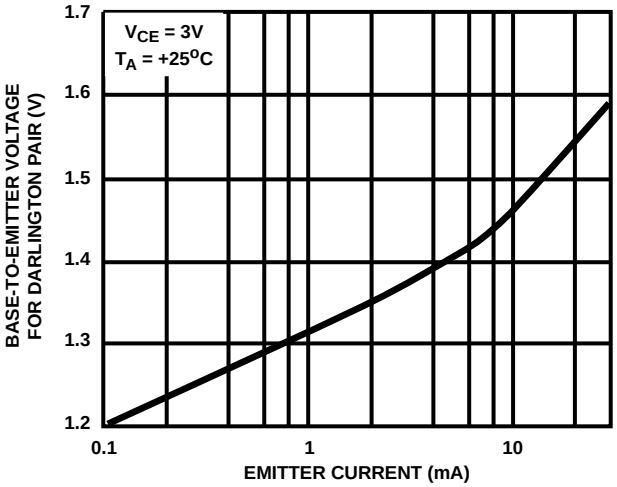


FIGURE 8. TYPICAL STATIC INPUT VOLTAGE CHARACTERISTIC FOR DARLINGTON PAIR (Q_3 AND Q_4) vs EMITTER CURRENT

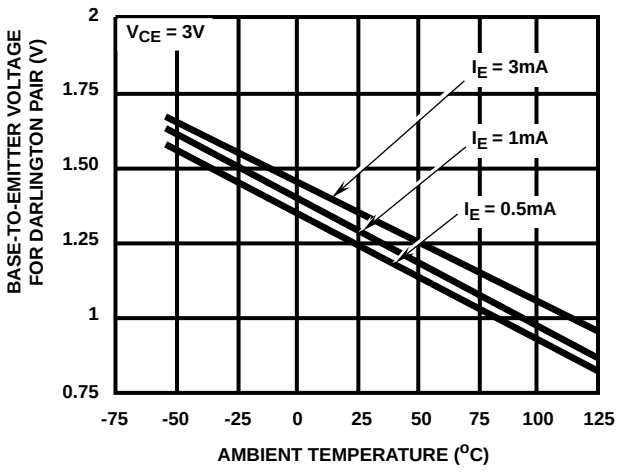


FIGURE 9. TYPICAL STATIC INPUT VOLTAGE CHARACTERISTIC FOR DARLINGTON PAIR (Q_3 AND Q_4) vs TEMPERATURE

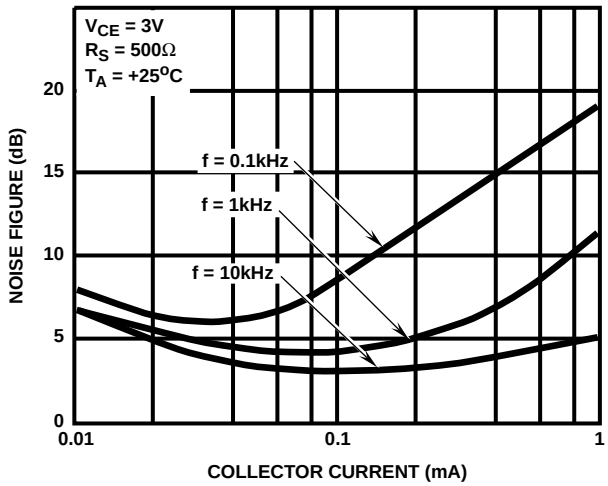


FIGURE 10. NOISE FIGURE vs COLLECTOR CURRENT, R_S = 500Ω

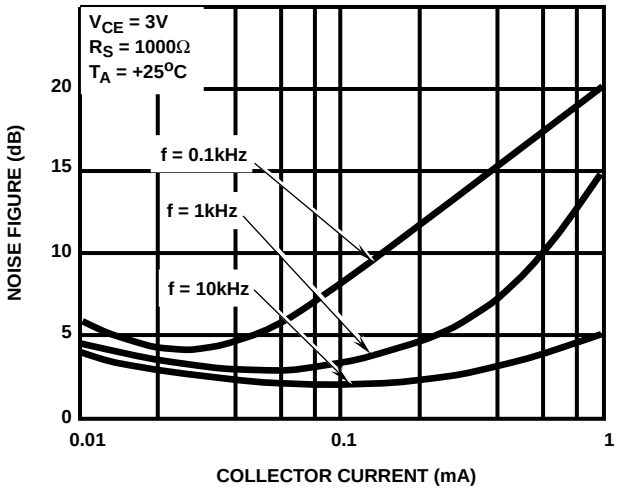


FIGURE 11. NOISE FIGURE vs COLLECTOR CURRENT, R_S = 1kΩ

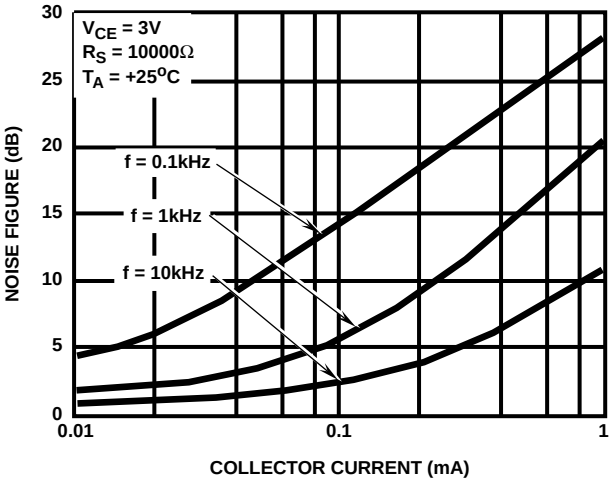


FIGURE 12. NOISE FIGURE vs COLLECTOR CURRENT, R_S = 10kΩ

Typical Performance Curves (Continued)

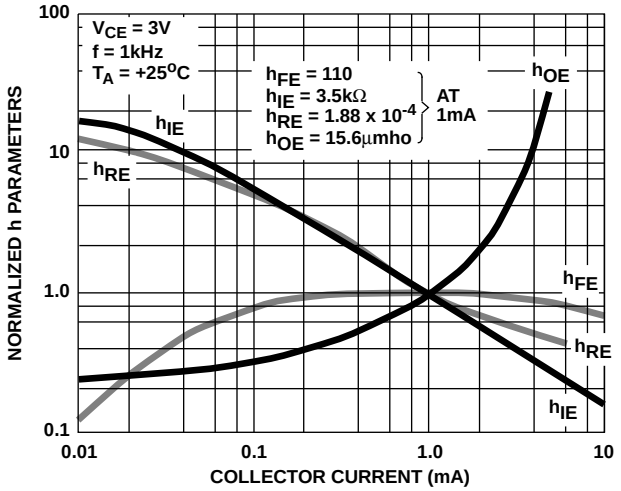


FIGURE 13. h PARAMETERS vs COLLECTOR CURRENT

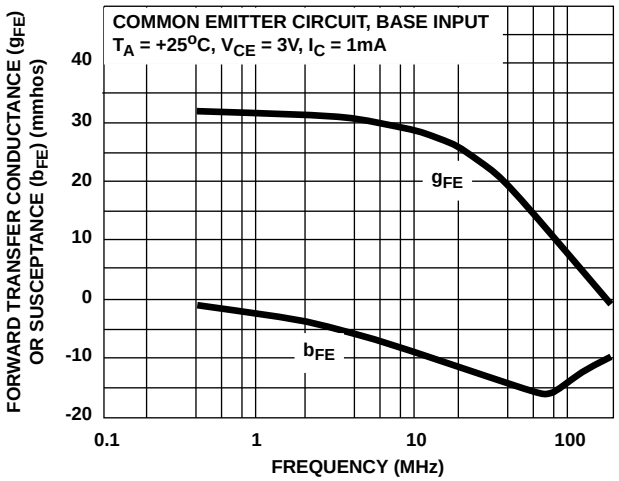


FIGURE 14. FORWARD TRANSFER ADMITTANCE (Y_{FE})

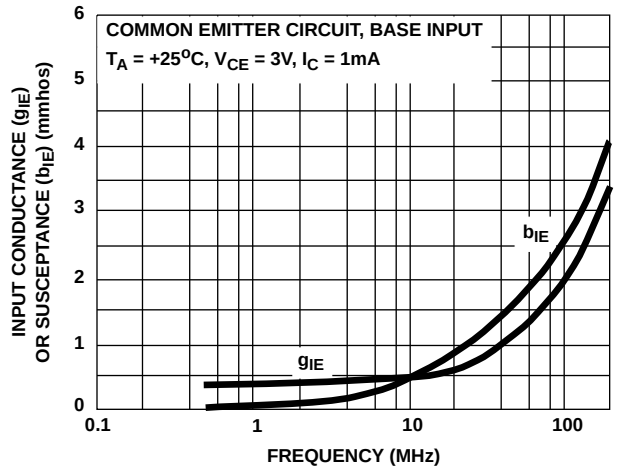


FIGURE 15. INPUT ADMITTANCE (Y_{IE})

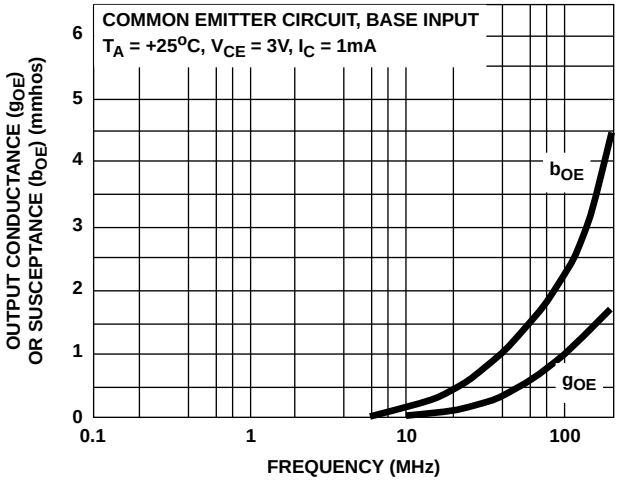


FIGURE 16. OUTPUT ADMITTANCE (Y_{OE})

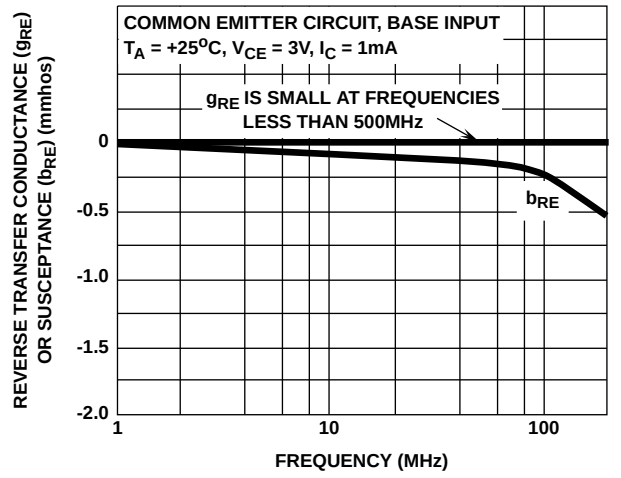


FIGURE 17. REVERSE TRANSFER ADMITTANCE (Y_{RE})

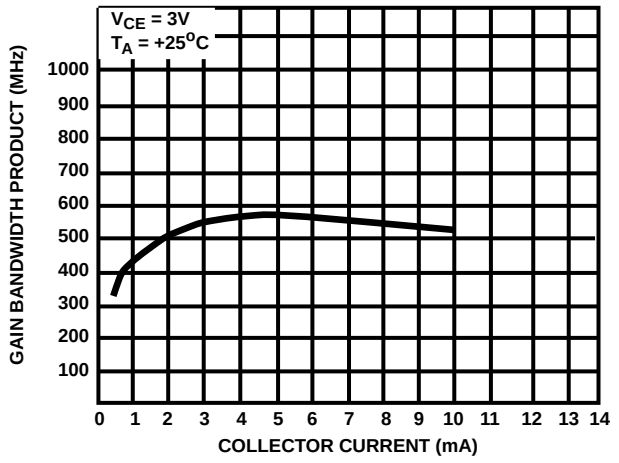


FIGURE 18. TYPICAL GAIN BANDWIDTH PRODUCT (f_T) vs COLLECTOR CURRENT