

## HIGH VOLTAGE FAST-SWITCHING NPN POWER TRANSISTOR

- HIGH VOLTAGE CAPABILITY
- FULLY MOLDED ISOLATED PACKAGE
- 2000 V DC ISOLATION (U.L. COMPLIANT)

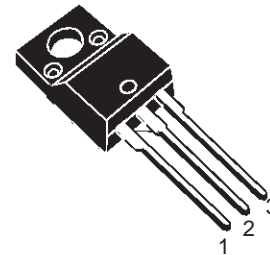
### APPLICATIONS:

- HORIZONTAL DEFLECTION FOR COLOUR TV AND MONITORS
- SWITCH MODE POWER SUPPLIES

### DESCRIPTION

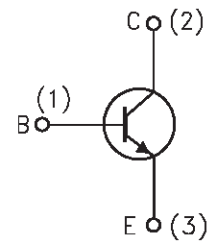
The BUH515FP is manufactured using Multiepitaxial Mesa technology for cost-effective high performance and uses a Hollow Emitter structure to enhance switching speeds.

The BUH series is designed for use in horizontal deflection circuits in televisions and monitors.



TO-220FP

### INTERNAL SCHEMATIC DIAGRAM



SC06960

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CBO}$	Collector-Base Voltage ( $I_E = 0$ )	1500	V
$V_{CEO}$	Collector-Emitter Voltage ( $I_B = 0$ )	700	V
$V_{EBO}$	Emitter-Base Voltage ( $I_C = 0$ )	10	V
$I_C$	Collector Current	8	A
$I_{CM}$	Collector Peak Current ( $t_p < 5$ ms)	12	A
$I_B$	Base Current	5	A
$I_{BM}$	Base Peak Current ( $t_p < 5$ ms)	8	A
$P_{tot}$	Total Dissipation at $T_c = 25$ °C	38	W
$T_{stg}$	Storage Temperature	-65 to 150	°C
$T_j$	Max. Operating Junction Temperature	150	°C

# THERMAL DATA

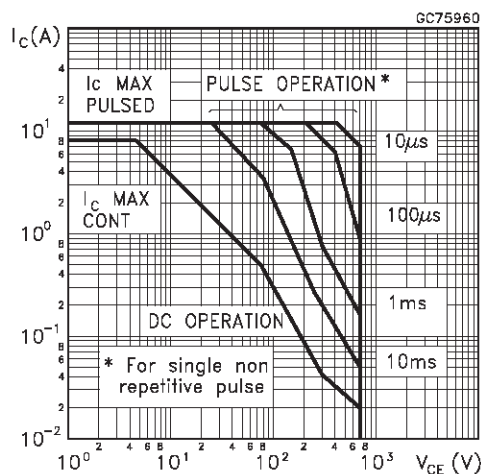
R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max	3.3	°C/W
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# ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C unless otherwise specified)

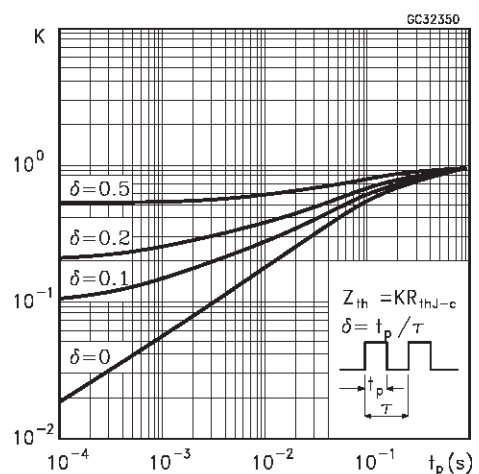
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I <sub>CES</sub>	Collector Cut-off Current (V <sub>BE</sub> = 0)	V <sub>CE</sub> = 1500 V V <sub>CE</sub> = 1500 V T <sub>j</sub> = 125 °C			0.2 2	mA mA
I <sub>EBO</sub>	Emitter Cut-off Current (I <sub>C</sub> = 0)	V <sub>EB</sub> = 5 V			100	μA
V <sub>CEO(sus)</sub>	Collector-Emitter Sustaining Voltage	I <sub>C</sub> = 100 mA	700			V
V <sub>EBO</sub>	Emitter-Base Voltage (I <sub>C</sub> = 0)	I <sub>E</sub> = 10 mA	10			V
V <sub>CE(sat)*</sub>	Collector-Emitter Saturation Voltage	I <sub>C</sub> = 5 A I <sub>B</sub> = 1.25 A			1.5	V
V <sub>BE(sat)*</sub>	Base-Emitter Saturation Voltage	I <sub>C</sub> = 5 A I <sub>B</sub> = 1.25 A			1.3	V
h <sub>FE*</sub>	DC Current Gain	I <sub>C</sub> = 5 A V <sub>CE</sub> = 5 V I <sub>C</sub> = 5 A V <sub>CE</sub> = 5 V T <sub>j</sub> = 100 °C	6 4		12	
t <sub>s</sub> t <sub>f</sub>	RESISTIVE LOAD Storage Time Fall Time	V <sub>CC</sub> = 400 V I <sub>C</sub> = 5 A I <sub>B1</sub> = 1.25 A I <sub>B2</sub> = 2.5 A		2.7 190	3.9 280	μs ns
t <sub>s</sub> t <sub>f</sub>	INDUCTIVE LOAD Storage Time Fall Time	I <sub>C</sub> = 5 A f = 15625 Hz I <sub>B1</sub> = 1.25 A I <sub>B2</sub> = -1.5 A V <sub>ceflyback</sub> = 1050 sin(π/5 10 <sup>6</sup> ) t V		2.3 350		μs ns
t <sub>s</sub> t <sub>f</sub>	INDUCTIVE LOAD Storage Time Fall Time	I <sub>C</sub> = 5A f = 31250 Hz I <sub>B1</sub> = 1.25 A I <sub>B2</sub> = -1.5 A V <sub>ceflyback</sub> = 1200 sin(π/5 10 <sup>6</sup> ) t V		2.3 200		μs ns

\* Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %

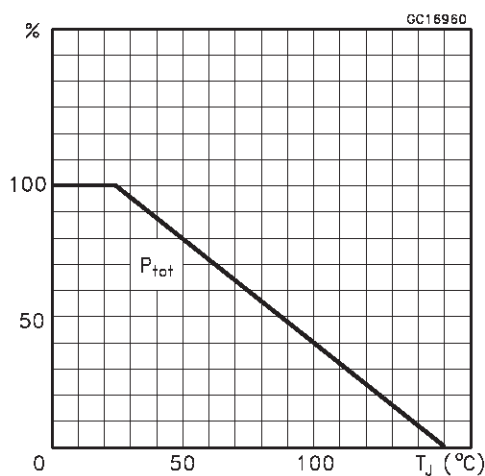
## Safe Operating Area



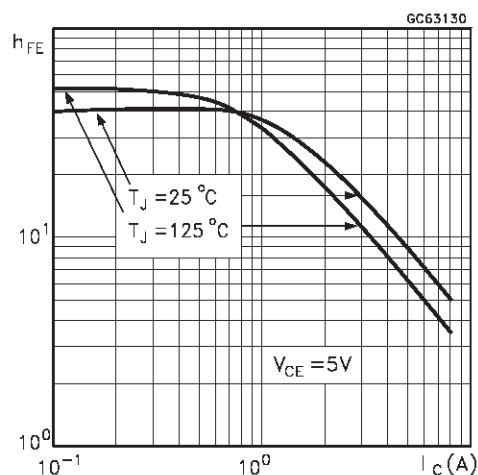
## Thermal Impedance



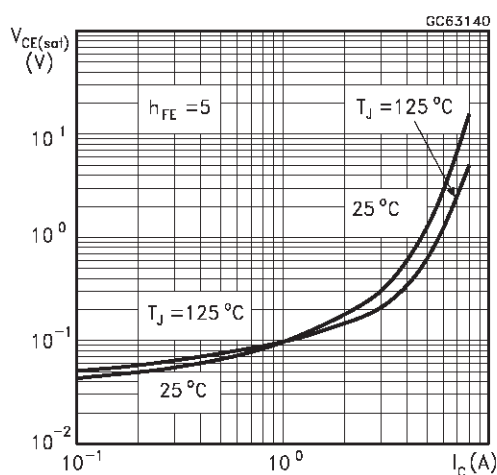
Derating Curve



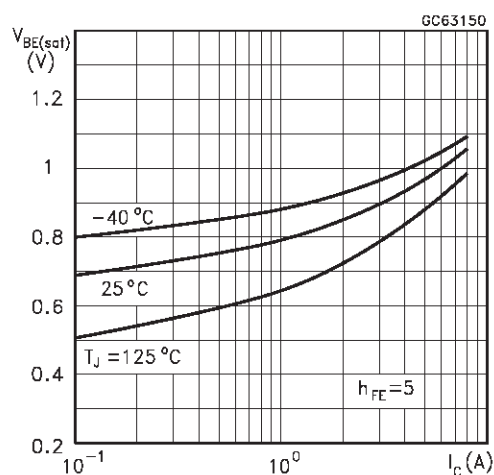
DC Current Gain



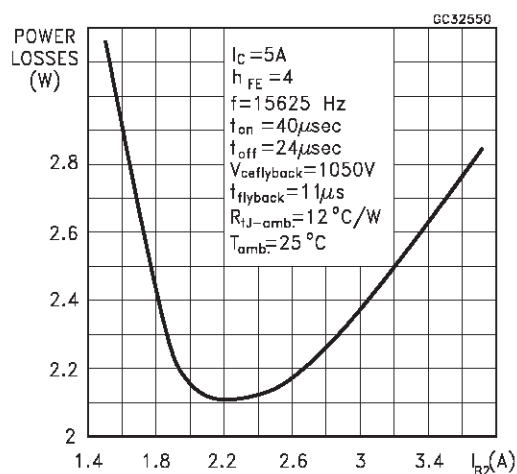
Collector Emitter Saturation Voltage



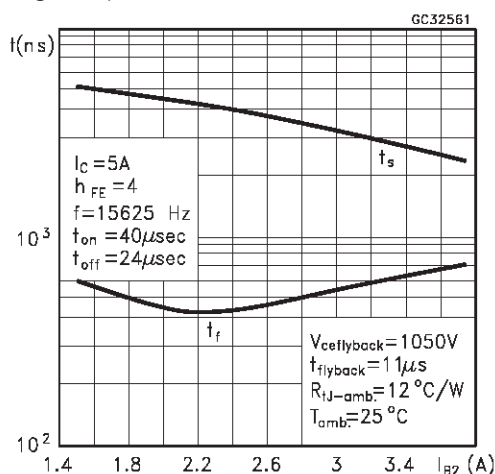
Base Emitter Saturation Voltage



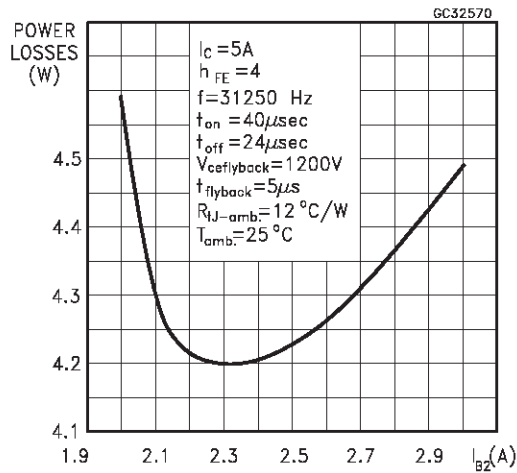
Power Losses at 16 KHz



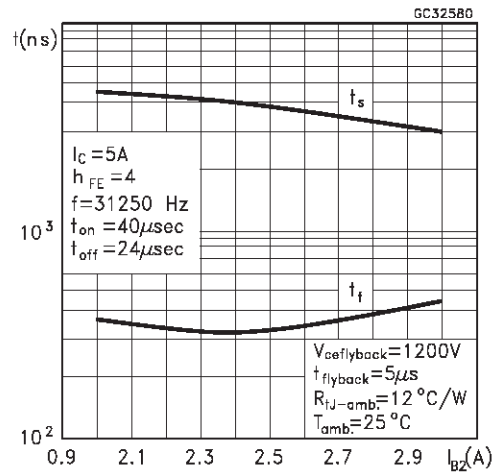
Switching Time Inductive Load at 16KHz  
(see figure 2)



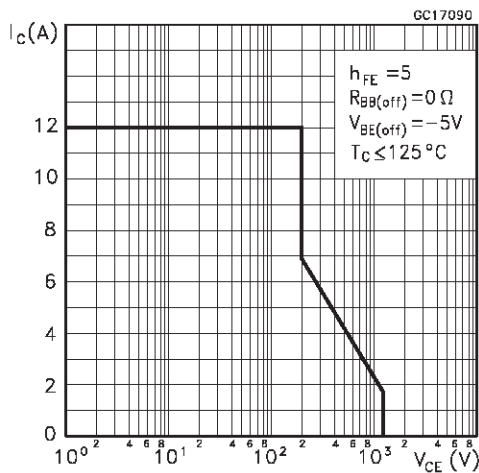
Power Losses at 32 KHz



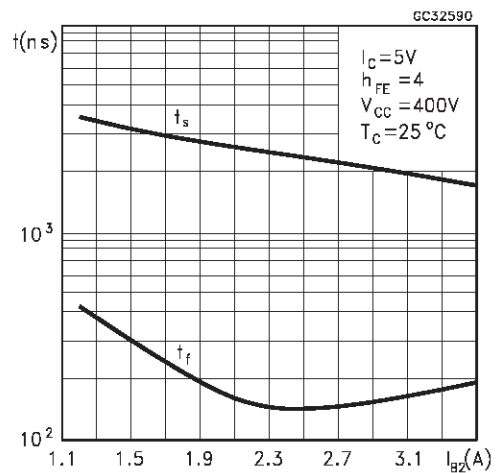
Switching Time Inductive Load at 32 KHz  
(see figure 2)



Reverse Biased SOA



Switching Time Resistive Load



BASE DRIVE INFORMATION

In order to saturate the power switch and reduce conduction losses, adequate direct base current  $I_{B1}$  has to be provided for the lowest gain  $h_{FE}$  at 100 °C (line scan phase). On the other hand, negative base current  $I_{B2}$  must be provided to turn off the power transistor (retrace phase).

Most of the dissipation, in the deflection application, occurs at switch-off. Therefore it is essential to determine the value of  $I_{B2}$  which minimizes power losses, fall time  $t_f$  and, consequently,  $T_j$ . A new set of curves have been defined to give total power losses,  $t_s$  and  $t_f$  as a function of  $I_{B2}$  at both 16 KHz and 32 KHz scanning frequencies for choosing the optimum negative drive. The test circuit is illustrated in

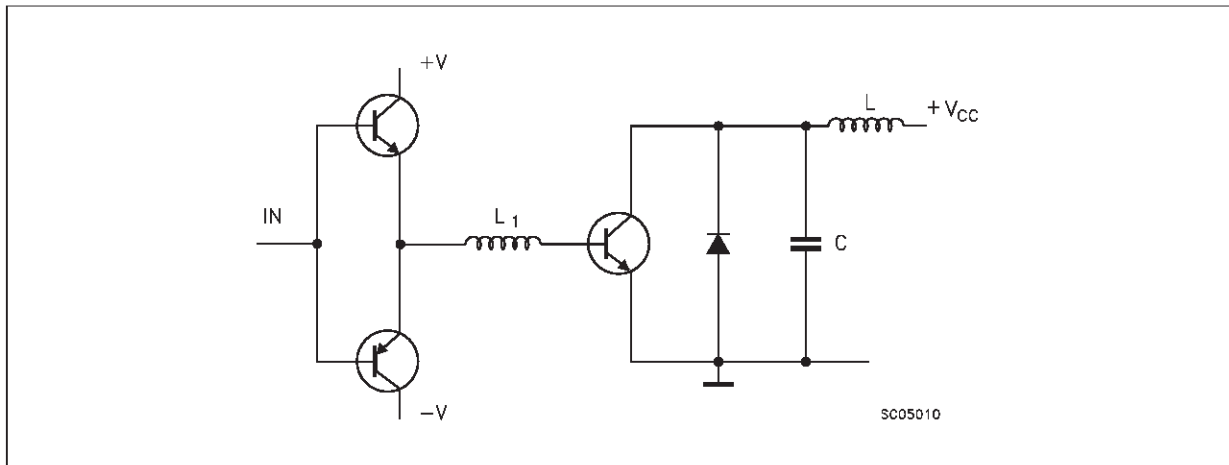
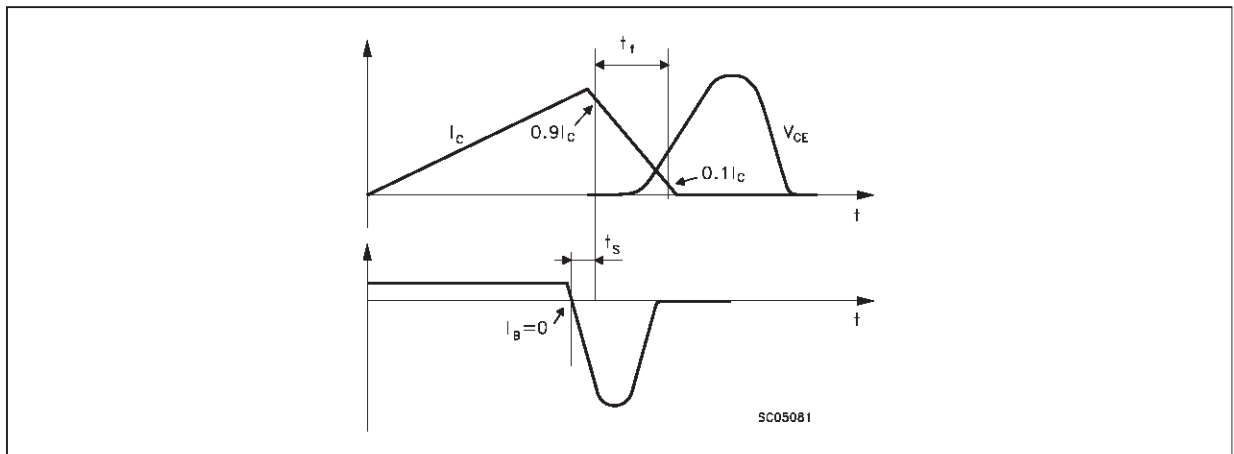
figure 1.

Inductance  $L_1$  serves to control the slope of the negative base current  $I_{B2}$  to recombine the excess carrier in the collector when base current is still present, this would avoid any tailing phenomenon in the collector current.

The values of  $L$  and  $C$  are calculated from the following equations:

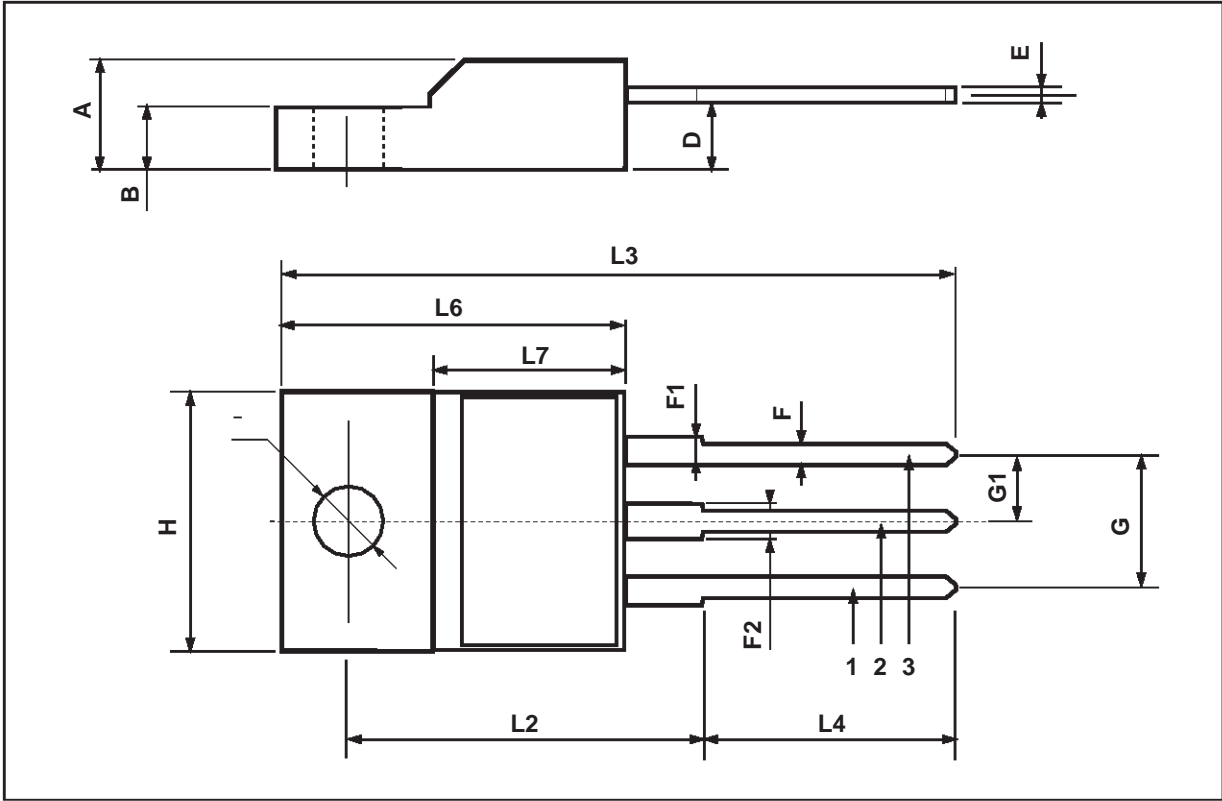
$$\frac{1}{2} L (I_C)^2 = \frac{1}{2} C (V_{CEfly})^2 \quad \omega = 2 \pi f = \frac{1}{\sqrt{LC}}$$

Where  $I_C$  = operating collector current,  $V_{CEfly}$  = flyback voltage,  $f$  = frequency of oscillation during retrace.

**Figure 1:** Inductive Load Switching Test Circuit.**Figure 2:** Switching Waveforms in a Deflection Circuit

TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



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