Digital NTSC/PAL Encoder
BU1417AK

The BU1417AK is an LSI IC that converts digital RGB input into analog video signals in the NTSC or PAL format.

●Applications

Video CDs and car navigation systems, etc.

●Features

1) Supported input clock signals : 27.0/13.5MHz, 28.636/14.318MHz, 28.375/14.1875MHz.
2) 24-bit input RGB signals (Supports 3 rates : 13.5, 14.3 and 14.2MHz)
3) Supports both timing master and timing slave sychronization signals.
4) NTSC, PAL, Y and C signals are output through 3-channel, 9-bit high-speed DAC (with 75Ω driver).
5) Internal 8-color OSD output function.
6) Single 5V power supply.

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}, AV_{DD}, DV_{DD}	−0.5~7.0	V
Input voltage	V_{IN}	−0.5~V_{DD}+0.5	V
Storage temperature	Tstg	−55~150	℃
Power dissipation	Pd	1375*1	mW

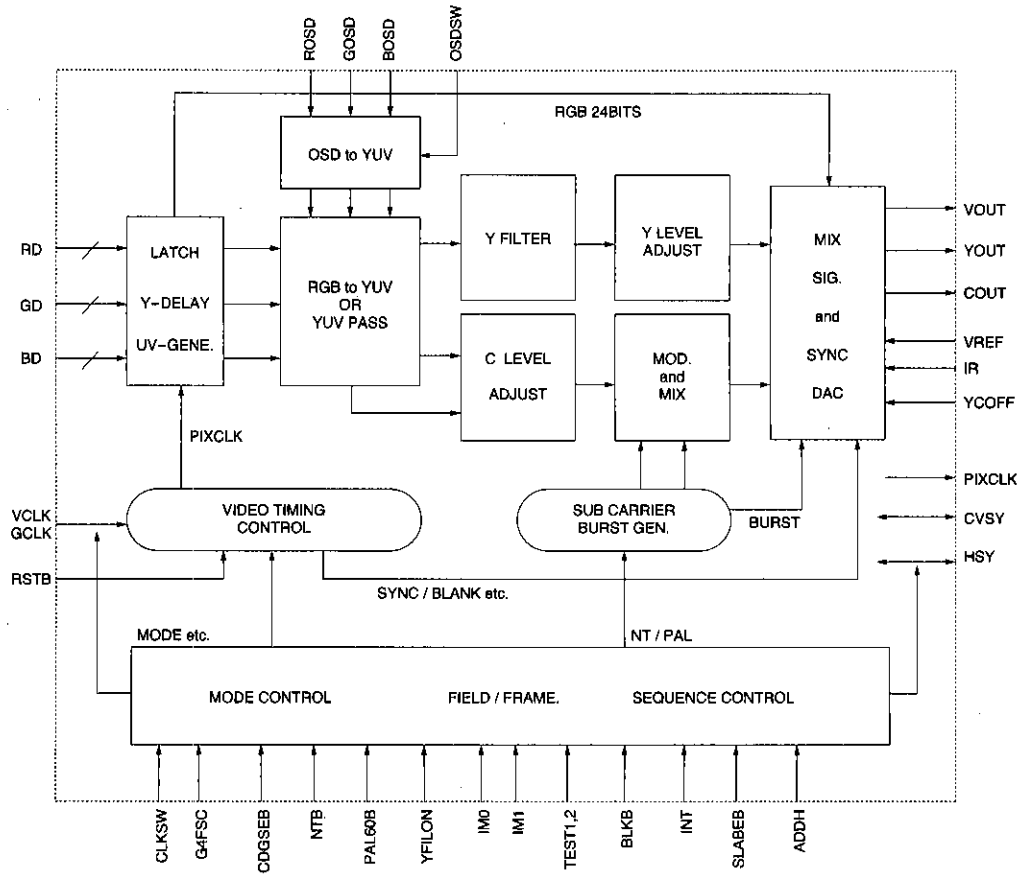
*1 Reduced by 11 mW for each increase in Ta of 1℃ over 25℃.
When mounted to a 70 × 70 × 1.6 mm glass epoxy board
* Does not represent guaranteed performance.
◎Not designed for radiation resistance.

●Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}=AV_{DD}=DV_{DD}*	4.75~5.25	V
Input voltage, high level	VIH	2.1~V_{DD}	V
Input voltage, low level	VIL	0~0.8	V
Analog input voltage	VAIN	0~AV_{DD}	V
Operating temperature	Topr	−25~60	℃

* Use at V_{DD} = AV_{DD} = DV_{DD}

●Block diagram



●Pin description

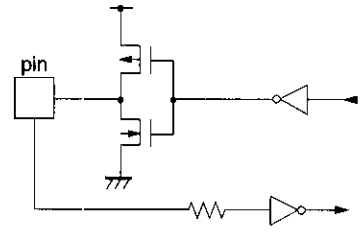
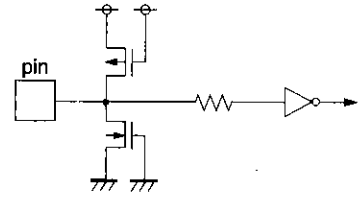
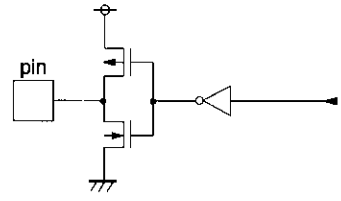
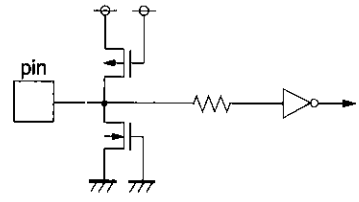
Pin No.	Pin name	Function	
1	BOSD	OSD BLUE DATA INPUT	*
2	GD0	GREEN DATA Bit0 (LSB)	*
3	GD1	GREEN DATA Bit1	*
4	GD2	GREEN DATA Bit2	*
5	GD3	GREEN DATA Bit3	*
6	GD4	GREEN DATA Bit4	
7	GD5	GREEN DATA Bit5	
8	GD6	GREEN DATA Bit6	
9	GND	DIGITAL GROUND	
10	GD7	GREEN DATA Bit7 (MSB)	
11	BD0	BLUE DATA Bit0 (LSB)	*
12	BD1	BLUE DATA Bit1	*
13	BD2	BLUE DATA Bit2	*
14	BD3	BLUE DATA Bit3	*
15	OSDSW	OSD INPUT ENABLE	*
16	CDGSWB	SELECT Video - CD/$\overline{\text{CD - G}}$	
17	BD4	BLUE DATA Bit4	
18	BD5	BLUE DATA Bit5	
19	BD6	BLUE DATA Bit6	
20	BD7	BLUE DATA Bit7 (MSB)	
21	GND	DIGITAL GROUND	
22	NTB	SELECT $\overline{\text{NTSC}}$/PAL MODE	
23	IM0	INPUT MODE SET Bit0	*
24	IM1	INPUT MODE SET Bit1	*
25	TEST1	NORMALLY PULLDOWN TO GND	*
26	TEST2	NORMALLY PULLDOWN TO GND	*
27	CVSY	C - SYNC OR V - SYNC INPUT	
28	HSY	H - SYNC INPUT	
29	PIXCLK	1/2 FREQ. OF INTERNAL CL	
30	BLKB	DATA BLANKING $\overline{\text{ENABLE}}$	*
31	V_{DD}	DIGITAL VDD	
32	INT	INTERLACE/$\overline{\text{NON - INTERLACE}}$	
33	SLABEB	SET MODE MASTER/$\overline{\text{SLABE}}$	*
34	ADDH	ADD ONE_LINE AT NON - INTER.	*
35	VREF	REFERENCE VOLTAGE (1.29V)	
36	CGND	CHROMA OUTPUT GROUND	
37	COUT	CHROMA OUTPUT	
38	VGND	COMPOSITE OUTPUT GROUND	
39	VOUT	COMPOSITE OUTPUT	
40	AVSS	ANALOG (DAC,VREF) GROUND	
41	NC	—	
42	IR	REFERENCE RESISTOR (1.2K)	
43	AVDD	ANALOG (DAC,REF) VDD	
44	YGND	LUMINANCE OUTPUT GROUND	
45	YOUT	LUMINANCE OUTPUT	
46	G4FSC	PULLDOWN TO GND	
47	GCLK	VIDEO CLOCK INPUT FOR CD - G	
48	YCOFF	DAC (YOUT,COUT) OFF	*
49	YFILON	PULLDOWN TO GND	*
50	PAL60B	$\overline{\text{PAL60 ON}}$ AT NTB=HIGH	◇
51	VCLK	VIDEO CLOCK INPUT FOR Video - CD	
52	RSTB	LOGIC PART INITIAL RESET	◇
53	CLKSW	DIVIDE INPUT CLK $\overline{\text{ENABLE}}$	
54	RD0	RED DATA Bit0 (LSB)	*
55	RD1	RED DATA Bit1	*
56	RD2	RED DATA Bit2	*
57	ROSD	OSD RED DATA INPUT	*
58	RD3	RED DATA Bit3	*
59	RD4	RED DATA Bit4	*
60	RD5	RED DATA Bit5	*
61	VDD	DIGITAL VDD	
62	RD6	RED DATA Bit6	*
63	RD7	RED DATA Bit7	*
64	GOSD	OSD GREEN DATA INPUT	*

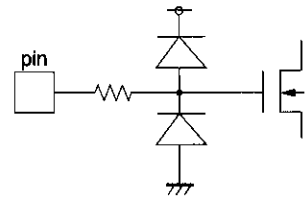
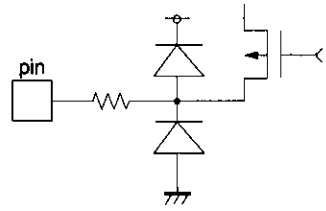
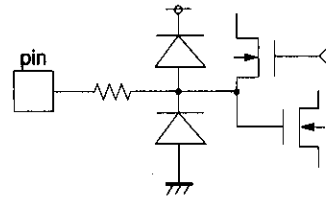
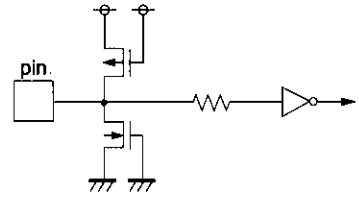
* Internal pull-down resistor

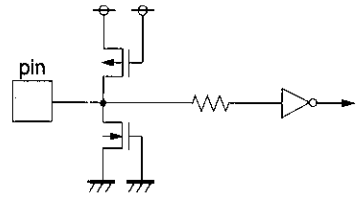
◇ Internal pull-up resistor

●Input/output circuits

Pin No.	Pin name	In/output	Equivalent circuit	Pin description
2~8 10	GD [0 : 7]	Input		G signals input during 24-bit RGB input.
11~14 17~20	BD [0 : 7]	Input		B signals input during 24-bit RGB input.
54~56 58~60 62,63	RD [0 : 7]	Input		R signals input during 24-bit RGB input.
1 57 64 15	ROSD GOSD BOSD OSDSW	Input		For OSD data input when using the OSD function. When OSDSW is HIGH, inputs from ROSD, GOSD and BOSD have priority.
16	CDGSWB	Input		For switching between the Video-CD mode (high) and CD-G mode (low)
22	NTB	Input		For switching between the NTSC mode (low) and PAL mode (high)
23 24	IMO IM1	Input		Control pin for setting the input mode to, RGB or DAC through.
28	HSY	Input and output		The horizontal synchronization pin. Inputs (when SLABEB is at the low level) or outputs (SLABEB when is at the high level) the negative HSYNC signal. Also used for the synch signal generated by halving the VCLK or GCLK clock frequencies.(when CLKSW is at the low level)

Pin No.	Pin name	In/output	Equivalent circuit	Pin description
27	CVSY	Input		Inputs the composite synchronization signal (CSYNC) or vertical synchronization signal (VSYNC) (when SLABEB is at the low level), or outputs the vertical synchronization signal (VSYNC) (when SLABEB is at the high level).
30	BLKB	Input		Setting this pin to the high level enables data output beginning with the line immediately following the one where equivalent pulse output ended (normally kept at the low level).
29	PIXCLK	Output		Output after the internal clock signal TS halved. Data are received at the edge transformation point of this clock signal.
32	INT	Input		Used to switch between interlacing (high level) and non-interlacing (low level). This pin is enabled in both the VIDEO-CD mode and CD-G mode.
33	SLABEB	Input		Used to switch between the master mode (high level) and slave mode (low level).
34	ADDH	Input		Enabled in the interlace mode. Used to switch between -0.5 lines (low level) and +0.5 lines (high level) as the number of lines in each interlacing field.

Pin No.	Pin name	In/output	Equivalent circuit	Pin description
35	VREF	Input		The reference voltage that determines the DAC output amplitude (1 LSB output current). Impress 1.29 V for normal (1 V_{P-P} output).
37	COUT	Output		S pin chroma output. CGND is the reference ground.
39	VOUT	Output		Composite output pin. VGND is the reference ground.
45	YOUT	Output		S pin luminance output. YGND is the reference ground.
42	IR	Input		Used to connect the reference resistor that determines DAC output amplitude (1 LSB output current). The current in this pin controls the per-bit current.
48	YCOFF	Input		Input of the low power mode switching signal. AT HIGH, the outputs of YOUT and COUT are turned off.
47	GCLK	Input		For input of the reference clock signal in the CD-G mode.
51	VCLK	Input		For input of the reference clock signal in the Video CD mode.

Pin No.	Pin name	In/output	Equivalent circuit	Pin description
52	RSTB	Input		For input of the reset signal that initializes the system
53	CLKSW	Input		Used to set the internal clock signal to one-half of GCLK/VCLK input (low level) or equal to GCLK/VCLK input (high level).
49 46	YFILON G4FSC	Input		Normally connect to GND.
50	PAL60B	Input		Used to switch between the PAL mode and PAL60 mode. Enabled when the NTB pin is at the high level.
25 26	TEST1 TEST2	Input		Normally connect to GND.
31,61 43	VDD AVDD	—	—	Power supply pin for the digital and analog blocks.
9,21 36 38 40 44 49	GND CGND VGND AVSS YGND DVSS	—	—	Ground pin for the digital and analog blocks, composite output, and Y and C signal output.

●Electrical characteristics (unless otherwise noted, Ta = 25℃, V_{DD} = AV_{DD} = DV_{DD} = 5.0V, GND = AVSS = DVSS = VGND = YGND = CGND = 0.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock frequency 1	fCLK1	—	27.0	—	MHz	Video CD mode and CD-G mode 1
Clock frequency 2	fCLK2	—	28.636	—	MHz	CD-G mode 2
Clock frequency 3	fCLK3	—	28.375	—	MHz	CD-G mode 3
Burst frequency 1	fBST1	—	3.5795	—	MHz	Subcarrier frequency (NTSC)
Burst frequency 2	fBST2	—	4.4336	—	MHz	Subcarrier frequency (PAL)
Burst cycle	CBST	—	9	—	CYC	
Operating circuit current	IDD	—	130.0	—	mA	*TBD
Output voltage, high level	VOH	4.0	4.5	—	V	IOH=−2.0mA
Output voltage, low level	VOL	—	0.5	1.0	V	IOH=2.0mA
Input voltage, high level	VIH	2.1	—	—	V	
Input voltage, low level	VIL	—	—	0.8	V	
Input current, high level	IIH	−10.0	0.0	10.0	μA	
Input current, low level	IIL	−10.0	0.0	10.0	μA	
DAC resolution	RES	—	9	—	BITS	
Linearity error	EL	—	±3.0	—	LSB	
Y white level current	IYW	—	25.14	—	mA	VREF=1.29V、RIR=1.2kΩ
Y black level current	IYB	—	7.24	—	mA	VREF=1.29V、RIR=1.2kΩ
Y zero level current	IYZ	−10.0	0.0	10.0	μA	

●Circuit operations

(1) General

The BU1417AK converts and outputs 8-bit digital image data to 9-bit composite signals (VOUT), luminosity signals (YOUT) and color signals (COUT) in the NTSC, PAL or PAL60 formats.

Digital image data are adaptable for decoded video CD and CD-G output. The output television signal can be switched to NTSC, PAL, PAL60, interlace or non-interlace. The clock signals input from VCLK and GCLK can be used as the source clock for the internal clock. The receiving and processing of input signals is synchronized with the rise of the internal clock (BCLK, the base clock).

Input signals are input from pins RD0 through RD7, GD0 through GD7 and BD0 through BD7 in the RGB (4 : 4 : 4) format. Input format is selected with IM0 and IM1.

Enabling OSDSW validates input data from ROSD, GOSD and OSD, allowing for the input of 7-color (8 including black) data. As a clock frequency equal to 1/2 of the internal clock frequency is simultaneously output from PIXCLK, an OSD IC can be synchronized with the BU1417AK by connecting its clock input pin to PIXCLK.

Input data are internally converted to YUV in the case of the RGB format or OSD input. Internal Y, U and V data are adjusted to the NTSC 100 IRE level, after which U and V data are phase-modulated by an internally ordered subcarrier (3.58MHz in the NTSC mode and 4.43MHz in the PAL or PAL60 mode), generating modulated color signals.

Finally, the needed synchronization levels, color blank level and burst signals, etc., are mixed, and NTSC composite signals, luminance signals and color signals are output through the 9-bit DAC.

NTSC composite : VOUT
Luminance signal (Y) : YOUT
Color signal (C) : COUT

When the video input pin (75Ω) is connected, the luminance component of DAC output has a roughly 1.0Vpp output range at the white level. For details concerning DAC output voltage levels, refer to Section 5, "DAC output level adjustment."
As the YOUT and COUT DAC output pins can be turned off by setting YCOFF to HIGH, the BU1417AK allows for a low power mode.

Table 1 : YCOFF low power mode

Pin No.	Pin	Output mode and power consumption *			
	YCOFF	VOUT	YOUT	COUT	Power consumption (Typ.)
48	LOW	Composite signal	Luminance signal	Chroma signal	0.65W
	HIGH	Composite signal	No output (0V)	No output (0V)	0.35W

* AV_{DD}=5.0V

(2) Mode setting

1) Output mode

Digital image data can be adapted for Video-CD and CD-G modes, which are selected according to the CDGSWB input voltage. The CD-G mode is selected when CDGSWB input is at the low level, the video CD mode when CDGSWB input is at the high level. Supported output television modes are NTSC, PAL and PAL60, which are selected according to the inputs of NTB and PAL60 : The NTSC mode is selected when NTB is at the low level, the PAL mode when PAL60B is at the high level, and the PAL60 mode4 when NTB is at the high level and PAL60B is at the low level.

Table 2-1-1 : Mode setting

NTB	PAL60	GDGSWB	Decoder mode	TV mode
0	*	0	CD - G	NTSC
0	*	1	Video - CD	NTSC
1	0	0	CD - G	PAL60
1	0	1	Video - CD	PAL60
1	1	0	CD - G	PAL
1	1	1	Video - CD	PAL

Also, output is switched between interlaced output and non-interlaced output depending on the input to INT : Non-interlaced output is selected when INT is at the low level, interlaced output when INT is at the high level. During non-interlaced output, the per-field line count can be controlled with ADDH : A per-field line count for interlaced output of −0.5 lines is selected when ADDH is at the low level, and a per-field line count for interlaced output of +0.5 lines when ADDH is at the high level.

Table 2-1-2 : Interlaced/non-interlaced mode setting

INT	ADDH	Scanning mode	Line count per field	
			NTSC/PAL60	PAL
0	0	Non-interlaced	262	312
0	1	Non-interlaced	263	313
1	*	Interlaced	262.5	312.5

In addition, BLKB is used to control data output that follows immediately after the end of the equivalent pulse : Data output immediately after the end of the equivalent pulse is prohibited when BLKB is at the low level, and enabled when BLKB is at the high level. Thus, this IC supports closed-caption and teletext broadcasting.

2) Input format

In addition to converts digital RGB input into the NTSC or PAL format, the BU1417AK can also converts digital RGB input to anlalog RGB signals. (DAC through mode)

The input format for digital data is set with IM1 and IM0 as shown in the table below.

Table 2-2-1 : Input format setting

IM1	IM0	Input format	Output signal
0	0	R (8 bits), G (8 bits) and B (8 bits)	Television signal (9-bit resolution)
1	1	RGB input expanded to ROSD, GOSD, BOSD	RGB analog signal (9 bits)

RGB through mode bit assignment is shown in table below

Table 2-2-2 : RGB through mode bit assignment

Output pin	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VOUT (39)	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	ROSD
YOUT (45)	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0	GOSD
COUT (37)	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	BOSD

The BU1417AK also has internal OSD switches and a color data generation function, simplifying combined use with an OSD IC that outputs blank and RGB signals. Because the BU1417AK outputs a clock frequency equal to 1/2 of the internal processing frequency, an ODSD IC can be synchronized by connecting its clock input to this output.
Inputs to ROSD, GOSD and BOSD are valid while OSDSW is at the HIGH level. The relationship between OSD data and color data output is shown in Table 2-2-3 below.

Table 2-2-3 : OSD function : Input data/color output correlation

OSDSW	ROSD	GOSD	BOSD	Output color signal
1	0	0	0	Block (blanking)
1	0	0	1	Blue
1	0	1	0	Green
1	0	1	1	Cyan
1	1	0	0	Red
1	1	0	1	Magenta
1	1	1	0	Yellow
1	1	1	1	White
0	*	*	*	Depends on input set with IM0 and IM1

3) Clock
The BU1417AK has a clock input pin for the video CD mode (VCLIK) and a clock input pin for the CD-G mode (GCLK). The state of CDGSWB determines which clock input is enabled. The disabled clock input is not supplied to the IC.

Table 2-3-1 : Switching clock input

CDGSW	GCLK input	VCLK input
0	Used by the internal clock	Invalid
1	Invalid	Used by the internal clock

Generally, the externally supplied clock frequency should be double the internal clock frequency (BCLK, base clock) (when CLKSW is at the low level). The phase relationship between the internal and external clock signals is like that shown in Fig. 2-3-1 below, with HYS input as the reference.. In the master mode, in which HSY is used for output, HSY output is timed as shown in Fig. 2-3-1 below. The BU1417AK receives data (RD, GD and BD, etc.) at the rise of the internal clock (BCLK), and data should be input as shown in the figure below.

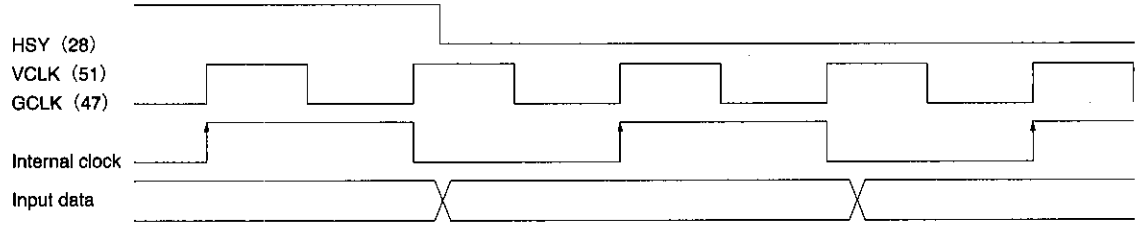


Fig. 2−3−1 Clock timig (CLKSW = 「LOW」)

An external clock frequency can be used as the internal clock frequency (BCLK) without modification by setting CLKSW to the high level. Data (RD, GD and BD, etc.) are also received with the rise of BCLK, and so data should be input as shown in Fig. 2-3-2 below, which also shows the relationship with HSY.

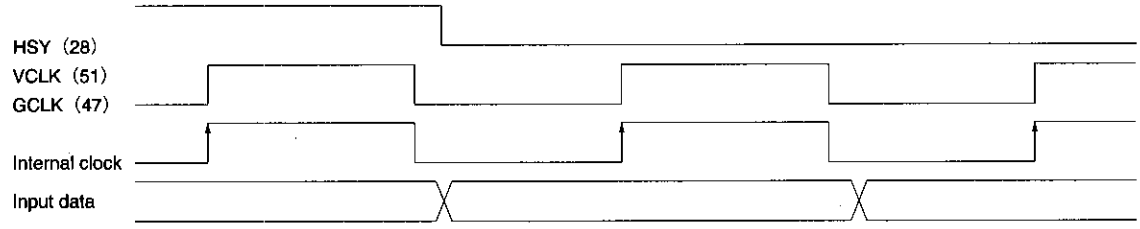


Fig. 2−3−2 Clock timing (CLKSW = 「HIGH」)

The BU1417AK generates a subcarrier (burst) frequency according to the input clock frequency. This limits the frequency used in each mode, and so data should be input at the frequencies shown below (Table 2-3-2).

Table 2-3-2 : Clock input frequencies (BU1417AK)

Pin CLKSW	Video-CD mode	CD-G mode	
	NTSC/PAL/PAL60 (common)	NTSC	PAL / PAL60
0	27.000MHz	28.636MHz	28.3750MHz
1	13.500MHz	14.318MHz	14.1875MHz

4) Synchronization signals

The BU1417AK has two synchronization signal modes : the encoder master mode, in which the synchronization signal is output, and the encoder slave mode, in which the IC is synchronized to a synchronization signal input externally. The mode is selected with SLABEB : The slave mode is selected when SLABEB is at the low level, the master mode when SLABEB is at the high level.

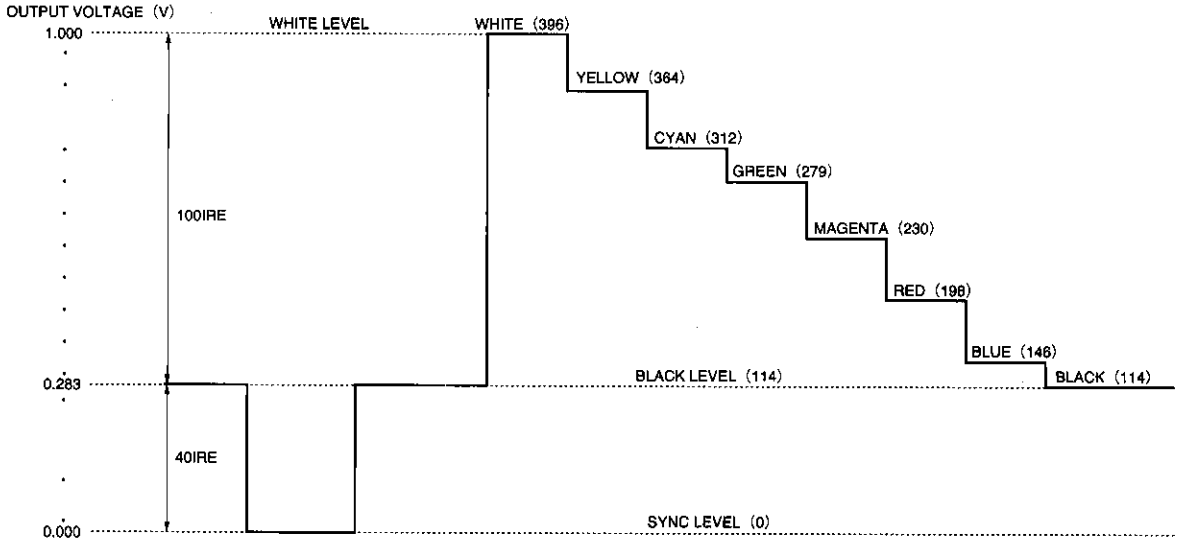
In the master mode, the signals from HSY and CVSY are output : the horizontal synchronization signal (HSYNC) from HSY and the vertical synchronization signal (VSYNC) from CVSY. In this mode, synchronization signal output is timed to the rise of RSTB, generating output according to the selected format (NTSC, PAL, PAL60, interlaced or non-interlaced).

In the slave mode, signals are input to HSY and CVSY : the horizontal synchronization signal (HSYNC) to HSY and the vertical synchronization signal (VSYNC) or a composite synchronization signal to CVSY. The IC automatically determines whether the input synchronization signal is VSYNC or CSYNC. Select the appropriate input synchronization signal for the mode that has been set. After termination of RSTB, input odd and even numbers alternately.

The BU1417AK is designed to handle only negative synchronization signals (i.e., those that result in the low level during the sink).

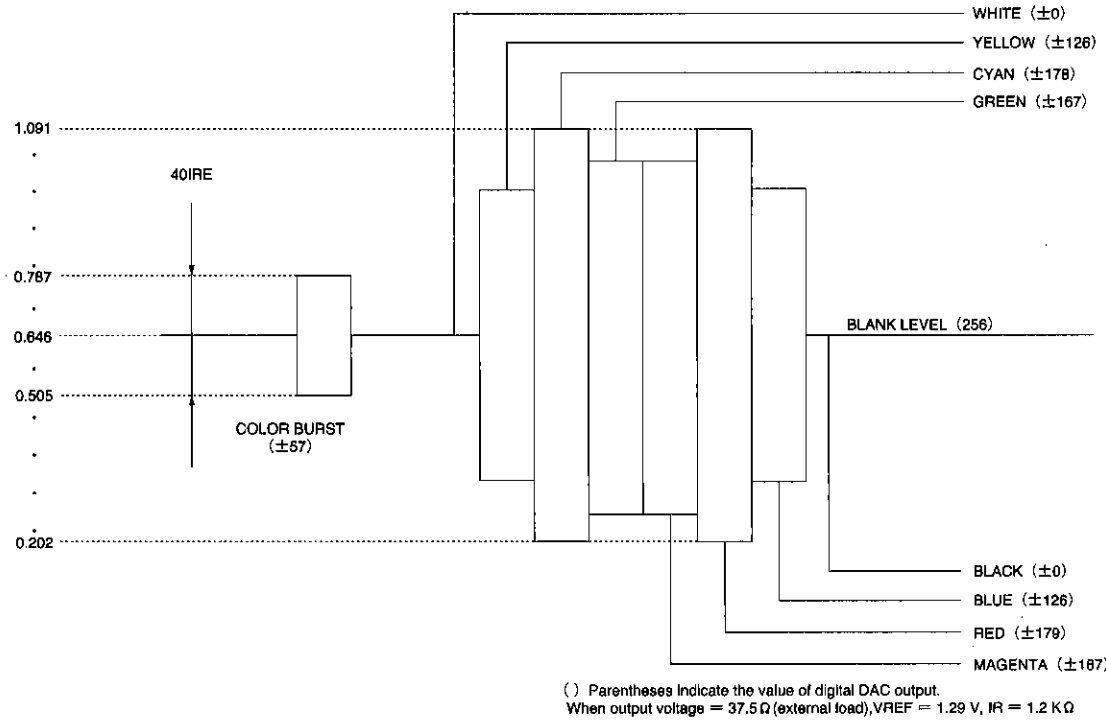
(3) Output level

Figures 1 through 6 below show pin output voltage level and the digital values of DAC output.



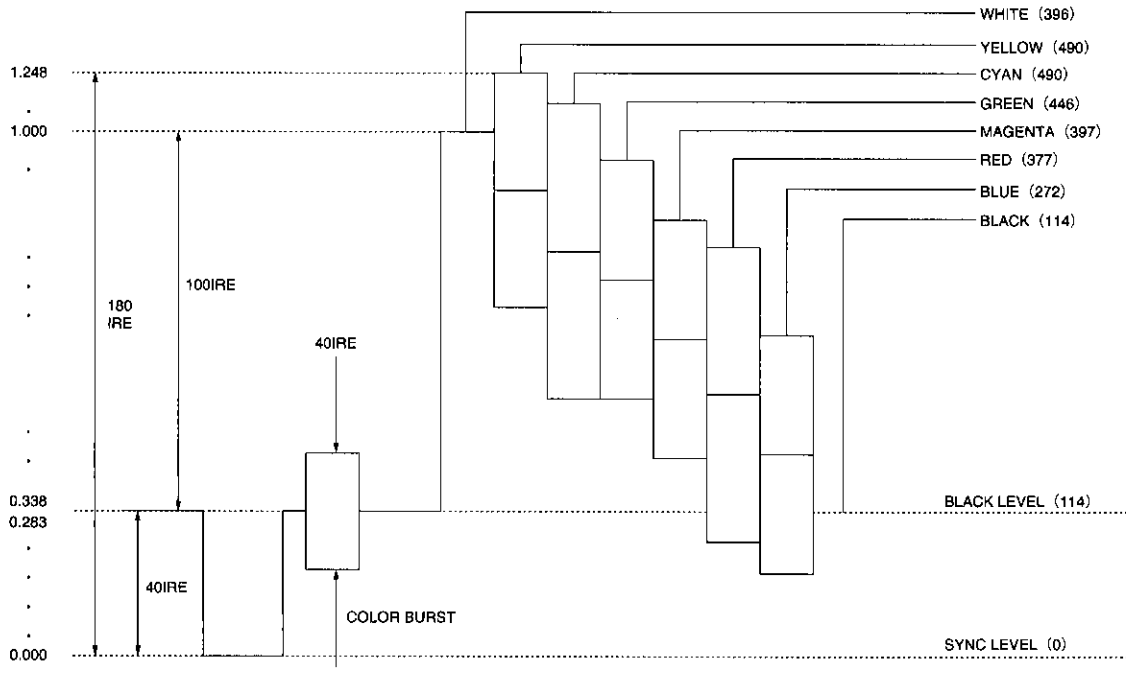
( ) Parentheses indicate the value of digital DAC output.
When output voltage = 37.5Ω (external load), VREF = 1.29 V, IR = 1.2 KΩ

Fig. 1 NTSC Y (luminosity) signal output level



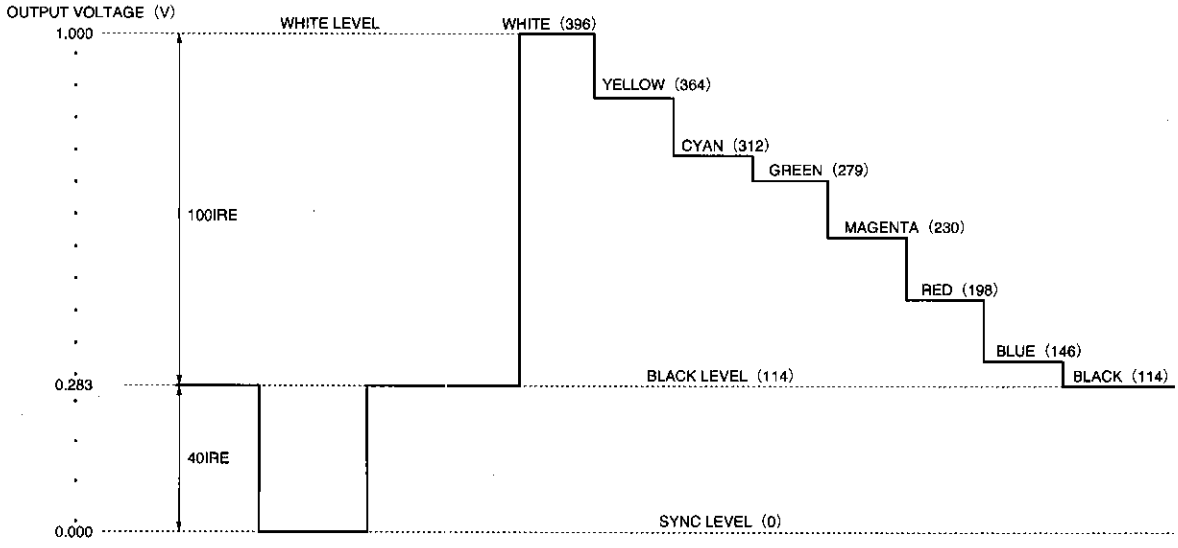
( ) Parentheses indicate the value of digital DAC output.
When output voltage = 37.5 Ω (external load), VREF = 1.29 V, IR = 1.2 KΩ

Fig. 2 NTSC C (chroma) signal output level



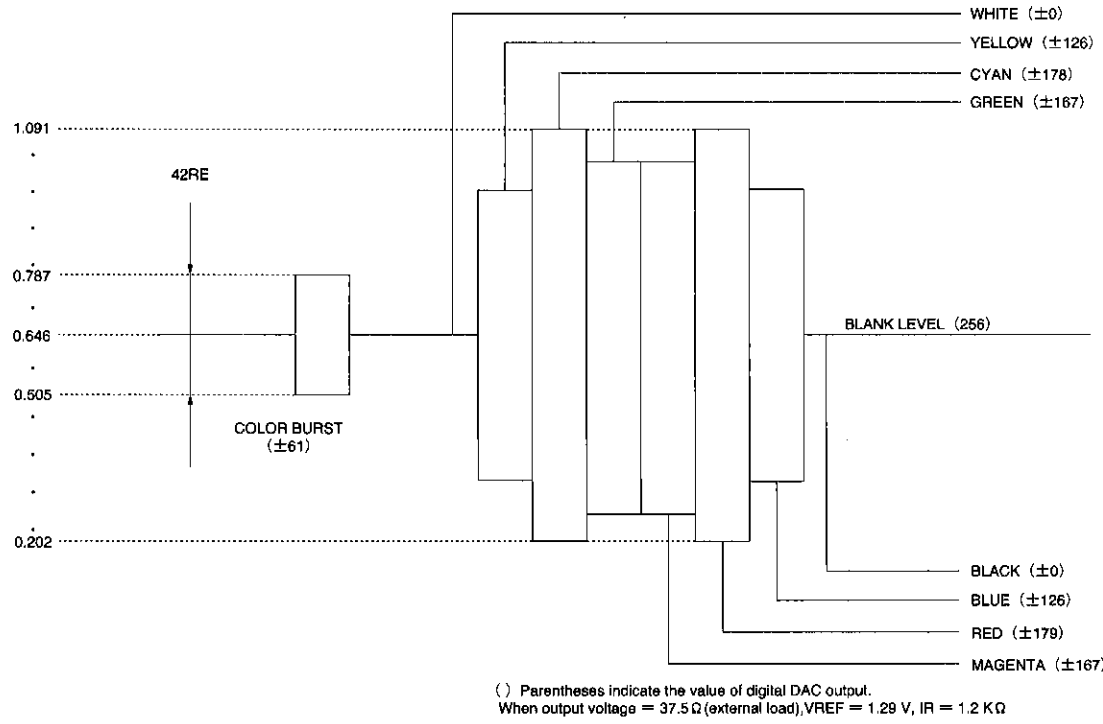
( ) Parentheses indicate the value of digital DAC output.
When output voltage = 37.5 Ω (external load), VREF = 1.29 V, IR = 1.2 KΩ

Fig. 3 NTSC V (composite) signal output level



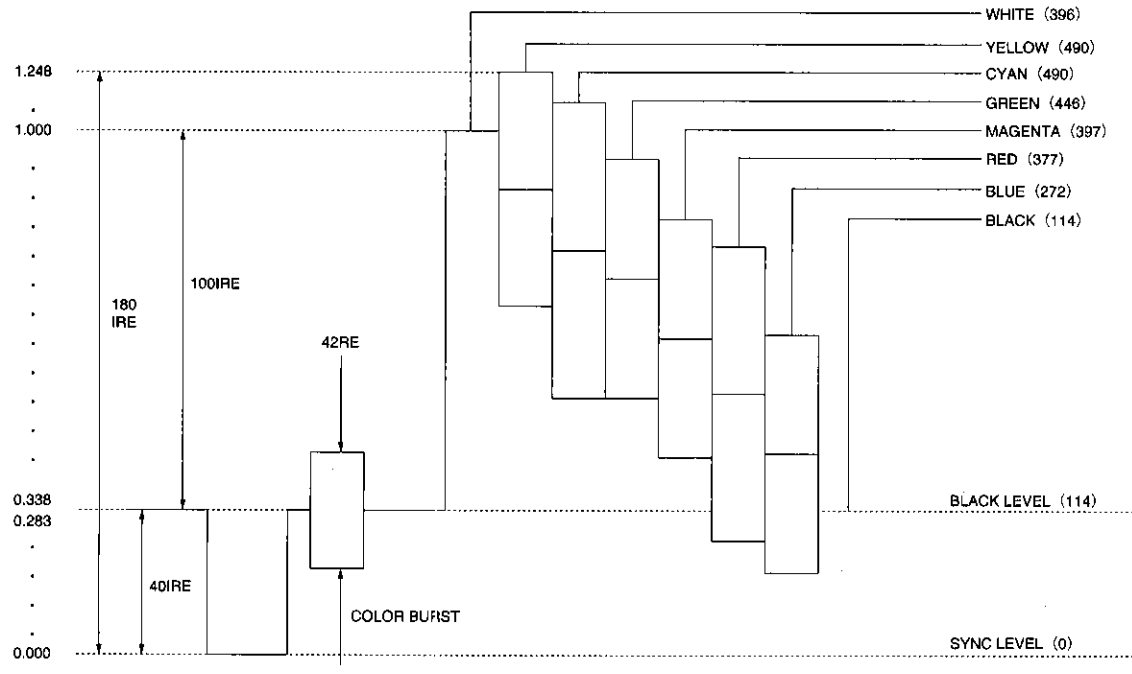
( ) Parentheses indicate the value of digital DAC output.
When output voltage = 37.5 Ω (external load), VREF = 1.29 V, IR = 1.2 KΩ

Fig. 4 PAL/PAL60 Y (luminosity) signal output level



( ) Parentheses indicate the value of digital DAC output.
When output voltage = 37.5 Ω (external load), VREF = 1.29 V, IR = 1.2 KΩ

Fig. 5 PAL/PAL60 C (chroma) signal output level



( ) Parentheses indicate the value of digital DAC output.
When output voltage = 37.5Ω (external load), VREF = 1.29 V, IR = 1.2 KΩ

Fig. 6 PAL/PAL60 V (composite) signal output level

(4) Timing

The BU1417AK is a digital encoder that outputs television signals in the NTSC, PAL or PAL60 format according to the inputs and outputs of VCLK, GCLK, HSY and VSY. The timing input and output pins are shown in Table 4-1 below.

Table 4-1 : Timing input and output (BU1417AK)

No	Pin	Name	Input/output	Function
1	52	RSTB	Input	System reset input
2	47	GCLK	Input	CD-G clock input
3	51	VCLK	Input	Video CD clock input
4	53	CLKSW	Input	Clock input mode setting
5	27	CVSY	Input and output	Vertical and composite synchronization signal input and output
6	28	HSY	Input and output	Horizontal synchronization signal input and output
7	16	CDGSWB	Input	Switching between the video CD and $\overline{\text{CD-G}}$ modes
8	22	NTB	Input	Switching between the NTSC and PAL modes
9	50	PAL60B	Input	Switching between the PAL and PAL60 modes
10	30	BLKB	Input	Enabling data output immediately after the equivalent pulse (9H)
11	32	INT	Input	Switching between the interlaced and non-interlaced modes
12	33	SLABEB	Input	Switching between the master and slave modes
13	34	ADDH	Input	Adding 1 line in the non-interlaced mode

Clock timing (when CLKSW = low level)

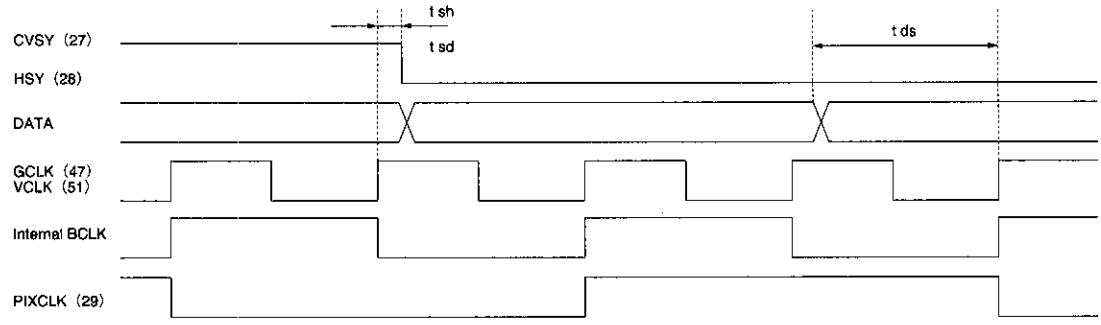


Fig. 7 Clock timing and data input timing

Parameter	Symbol	Unit	Min.	Typ.	Max.
Input hold time ,SYNC	t sh	nS	—	10.0	—
Output delay time, SYNC	t sd	nS	—	20.0	—
Data setup time	t ds	nS	—	15.0	—

In the slave mode, time inputs to HSY and CVSY according to the timing for HSY in Fig. 7. In the master mode, synchronization signal output is timed as shown in Fig. 7.

Clock timing (when CLKSW = high level)

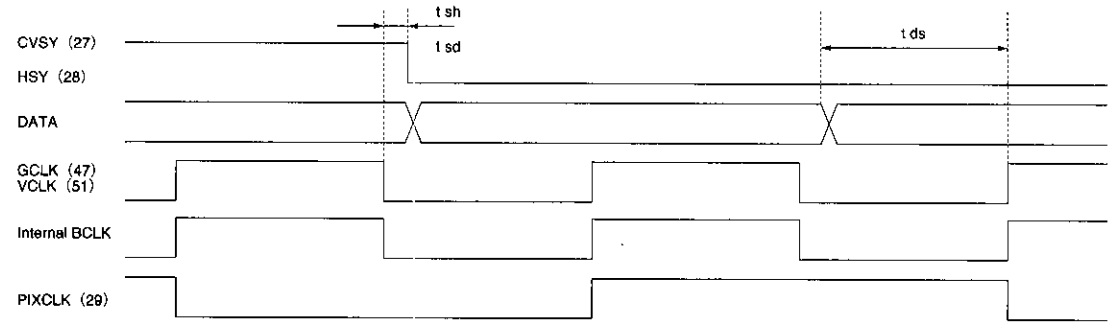


Fig. 8 Clock timing and data input timing

Parameter	Symbol	Unit	Min.	Typ.	Max.
Input hold time, SYNC	t sh	nS	—	10.0	—
Output delay time,SYNC	t sd	nS	—	20.0	—
Data setup time	t ds	nS	—	15.0	—

In the slave mode, inputs to HSY and CVSY should be timed according to the timing for HSY (Fig. 8). In the master mode, synchronization signal output is timed as shown in Fig. 8.

Odd/even discrimination timing in the slave mode

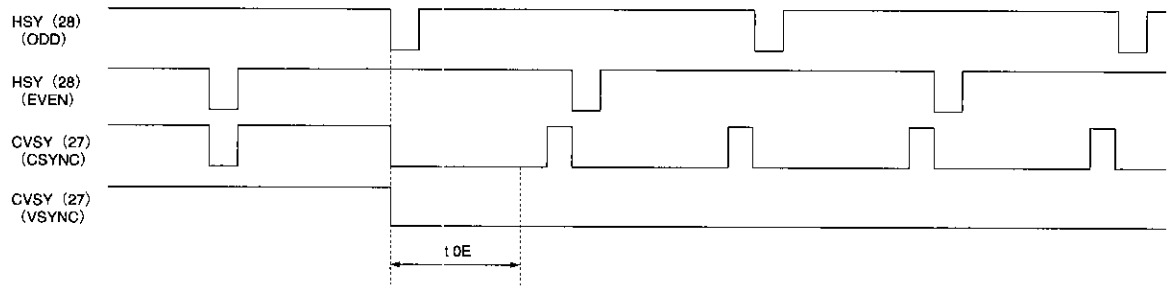


Fig. 9 Odd/even discrimination timing in the slave mode

Parameter	Symbol	Unit	Min.	Typ.	Max.
Odd/even discrimination	t 0E	BCLK	—	128	—

In the slave mode, discrimination between odd and even is based on the timing shown above. Set the CSYNC equivalent pulse input to CVSY so that CVSY does not set to the high level until the time shown above has elapsed.

PIXCLK output timing

The frequency of the PIXCLK signal output by BU1417AK is 1/4 of VCLK (or GCLK) when CLKSW is at the low level and 1/2 of VCLK (or GCLK) when CLKSW is at the high level. PIXCLK is phase-corrected in synchronization with the rise of the input (or output) of HYS.

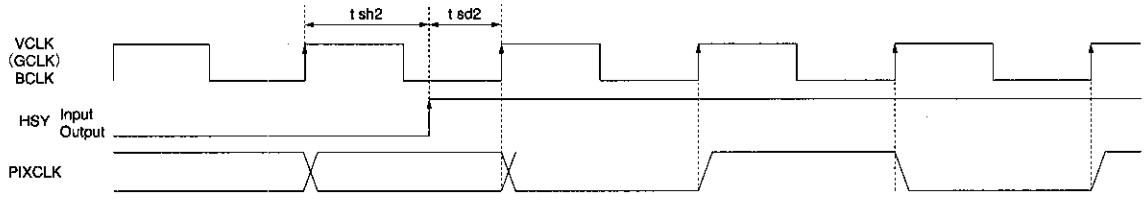


Fig. 10 PIXCLK output timing (when CLKSW = high)

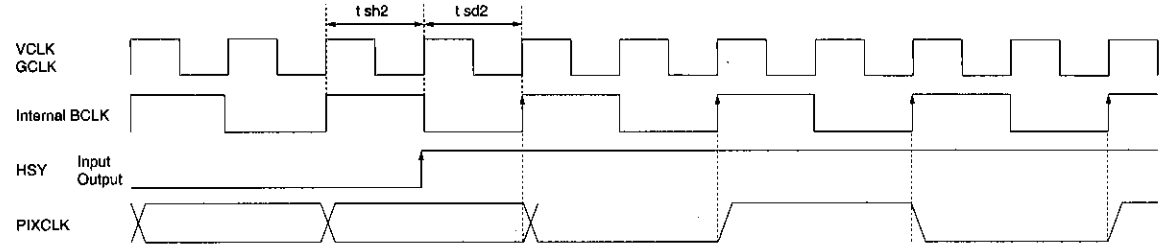


Fig. 11 PIXCLK output timing (when CLKSW = low)

Parameter	Symbol	Unit	Min.	Typ.	Max.
Input hold time, SYNC	t sh2	nS	—	37.0	—
Input hold time, SYNC	t sd2	nS	—	37.0	—

Frame timing (NTSC/PAL60 : interlaced)

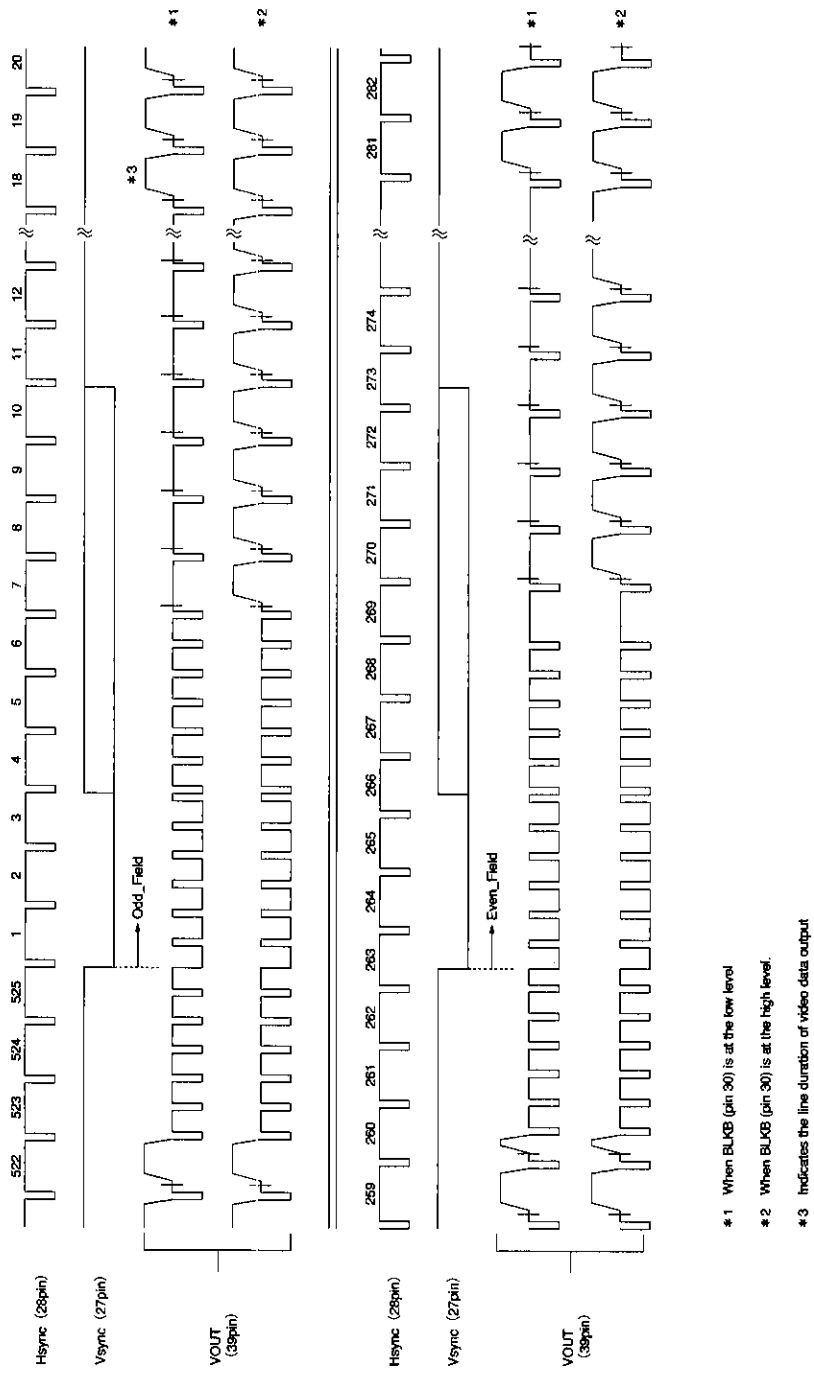


Fig. 12

Frame timing (PAL : interlaced)

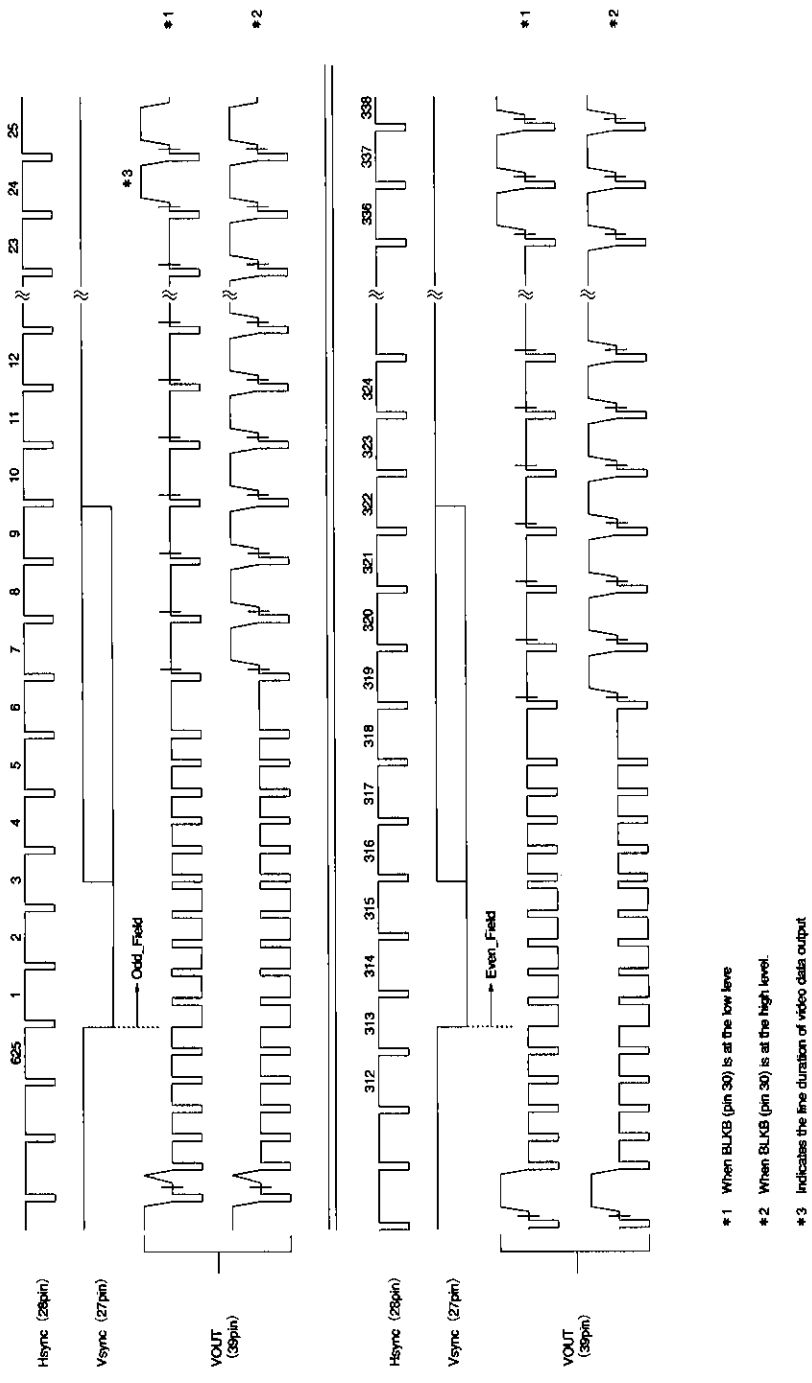


Fig. 13

Frame timing in the CD-G mode (NTSC/PAL 60 : non-interlaced)

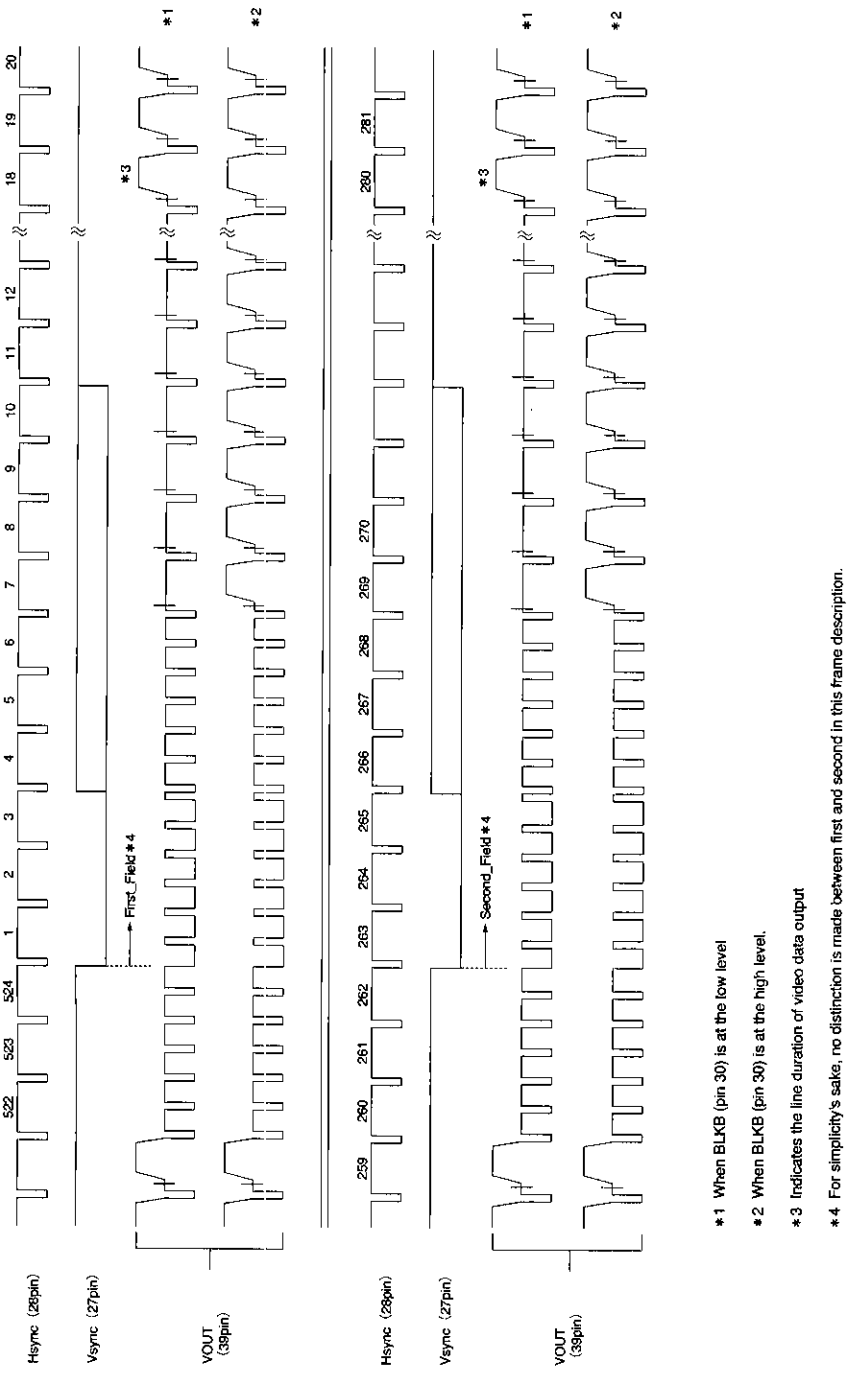
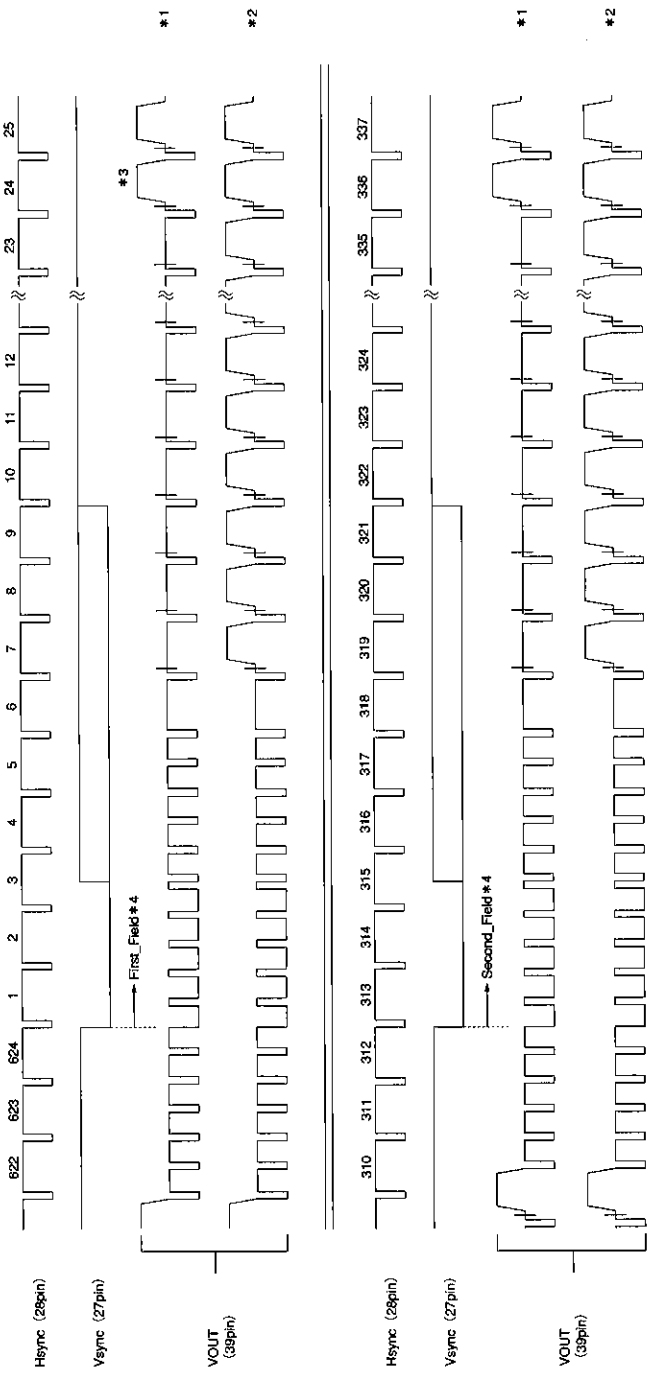


Fig. 14

Frame timing in the CD-G mode (PAL : non-interlaced)



*1 When BLKB (pin 30) is at the low level

*2 When BLKB (pin 30) is at the high level.

*3 Indicates the line duration of video data output

*4 For simplicity's sake, no distinction is made between first and second in this frame description.

Fig. 15

Television signal timing diagram (NTSC)

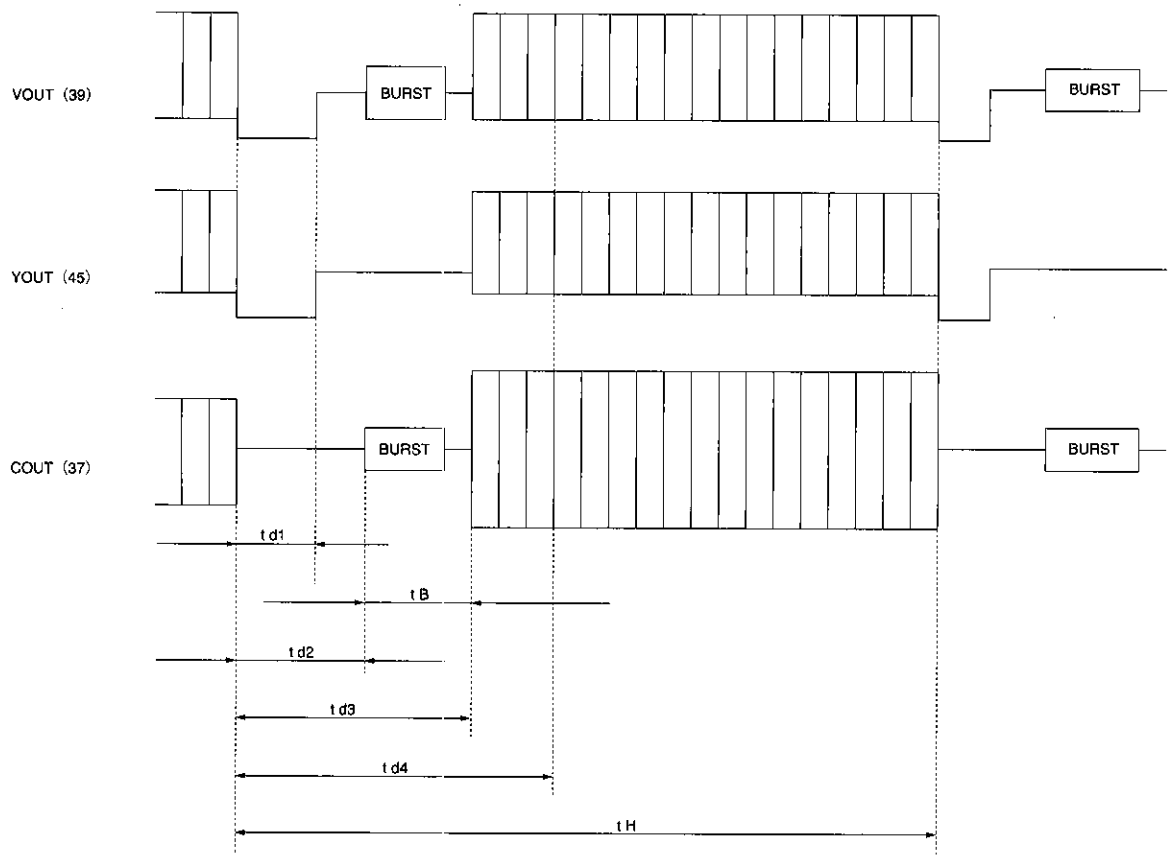


Fig. 16

Parameter	Symbol	Unit	Video - CD	CD - G	Note
SYNC rise	t d1	VCLK	128	134	Automatically generated by BU1417AK
Burst start	t d2	VCLK	142	152	Automatically generated by BU1417AK
Burst end	t d3	VCLK	212	224	Automatically generated by BU1417AK
Data valid	t d4	VCLK	254	270	Data input is blank during this period
Line duration	t H	VCLK	1716	1820	Hsync is input during this period
Burst cycle	t B	fsc	9	9	Automatically generated by BU1417AK

* The VCLK counts above apply when CLKSW is at the low level.

Television signal timing diagram (PAL/PAL60)

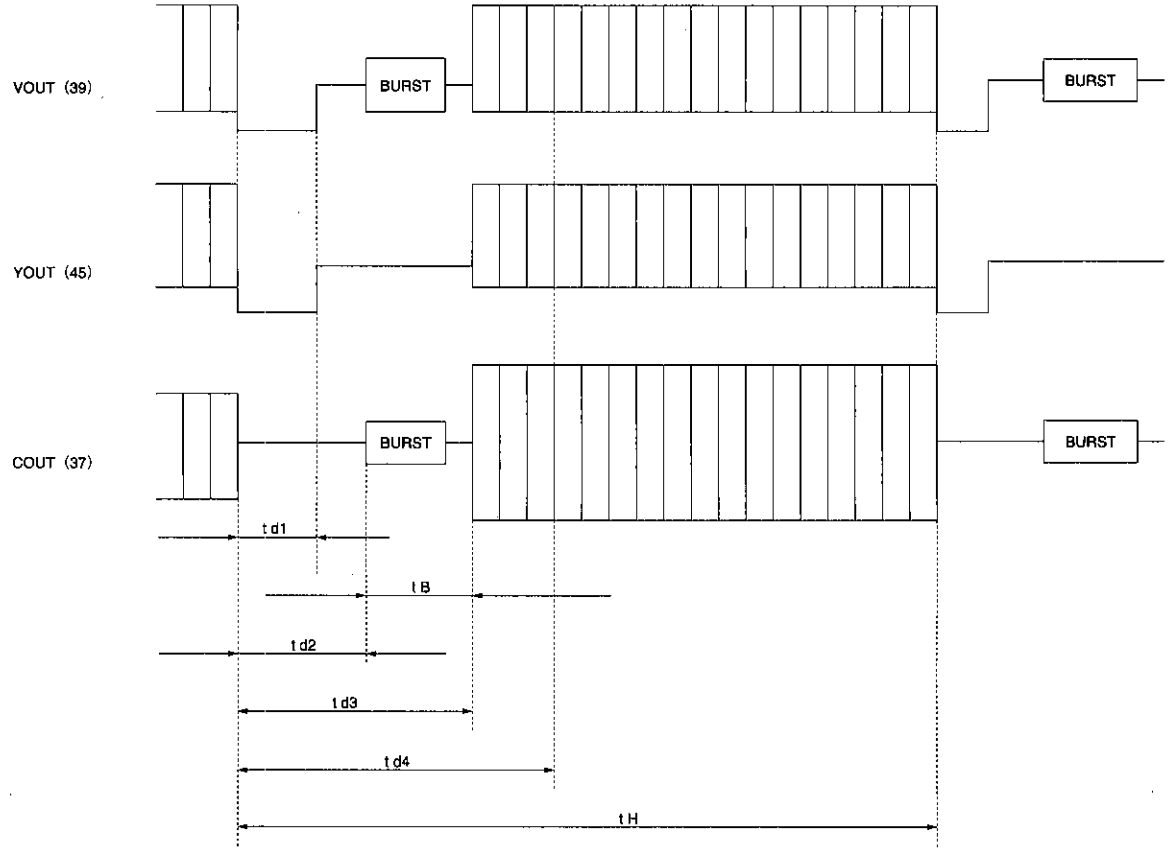


Fig. 17

Parameter	Symbol	Unit	PAL		PAL60		Notes
			V - CD	CD - G	V - CD	CD - G	
SYNC rise	t d1	VCLK	128	134	128	314	Automatically generated by BU1417AK
Burst start	t d2	VCLK	152	158	142	150	Automatically generated by BU1417AK
Burst end	t d3	VCLK	512	224	212	222	Automatically generated by BU1417AK
Data valid	t d4	VCLK	284	298	254	204	Data input is blank during this period
Line duration	t H	VCLK	1728	1816	1716	1804	Hsync is input during this period
Burst cycle	t B	fsc	9	9	9	9	Automatically generated by BU1417AK

*The VCLK counts above apply when CLKSW is at the low level.

(5) DAC output level adjustment

The DAC output level is determined by the internal DAC output current and the attached DAC output resistor. The output current of each DAC bit is determined by the VREF pin (pin 35) voltage and by the resistor attached to the IR pin (pin 42) (see below).

I (1LSB) = VVREF / (RIR + R0) × 1 / 16[A] (equation 5-1)

VVREF : voltage impressed on VREF [V]
RIR : resistor attached to IR [Ω]
R0 : Internal parasitic resistance of IC (Approx. 70Ω) [Ω]

Thus, when VVREF = 1.29V and RIR = 1.2kΩ, the current output for each LSB is 63.48 μA. The white level of Y has a digital value of 396 (decimal) and therefore is calculated as follows :

V (Y white) = 0.06348 × 396 = 25.14 [mA]

If a 37.5Ω resistor is attached to DAC output, amplitude is 0.943 [V_{P-P}].

Similarly, when VVREF = 1.29V and RIR = 1.6kΩ, a per-LSB current of 48.28 μA is output. The white level of the Y signal has a digital value of 396 (in decimal) and therefore equals the following :

V (Y white) = 0.04828 × 396 = 19.12 (mA)

If a 50.0Ω resistor is attached to DAC output, amplitude is 0.965 [V_{P-P}].

The DAC output level can be fine-tuned according to equation 5-1 above. Please contact ROHM when using constants that differ significantly from those above (i.e., output level = 1V_{P-P}, VVREF = 1.29V, RIR = 1.2kΩ or 1.6kΩ, attached DAC output resistor = 37.5Ω or 50.0kΩ).

●Application example

(1) Master mode example

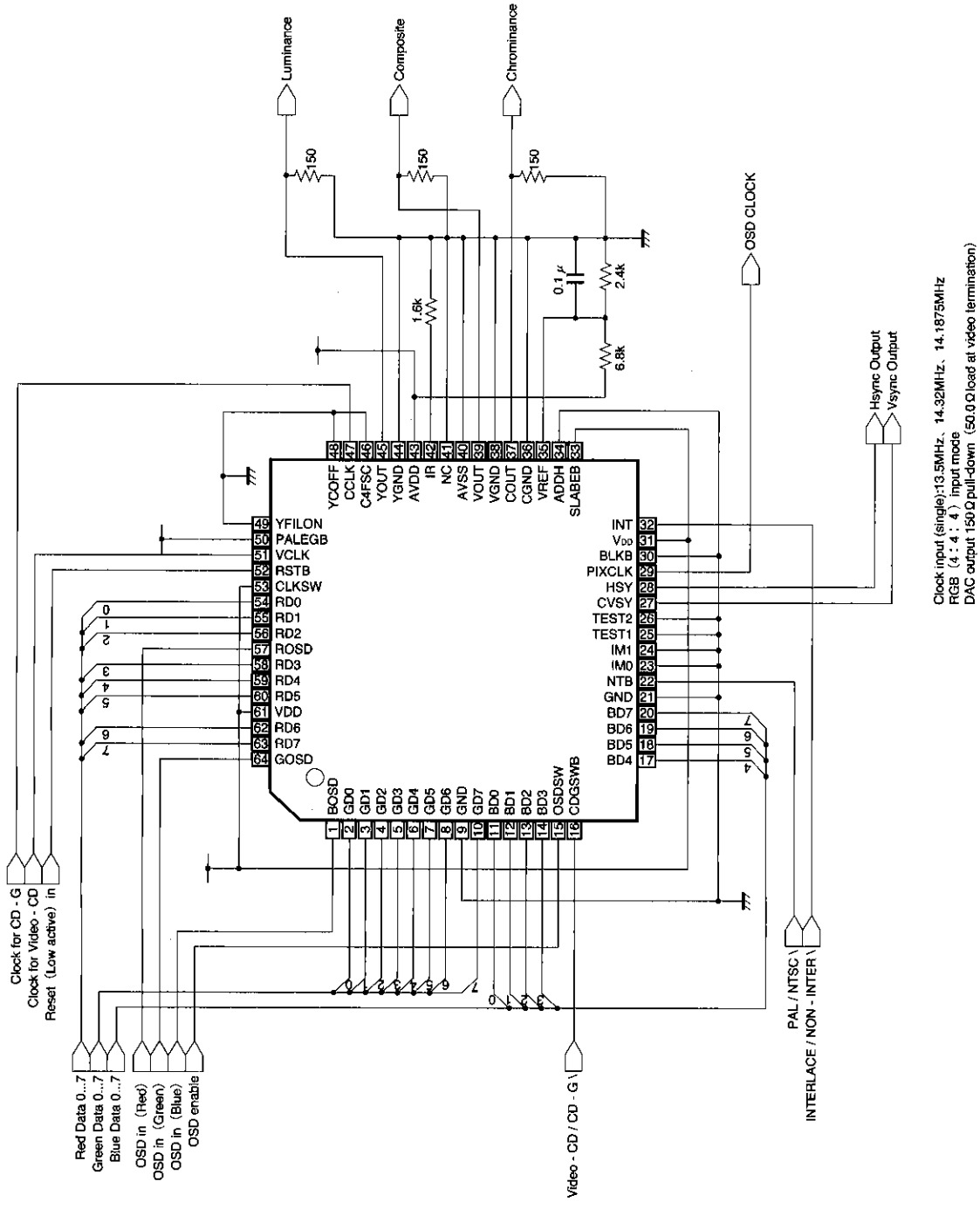


Fig. 18

(2) Slave mode example

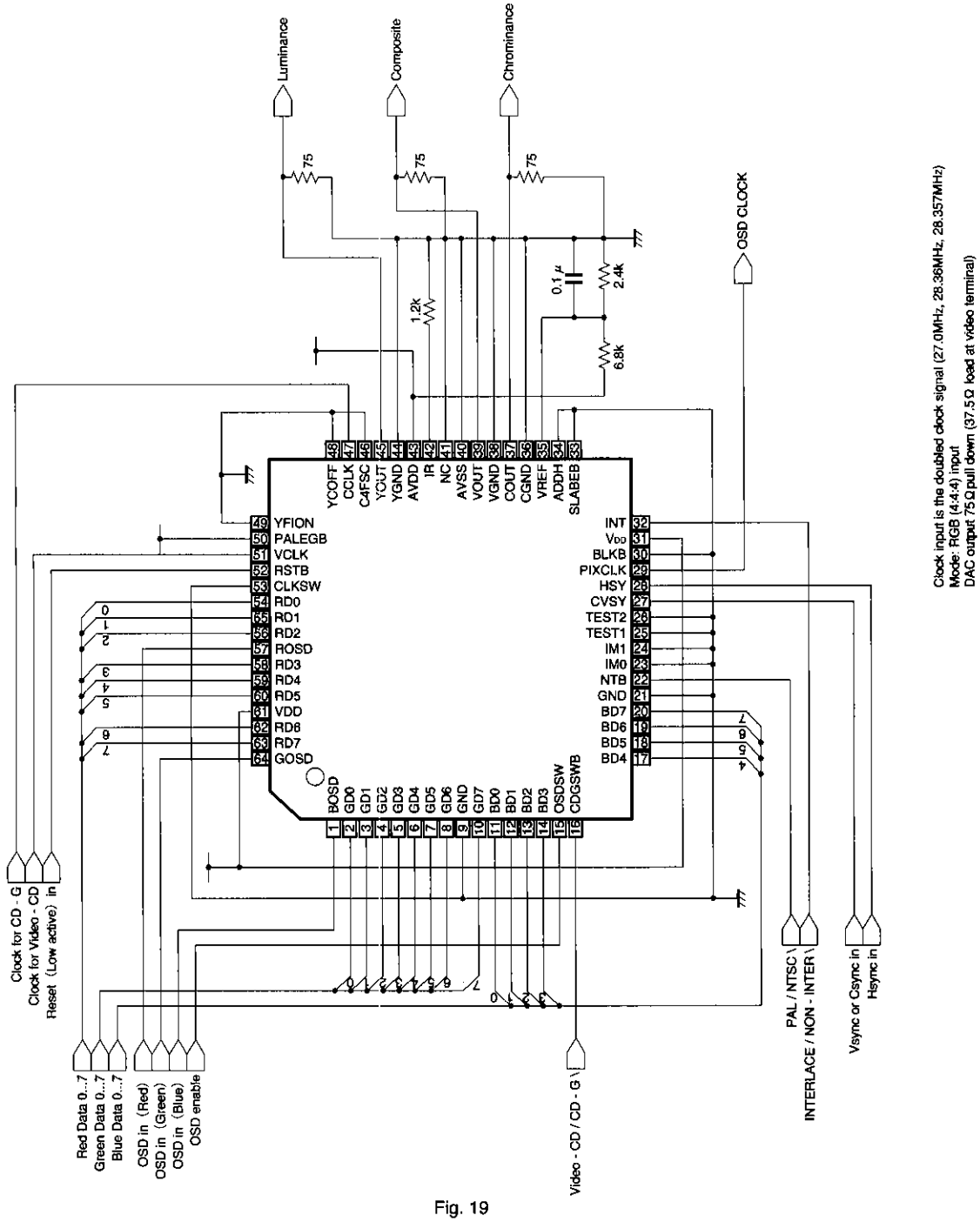
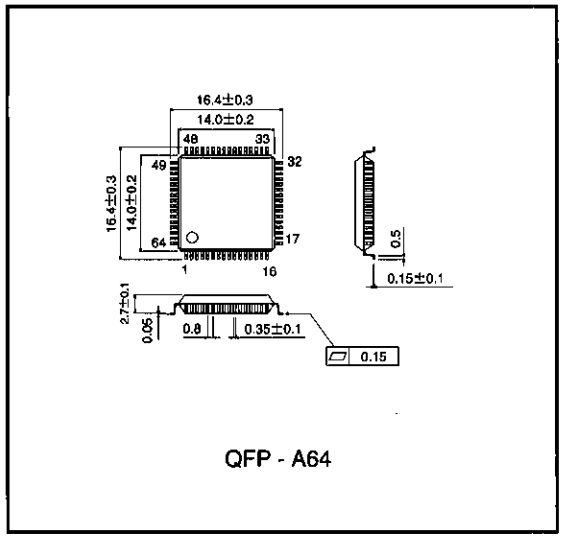


Fig. 19

●External dimensions (Units: mm)



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