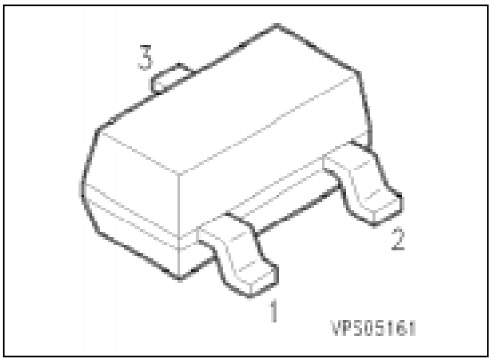
SIEMENS

Silicon N Channel MOSFET Triode — BF 999

- For high-frequency stages up to 300 MHz, preferably in FM applications



Type	Marking	Ordering Code (tape and reel)	Pin Configuration 1	2	3	Package[1)]
BF 999	LB	Q62702-F1132	G	D	S	SOT-23

Maximum Ratings

Parameter	Symbol	Values	Unit
Drain-source voltage	V_{DS}	20	V
Drain current	I_D	30	mA
Gate-source peak current	$\pm I_{GSM}$	10	
Total power dissipation, $T_A \leq 60$ ˚C	P_{tot}	200	mW
Storage temperature range	T_{stg}	– 55 … + 150	˚C
Channel temperature	T_{ch}	150	

Thermal Resistance

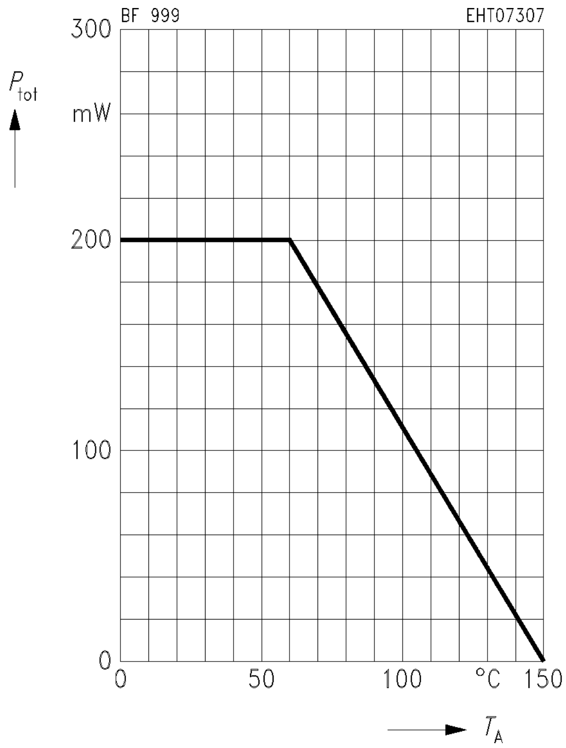
Junction - ambient [2)]	$R_{th\,JA}$	≤ 450	K/W

1) For detailed information see chapter Package Outlines.
2) Package mounted on alumina 15 mm × 16.7 mm × 0.7 mm.

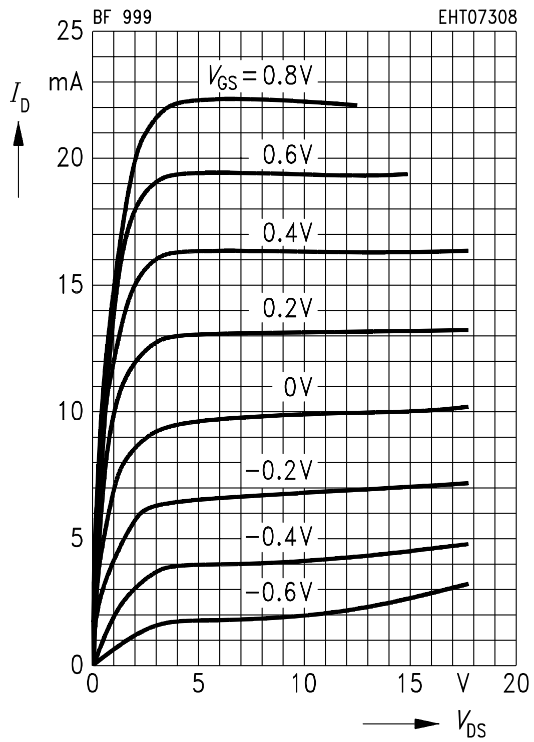
Electrical Characteristics
at T_A = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Drain-source breakdown voltage I_D = 10 μA, – V_{GS} = 4 V	$V_{(BR) DS}$	20	–	–	V
Gate-source breakdown voltage ± I_{GS} = 10 mA, V_{DS} = 0	± $V_{(BR) GSS}$	6.5	–	12	
Gate-source leakage current ± V_{GS} = 5 V, V_{DS} = 0	± I_{GSS}	–	–	50	nA
Drain current V_{DS} = 10 V, V_{GS} = 0	I_{DSS}	5	–	18	mA
Gate-source pinch-off voltage V_{DS} = 10 V, I_D = 20 μA	– $V_{GS (p)}$	–	–	2.5	V
AC Characteristics					
Forward transconductance V_{DS} = 10 V, I_D = 10 mA, f = 1 kHz	g_{fs}	14	16	–	mS
Gate input capacitance V_{DS} = 10 V, I_D = 10 mA, f = 1 MHz	C_{gss}	–	2.5	–	pF
Reverse transfer capacitance V_{DS} = 10 V, I_D = 10 mA, f = 1 MHz	C_{dg}	–	25	–	fF
Output capacitance V_{DS} = 10 V, I_D = 10 mA, f = 1 MHz	C_{dss}	–	1	–	pF
Power gain (test circuit) V_{DS} = 10 V, I_D = 10 mA, f = 200 MHz, G_G = 2 mS, G_L = 0.5 mS	G_p	–	25	–	dB
Noise figure (test circuit) V_{DS} = 10 V, I_D = 10 mA, f= 200 MHz, G_G = 2 mS, G_L = 0.5 mS	F	–	1	–	

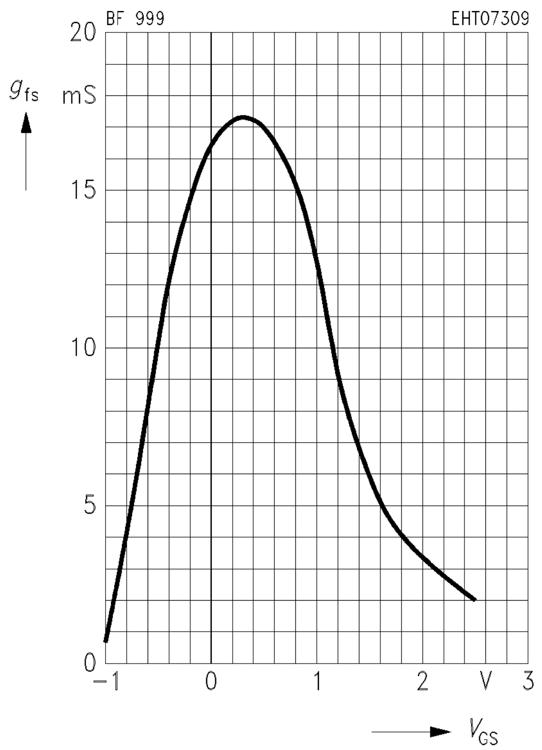
Total power dissipation $P_{tot} = f(T_A)$



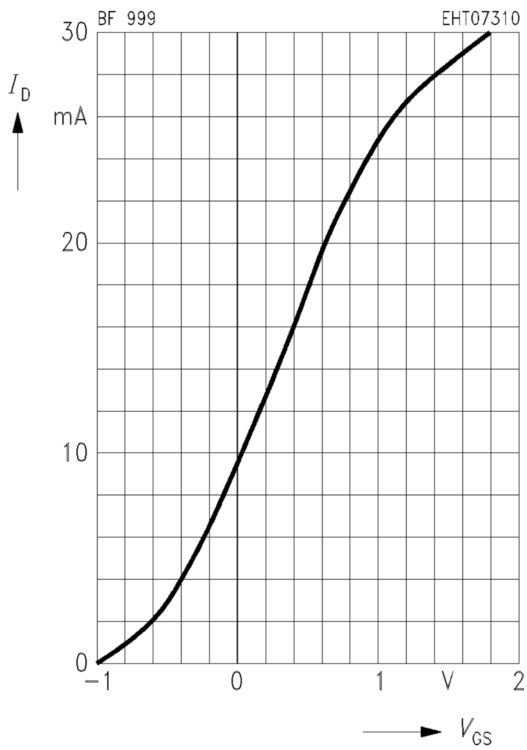
Output characteristics $I_D = f(V_{DS})$



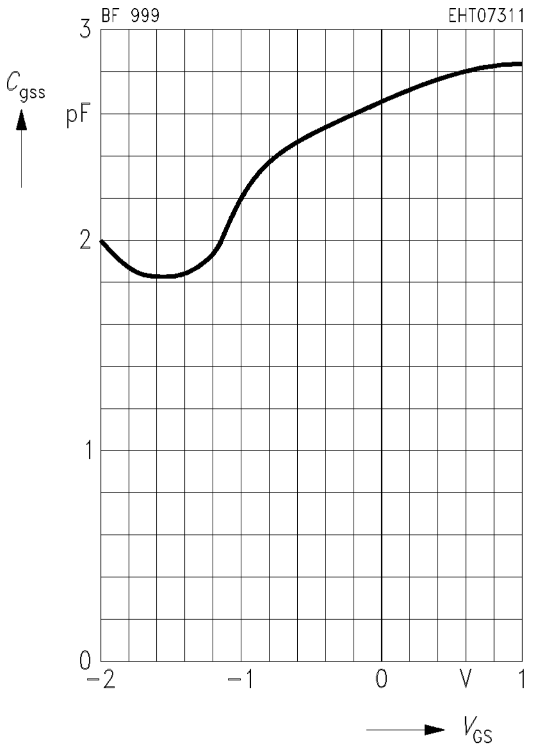
Gate transconductance $g_{fs} = f(V_{GS})$
V_{DS} = 10 V, I_{DSS} = 10 mA, f = 1 kHz



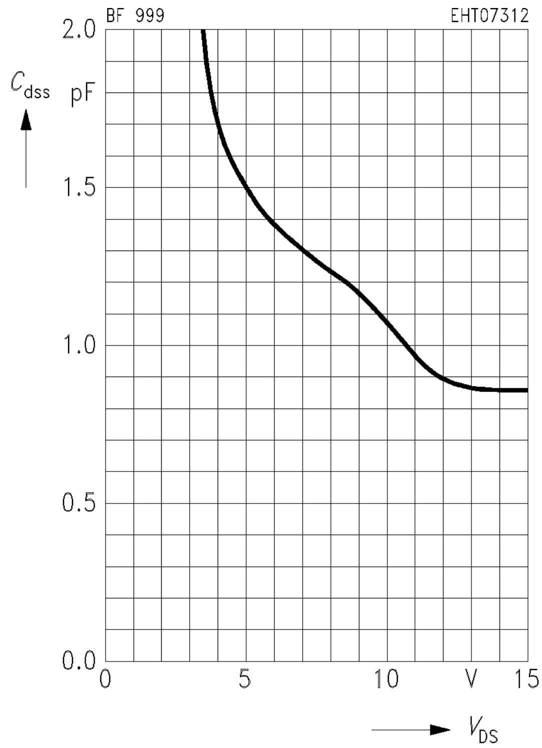
Drain current $I_D = f(V_{GS})$
V_{DS} = 10 V



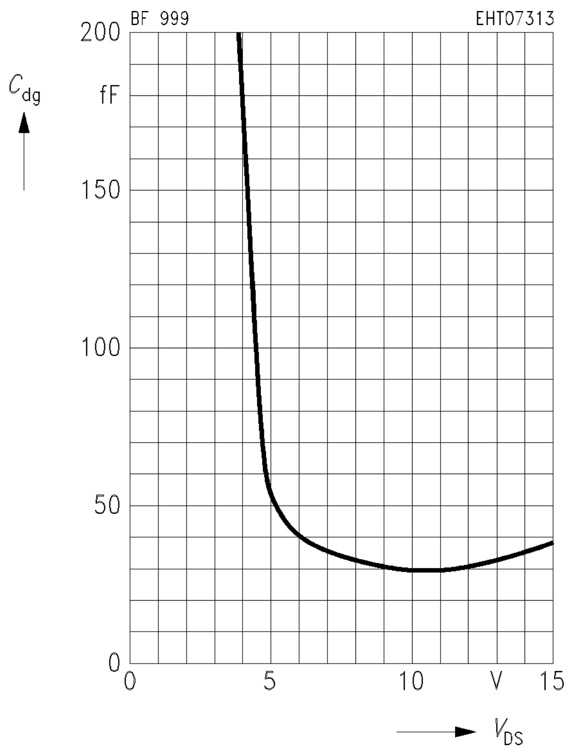
Gate input capacitance $C_{gss} = f\ (V_{GS})$
V_{DS} = 10 V, I_{DSS} = 10 mA, f = 1 MHz



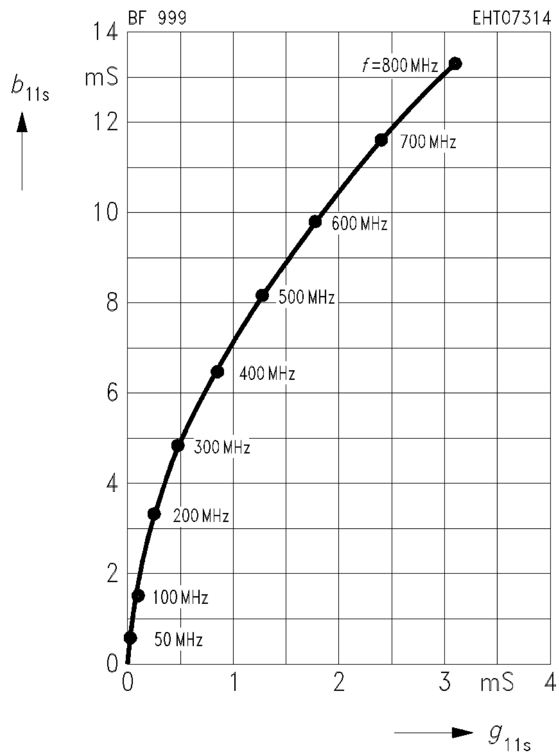
Output capacitance $C_{dss} = f\ (V_{DS})$
V_{GS} = 0, I_{DSS} = 10 mA, f = 1 MHz



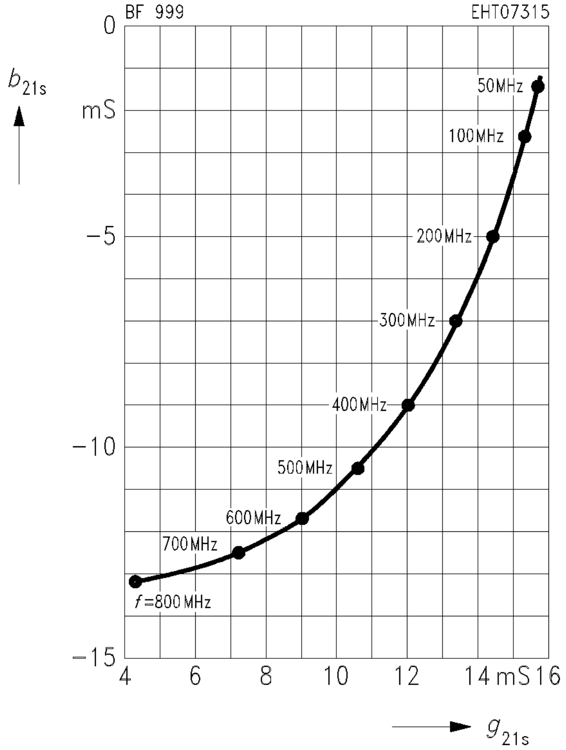
Reverse transfer capacitance
$C_{dg} = f\ (V_{DS})$
I_{DSS} = 10 mA, f = 1 MHz, V_{GS} = 0



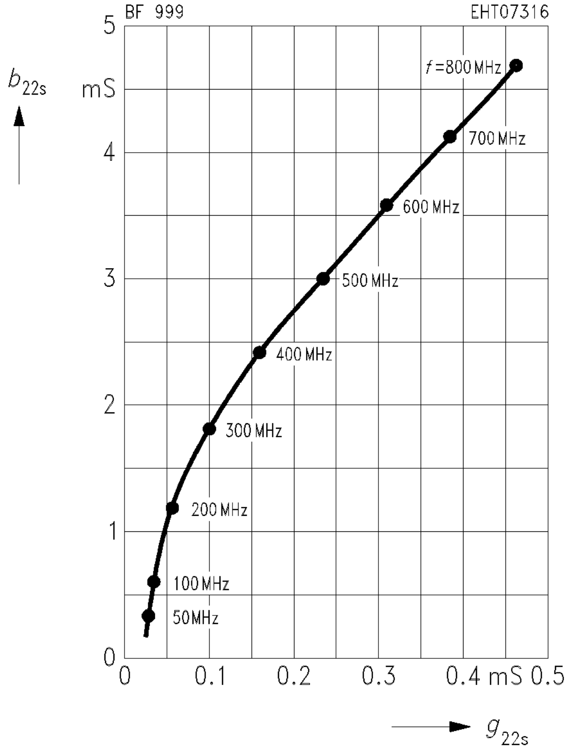
Gate input admittance y_{11s}
V_{DS} = 10 V, V_{GS} = 0,
I_{DSS} = 10 mA, (common-source)



Gate forward transfer admittance y_{21s}
V_{DS} = 10 V, V_{GS} = 0,
I_{DSS} = 10 mA, (common-source)



Output admittance y_{22s}
V_{DS} = 10 V, V_{GS} = 0,
I_{DSS} = 10 mA, (common-source)



Test circuit for power gain and noise figure
f = 200 MHz