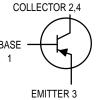
PNP Silicon Transistor

BF721T1

Motorola Preferred Device

PNP SILICON TRANSISTOR SURFACE MOUNT





MAXIMUM RATINGS

Rating	Symbol	Value	Unit	
Collector-Emitter Voltage	VCEO	-300	Vdc	
Collector-Base Voltage	V _{СВО}	-300	Vdc	
Collector-Emitter Voltage	VCER	-300	Vdc	
Emitter-Base Voltage	V _{EBO}	-5.0	Vdc	
Collector Current	IC	-100	mAdc	
Total Power Dissipation up to $T_A = 25^{\circ}C^{(1)}$	PD	1.5	Watts	
Storage Temperature Range	T _{stg}	-65 to +150	°C	
Junction Temperature	TJ	150	°C	



DEVICE MARKING

DF

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance from Junction to Ambient(1)	$R_{ heta JA}$	83.3	°C/W

$\textbf{ELECTRICAL CHARACTERISTICS} \ (T_A = 25^{\circ}\text{C unless otherwise noted})$

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I _C = -1.0 mAdc, I _B = 0)	V(BR)CEO	-300	_	Vdc
Collector-Base Breakdown Voltage (I _C = -100 μAdc, I _E = 0)	V(BR)CBO	-300	_	Vdc
Collector-Emitter Breakdown Voltage (I _C = –100 μAdc, R _{BE} = 2.7 kΩ)	V(BR)CER	-300	_	Vdc
Emitter-Base Breakdown Voltage ($I_E = -10 \mu Adc$, $I_C = 0$)	V(BR)EBO	-5.0	_	Vdc
Collector-Base Cutoff Current (V _{CB} = -200 Vdc, I _E = 0)	ICBO	_	-10	nAdc
Collector–Emitter Cutoff Current (V _{CE} = -250 Vdc, R _{BE} = 2.7 k Ω) (V _{CE} = -200 Vdc, R _{BE} = 2.7 k Ω , T _J = 150 °C)	ICER		-50 -10	nAdc μAdc

^{1.} Device mounted on a glass epoxy printed circuit board 1.575 in. x 1.575 in. x 0.059 in.; mounting pad for the collector lead min. 0.93 in².

Thermal Clad is a trademark of the Bergquist Company

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3



BF721T1

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS				
DC Current Gain (V _{CE} = -25 mAdc, V _{CE} = -20 Vdc)	h _{FE}	50	_	
Collector-Emitter Saturation Voltage (I _C = -30 mAdc, I _B = -5.0 mAdc)	VCE(sat)	_	-0.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product $(V_{CE} = -10 \text{ Vdc}, I_{C} = -10 \text{ mAdc}, f = 35 \text{ MHz})$	fΤ	60	_	MHz
Feedback Capacitance ($V_{CE} = -30 \text{ Vdc}$, $I_{C} = 0$, $f = 1.0 \text{ MHz}$)	C _{re}	_	1.6	pF

INFORMATION FOR USING THE SOT-223 SURFACE MOUNT PACKAGE

POWER DISSIPATION

The power dissipation of the SOT-223 is a function of the pad size. These can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, T_{A} . Using the values provided on the data sheet for the SOT-223 package, P_{D} can be calculated as follows.

$$P_D = \frac{T_{J(max)} - T_{A}}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into

the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 1.5 watts.

$$P_D = \frac{150^{\circ}C - 25^{\circ}C}{83.3^{\circ}C/W} = 1.5 \text{ watts}$$

The 83.3° C/W for the SOT-223 package assumes the recommended collector pad area of 965 sq. mils on a glass epoxy printed circuit board to achieve a power dissipation of 1.5 watts. If space is at a premium, a more realistic approach is to use the device at a P_D of 833 mW using the footprint shown. Using a board material such as Thermal Clad, a power dissipation of 1.6 watts can be achieved using the same footprint.

MOUNTING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

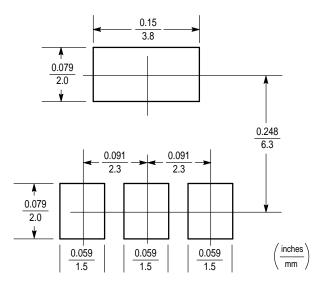
- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.

- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes.
 Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling
- * Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

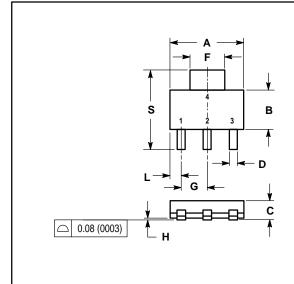
Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

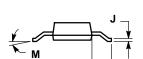
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-223

PACKAGE DIMENSIONS





CASE 318E-04 ISSUE H TO-261AA

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.249	0.263	6.30	6.70
В	0.130	0.145	3.30	3.70
С	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
Н	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
М	0°	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

STYLE 1:

PIN 1. BASE

- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

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