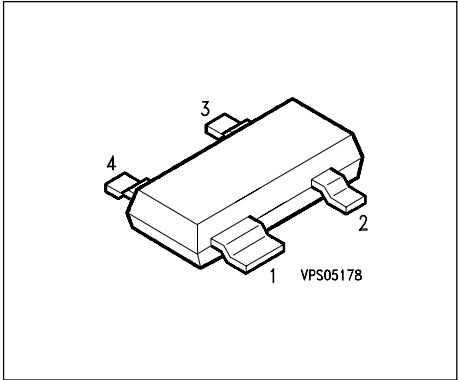
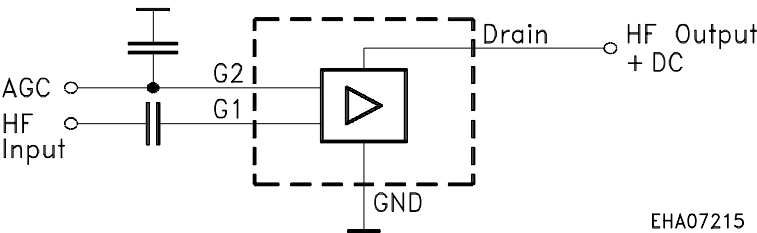


Silicon N-Channel MOSFET Tetrode



ESD: Electrostatic discharge sensitive device, observe handling precaution!

Type	Marking	Ordering Code	PIN Configuration				Package
BF 1012S	NYs	Q62702-F1627	1 = S	2 = D	3 = G ₂	4 = G ₁	SOT-143

Maximum Ratings

Parameter	Symbol	Values	Unit
Drain-source voltage	V_{DS}	16	V
Continuos drain current	I_D	25	mA
Gate 1/gate 2 peak source current	$\pm I_{G1/2SM}$	10	
Gate 1 (external biasing)	$+V_{G1SE}$	3	V
Total power dissipation, $T_S \leq 76^\circ\text{C}$	P_{tot}	200	mW
Storage temperature	T_{stg}	- 55 ... + 150	$^\circ\text{C}$
Channel temperature	T_{ch}	150	

Thermal Resistance

Channel - soldering point	R_{thchs}	≤ 370	K/W
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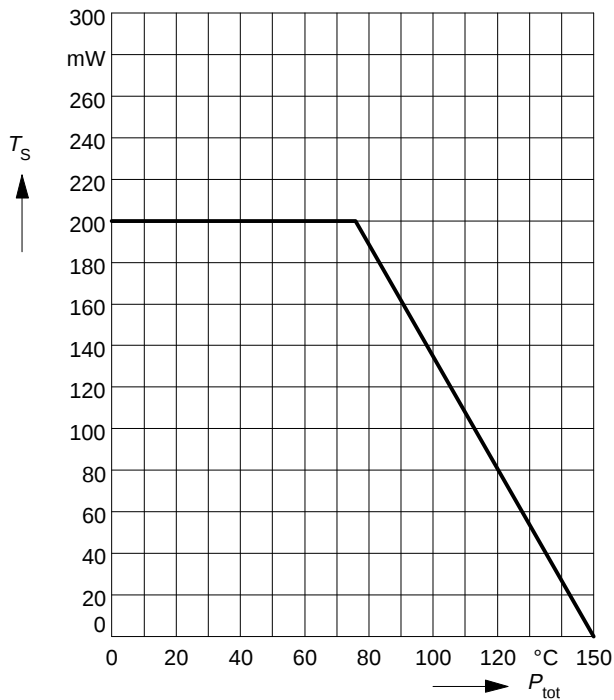
Electrical Characteristics at TA = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Drain-source breakdown voltage $I_D = 300\text{ }\mu\text{A}$, $-V_{G1S} = 4\text{ V}$, $-V_{G2S} = 4\text{ V}$	$V_{(BR)DS}$	16	-	-	V
Gate 1 - source breakdown voltage $+I_{G1S} = 10\text{ mA}$, $V_{G2S} = 0\text{ V}$, $V_{DS} = 0\text{ V}$	$+V_{(BR)G1SS}$	8	-	12	
Gate 2 source breakdown voltage $\pm I_{G2S} = 10\text{ mA}$, $V_{G1S} = 0$, $V_{DS} = 0$	$\pm V_{(BR)G2SS}$	10	-	16	
Gate 1 source current $V_{G1S} = 6\text{ V}$, $V_{G2S} = 0\text{ V}$	$+I_{G1SS}$	-	-	60	μA
Gate 2 source leakage current $\pm V_{G2S} = 8\text{ V}$, $V_{G1S} = 0$, $V_{DS} = 0$	$\pm I_{G2SS}$	-	-	50	nA
Drain current $V_{DS} = 12\text{ V}$, $V_{G1S} = 0$, $V_{G2S} = 6\text{ V}$	I_{DSS}	-	-	500	μA
Operating current (selfbiased) $V_{DS} = 12\text{ V}$, $V_{G2S} = 6\text{ V}$	I_{DSO}	8	12	-	mA
Gate 2-source pinch-off voltage $V_{DS} = 12\text{ V}$, $I_D = 100\text{ }\mu\text{A}$	$V_{G2S(p)}$	-	0.9	-	V

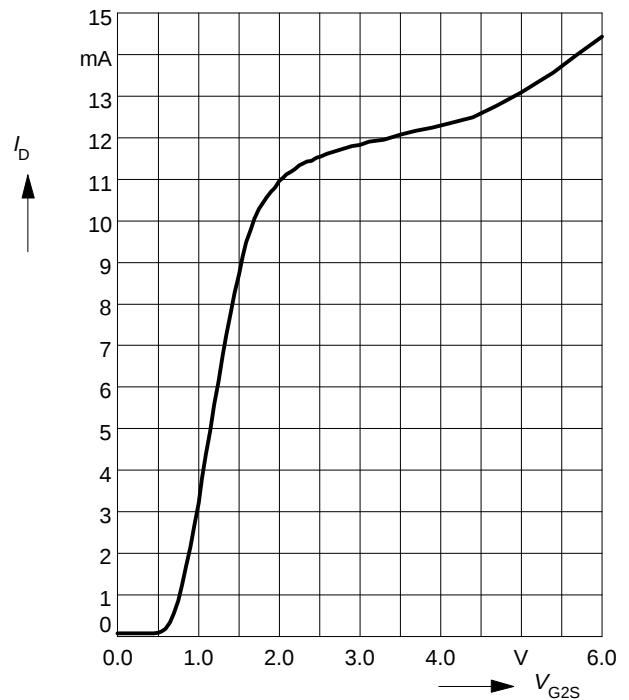
AC Characteristics

Forward transconductance (self biased) $V_{DS} = 12 V$, $V_{G2S} = 6 V$, $f = 1 kHz$	g_{fs}	26	30	-	mS
Gate 1-input capacitance (self biased) $V_{DS} = 12 V$, $V_{G2S} = 6 V$, $f = 1 MHz$	C_{g1ss}	-	2.1	2.7	pF
Output capacitance (self biased) $V_{DS} = 12 V$, $V_{G2S} = 6 V$, $f = 1 MHz$	C_{dss}	-	0.9	-	
Power gain (self biased) $V_{DS} = 12 V$, $V_{G2S} = 6 V$, $f = 800 MHz$	G_{ps}	18	22	-	dB
Noise figure (self biased) $V_{DS} = 12 V$, $V_{G2S} = 6 V$, $f = 800 MHz$	F_{800}	-	1.4	-	
Gain control range (self biased) $V_{DS} = 12 V$, $V_{G2S} = 1 V$, $f = 800 MHz$	ΔG_{ps}	40	50	-	

Total power dissipation $P_{\text{tot}} = f(T_S)$



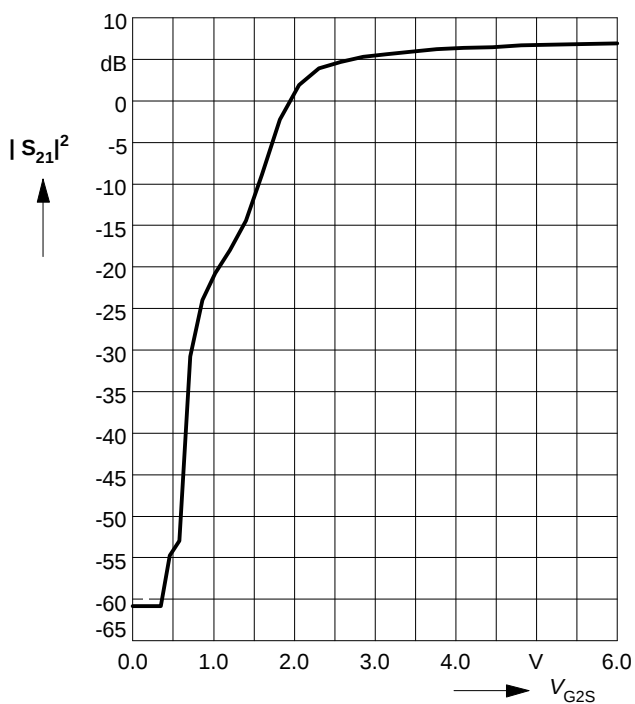
Drain current $I_D = f(V_{G2S})$



Insertion power gain

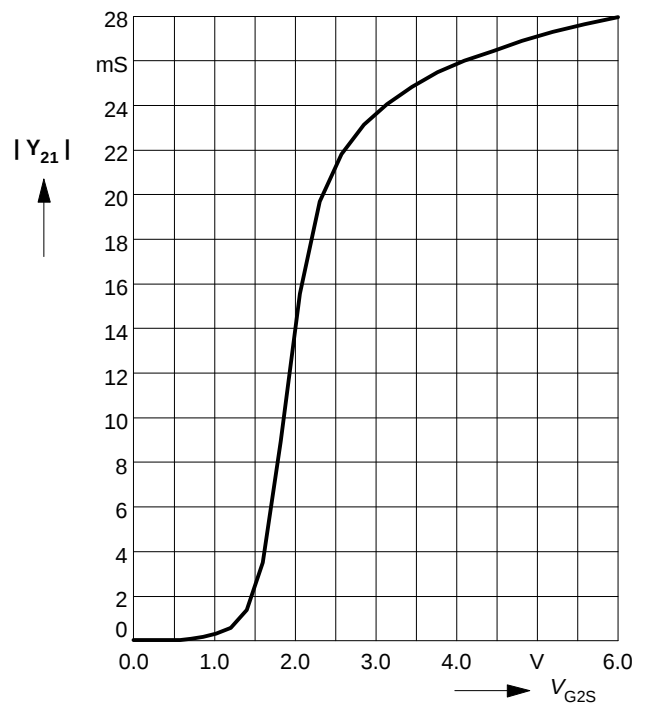
$$|S_{21}|^2 = f(V_{G2S})$$

$f = 800\text{MHz}$

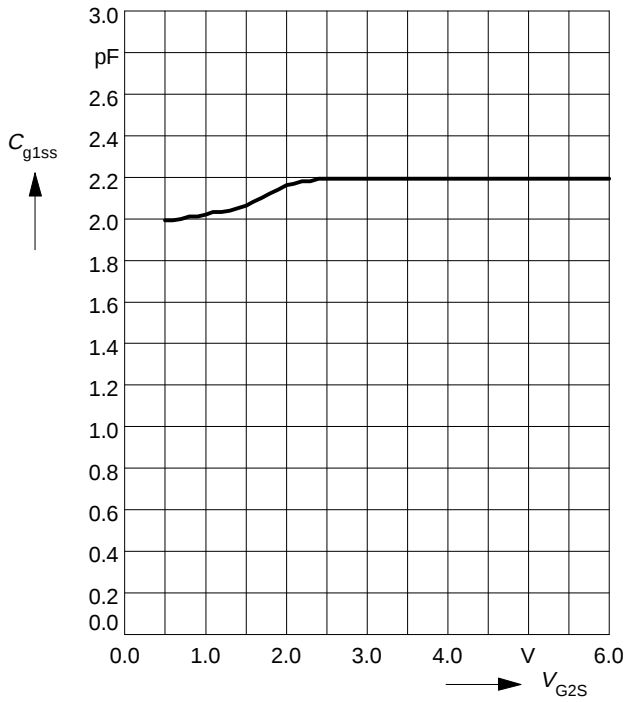


Forward transfer admittance

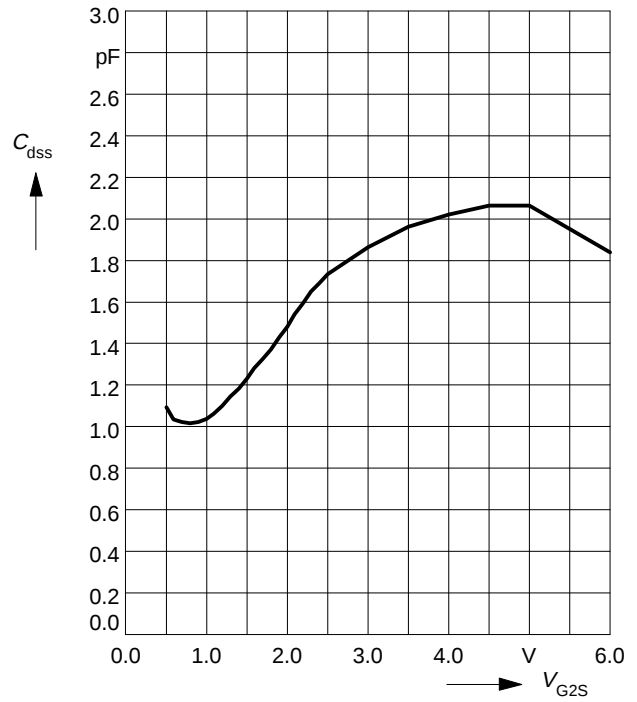
$$|Y_{21}| = f(V_{G2S})$$



Gate 1 input capacitance $C_{g1ss} = f(V_{G2S})$
 $f=1\text{MHz}$



Output capacitance $C_{dss} = f(V_{G2})$
 $f=1\text{MHz}$



Technical drawing of a 4-pin DIN 6784 connector. The drawing includes a top view and a side view.

Top View Dimensions:

- Total width: 2.9 ± 0.1
- Pin pitch: 1.9
- Pin diameter: $0.4^{+0.1}_{-0.05}$
- Body thickness: $0.8^{+0.1}_{-0.05}$
- Pin 1 and 2 are on the left, Pin 3 and 4 are on the right.

Side View Dimensions:

- Maximum height: 1.0 max
- Minimum height: 0.6 min
- Maximum width: 1.1 max
- Maximum depth: 2.6 max
- Pin 1 and 2 are on the left, Pin 3 and 4 are on the right.
- Pin 1 and 2 are angled at $2^\circ \dots 30^\circ$.
- Pin 3 and 4 are angled at 10° .
- Pin 1 and 2 are positioned 0.15 and 0.08 from the top edge.
- Pin 3 and 4 are positioned 0.1 max from the top edge.
- Pin 1 and 2 are positioned 1.3 ± 0.1 from the bottom edge.
- Pin 3 and 4 are positioned 1.3 ± 0.1 from the bottom edge.

Other Information:

- Standard: $n.DIN 6784$
- Part Number: $GPS05559$