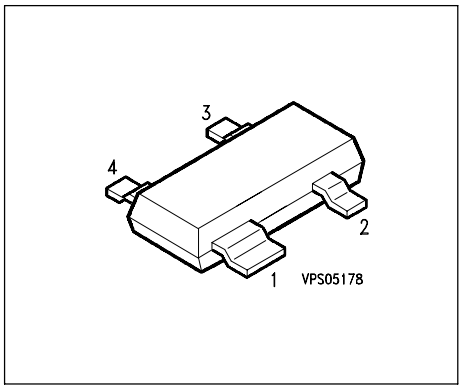
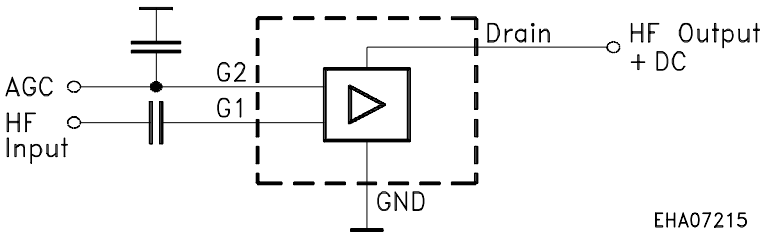
## Silicon N-Channel MOSFET Tetrode




**ESD**: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precaution!

| Type | Marking | Ordering Code | PIN Configuration | | | | Package |
|---|---|---|---|---|---|---|---|
| BF 1012S | NYs | Q62702-F1627 | 1 = S | 2 = D | 3 = $G_2$ | 4 = $G_1$ | SOT-143 |

**Maximum Ratings**

| Parameter | Symbol | Values | Unit |
|---|---|---|---|
| Drain-source voltage | $V_{DS}$ | 16 | V |
| Continuos drain current | $I_D$ | 25 | mA |
| Gate 1/gate 2 peak source current | $\pm I_{G1/2SM}$ | 10 | |
| Gate 1 (external biasing) | $+V_{G1SE}$ | 3 | V |
| Total power dissipation, $T_S \leq 76°C$ | $P_{tot}$ | 200 | mW |
| Storage temperature | $T_{stg}$ | - 55 ... + 150 | °C |
| Channel temperature | $T_{ch}$ | 150 | |

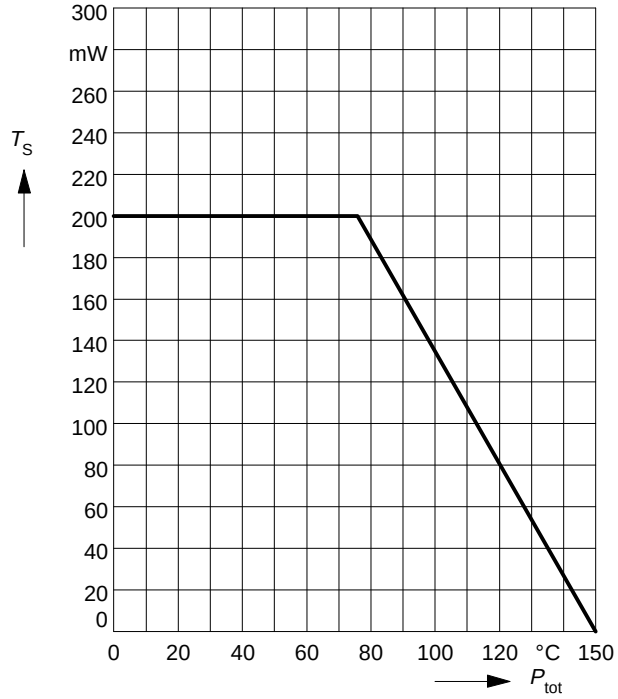
**Thermal Resistance**

| | | | |
|---|---|---|---|
| Channel - soldering point | $R_{thchs}$ | $\leq$ 370 | K/W |

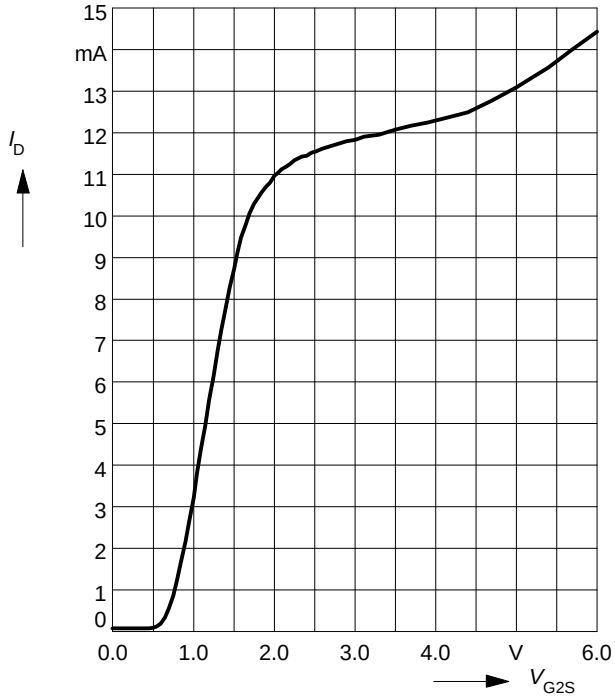
**Electrical Characteristics** at TA = 25°C, unless otherwise specified

| Parameter | Symbol | Values | | | Unit |
|---|---|---|---|---|---|
| | | min. | typ. | max. | |
| **DC Characteristics** | | | | | |
| Drain-source breakdown voltage<br>$I_D$ = 300 µA, -$V_{G1S}$ = 4 V, - $V_{G2S}$ = 4 V | $V_{(BR)DS}$ | 16 | - | - | V |
| Gate 1 - source breakdown voltage<br>+$I_{G1S}$ = 10 mA, $V_{G2S}$ = 0 V, $V_{DS}$ = 0 V | +$V_{(BR)G1SS}$ | 8 | - | 12 | |
| Gate 2 source breakdown voltage<br>±$I_{G2S}$ = 10 mA, $V_{G1S}$ = 0 , $V_{DS}$ = 0 | ±$V_{(BR)G2SS}$ | 10 | - | 16 | |
| Gate 1 source current<br>$V_{G1S}$ = 6 V, $V_{G2S}$ = 0 V | +$I_{G1SS}$ | - | - | 60 | µA |
| Gate 2 source leakage current<br>±$V_{G2S}$ = 8 V, $V_{G1S}$ = 0 , $V_{DS}$ = 0 | ±$I_{G2SS}$ | - | - | 50 | nA |
| Drain current<br>$V_{DS}$ = 12 V, $V_{G1S}$ = 0 , $V_{G2S}$ = 6 V | $I_{DSS}$ | - | - | 500 | µA |
| Operating current (selfbiased)<br>$V_{DS}$ = 12 V, $V_{G2S}$ = 6 V | $I_{DSO}$ | 8 | 12 | - | mA |
| Gate 2-source pinch-off voltage<br>$V_{DS}$ = 12 V, $I_D$ = 100 µA | $V_{G2S(p)}$ | - | 0.9 | - | V |
| **AC Characteristics** | | | | | |
| Forward transconductance (self biased)<br>$V_{DS}$ = 12 V, $V_{G2S}$ = 6 V, $f$ = 1 kHz | $g_{fs}$ | 26 | 30 | - | mS |
| Gate 1-input capacitance (self biased)<br>$V_{DS}$ = 12 V, $V_{G2S}$ = 6 V, $f$ = 1 MHz | $C_{g1ss}$ | - | 2.1 | 2.7 | pF |
| Output capacitance (self biased)<br>$V_{DS}$ = 12 V, $V_{G2S}$ = 6 V, $f$ = 1 MHz | $C_{dss}$ | - | 0.9 | - | |
| Power gain (self biased)<br>$V_{DS}$ = 12 V, $V_{G2S}$ = 6 V, $f$ = 800 MHz | $G_{ps}$ | 18 | 22 | - | dB |
| Noise figure (self biased)<br>$V_{DS}$ = 12 V, $V_{G2S}$ = 6 V, $f$ = 800 MHz | $F_{800}$ | - | 1.4 | - | |
| Gain control range (self biased)<br>$V_{DS}$ = 12 V, $V_{G2S}$ = 1 V, $f$ = 800 MHz | $\Delta G_{ps}$ | 40 | 50 | - | |

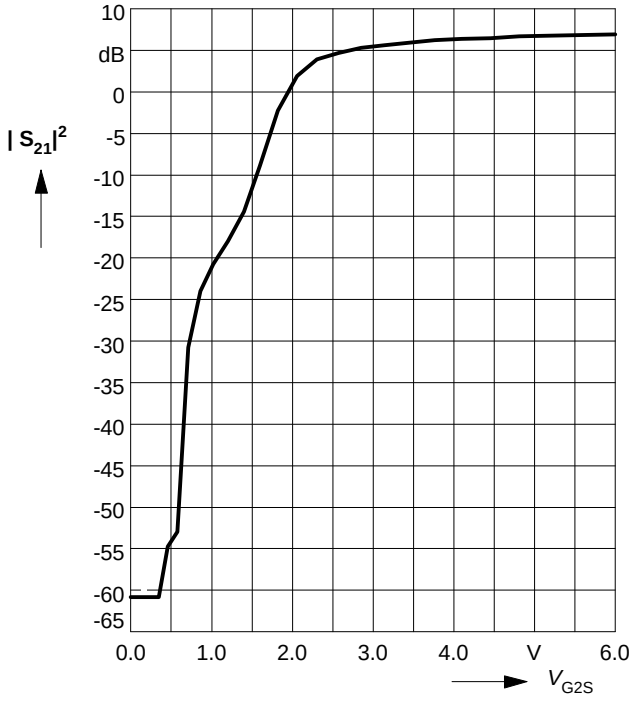
**Total power dissipation** $P_{tot} = f(T_S)$



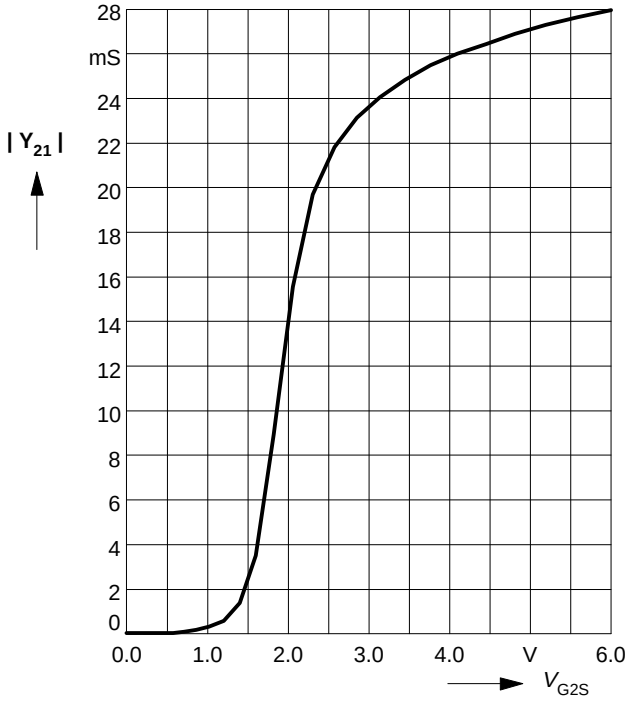

**Drain current** $I_D = f(V_{G2S})$



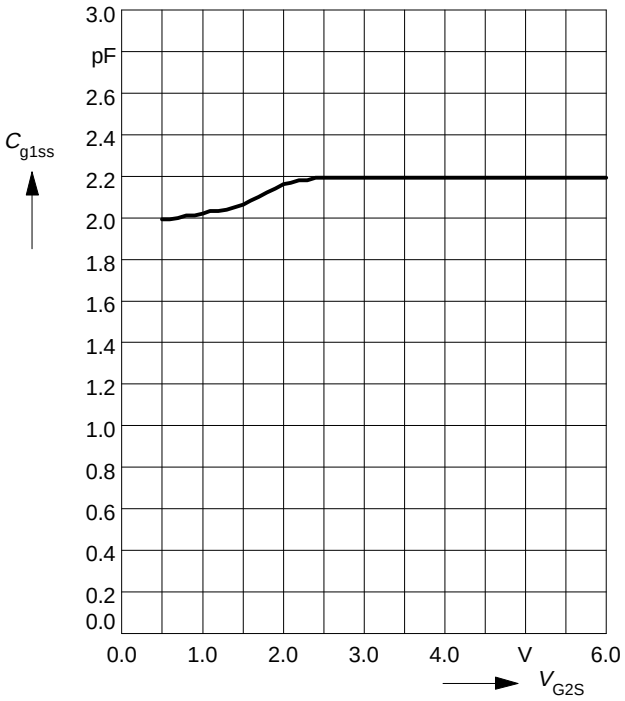

**Insertion power gain**
$|S_{21}|^2 = f(V_{G2S})$
f = 800MHz



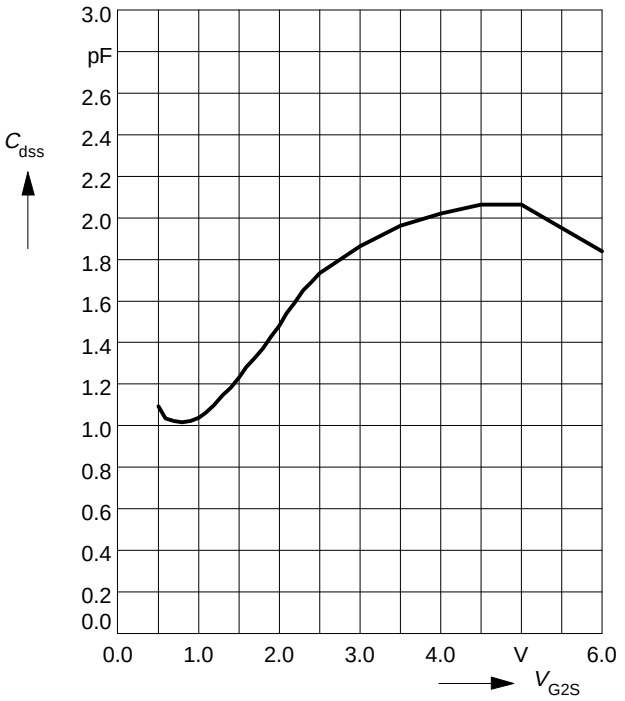

**Forward transfer admittance**
$|Y_{21}| = f(V_{G2S})$



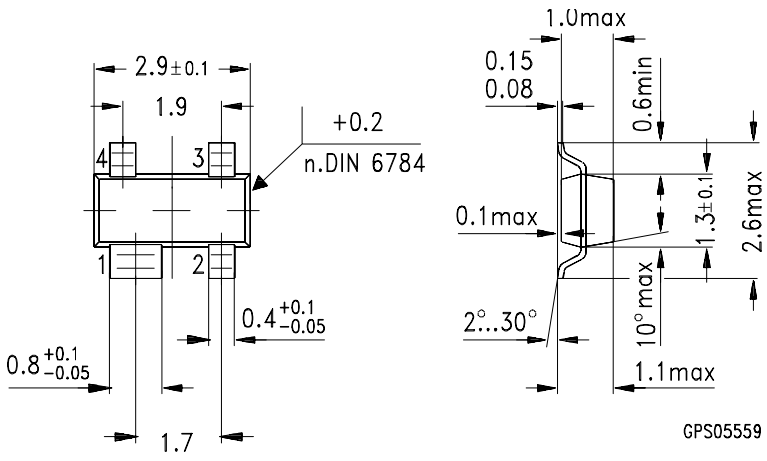
**Gate 1 input capacitance** $C_{g1ss} = f(V_{g2s})$
f=1MHz




**Output capacitance** $C_{dss} = f(V_{G2})$
f=1MHz



Package


2.9±0.1
1.9
+0.2
n.DIN 6784
4
3
1
2
0.4 +0.1 −0.05
0.8 +0.1 −0.05
1.7
1.0max
0.15
0.08
0.6min
0.1max
1.3±0.1
2.6max
2°...30°
10° max
1.1max
GPS05559