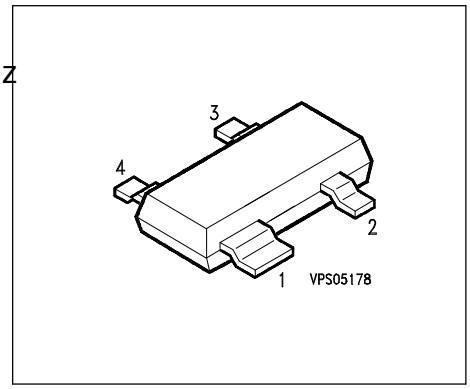
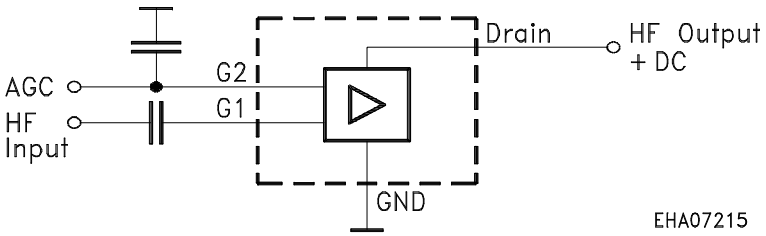
Silicon N-Channel MOSFET Tetrode

- For low-noise, high gain-controlled input stages up to 1GHz
- Operating voltage 5V
- Integrated stabilized bias network





ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precaution!

Type	Marking	Ordering Code	PIN Configuration				Package
BF 1005S	NZs	Q62702-F1665	1 = S	2 = D	3 = G_2	4 = G_1	SOT-143

Maximum Ratings

Parameter	Symbol	Values	Unit
Drain-source voltage	V_{DS}	8	V
Continuos drain current	I_D	25	mA
Gate 1/gate 2 peak source current	$\pm I_{G1/2SM}$	10	
Gate 1 (external biasing)	$+V_{G1SE}$	3	V
Total power dissipation, $T_S \leq 76°C$	P_{tot}	200	mW
Storage temperature	T_{stg}	- 55 ... + 150	°C
Channel temperature	T_{ch}	150	

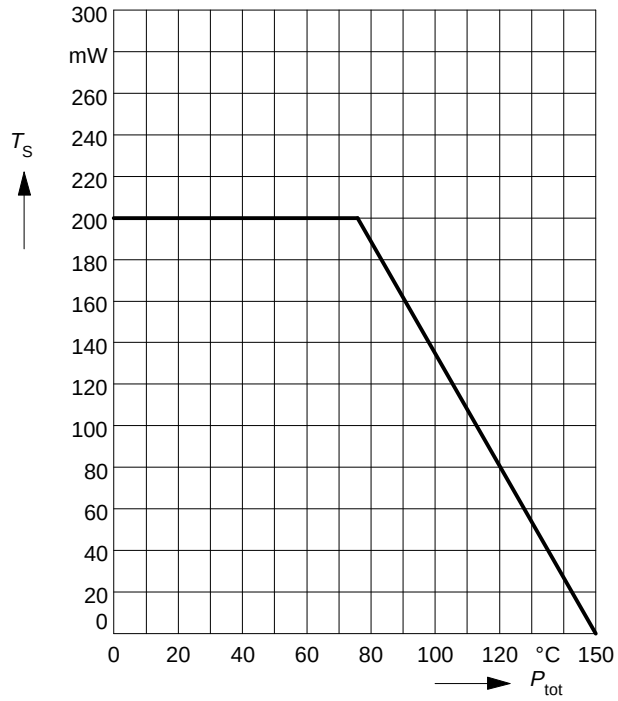
Thermal Resistance

Channel - soldering point	R_{thchs}	≤ 370	K/W

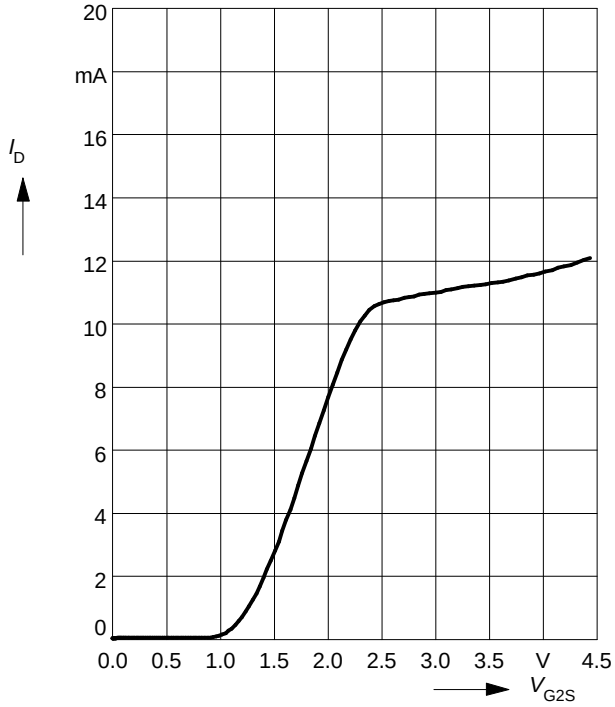
Electrical Characteristics at TA = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Drain-source breakdown voltage I_D = 650 µA, -V_{G1S} = 4 V, - V_{G2S} = 4 V	$V_{(BR)DS}$	12	-	-	V
Gate 1 - source breakdown voltage +I_{G1S} = 10 mA, V_{G2S} = 0 V, V_{DS} = 0 V	+$V_{(BR)G1SS}$	8	-	12	
Gate 2 source breakdown voltage ±I_{G2S} = 10 mA, V_{G1S} = 0 , V_{DS} = 0	±$V_{(BR)G2SS}$	8	-	13	
Gate 1 source current V_{G1S} = 6 V, V_{G2S} = 0 V	+I_{G1SS}	-	100	-	µA
Gate 2 source leakage current ±V_{G2S} = 8 V, V_{G1S} = 0 , V_{DS} = 0	±I_{G2SS}	-	-	50	nA
Drain current V_{DS} = 5 V, V_{G1S} = 0 , V_{G2S} = 4.5 V	I_{DSS}	-	-	800	µA
Operating current (selfbiased) V_{DS} = 5 V, V_{G2S} = 4.5 V	I_{DSO}	-	13	-	mA
Gate 2-source pinch-off voltage V_{DS} = 5 V, I_D = 200 µA	$V_{G2S(p)}$	-	1	-	V
AC Characteristics					
Forward transconductance (self biased) V_{DS} = 5 V, V_{G2S} = 4.5 V, f = 1 kHz	g_{fs}	-	30	-	mS
Gate 1-input capacitance (self biased) V_{DS} = 5 V, V_{G2S} = 4.5 V, f = 1 MHz	C_{g1ss}	-	2.4	2.7	pF
Output capacitance (self biased) V_{DS} = 5 V, V_{G2S} = 4.5 V, f = 100 MHz	C_{dss}	-	1.3	-	
Power gain (self biased) V_{DS} = 5 V, V_{G2S} = 4.5 V, f = 800 MHz	G_{ps}	-	19	-	dB
Noise figure (self biased) V_{DS} = 5 V, V_{G2S} = 4.5 V, f = 800 MHz	F_{800}	-	1.6	-	
Gain control range (self biased) V_{DS} = 5 V, V_{G2S} = 1 V, f = 800 MHz	ΔG_{ps}	40	50	-	

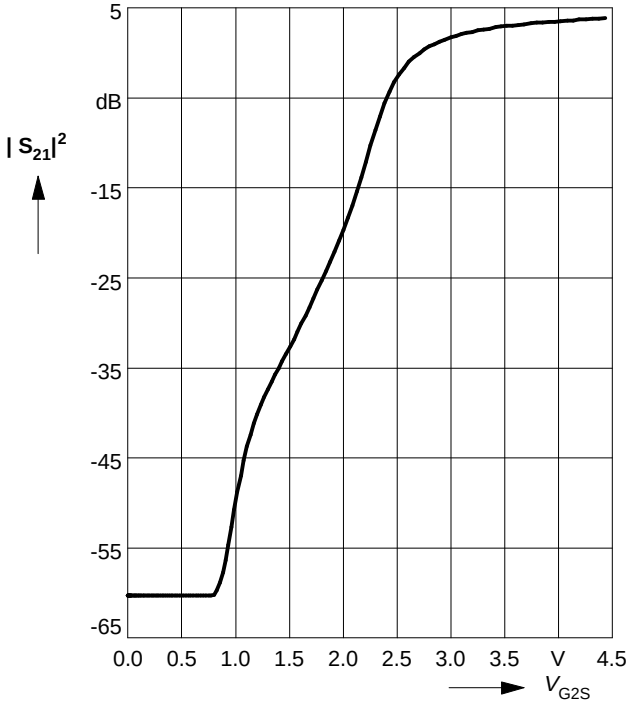
Total power dissipation $P_{tot} = f(T_S)$



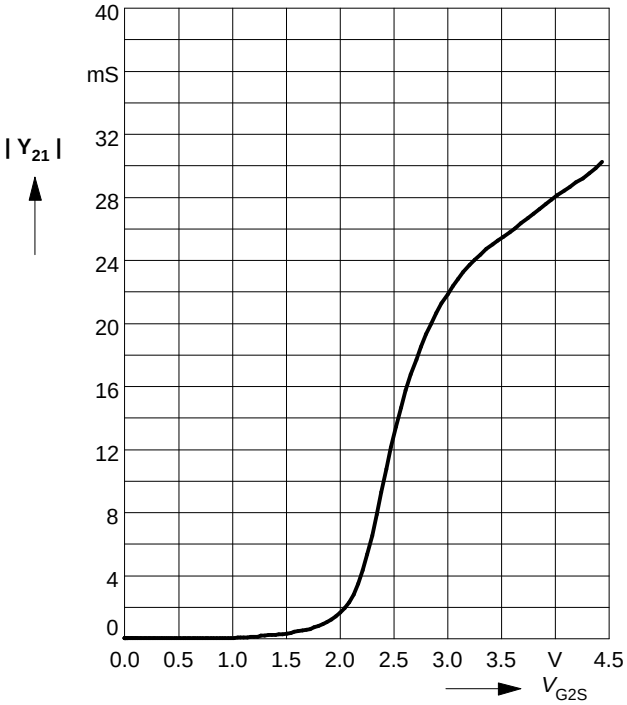
Drain current $I_D = f(V_{G2S})$



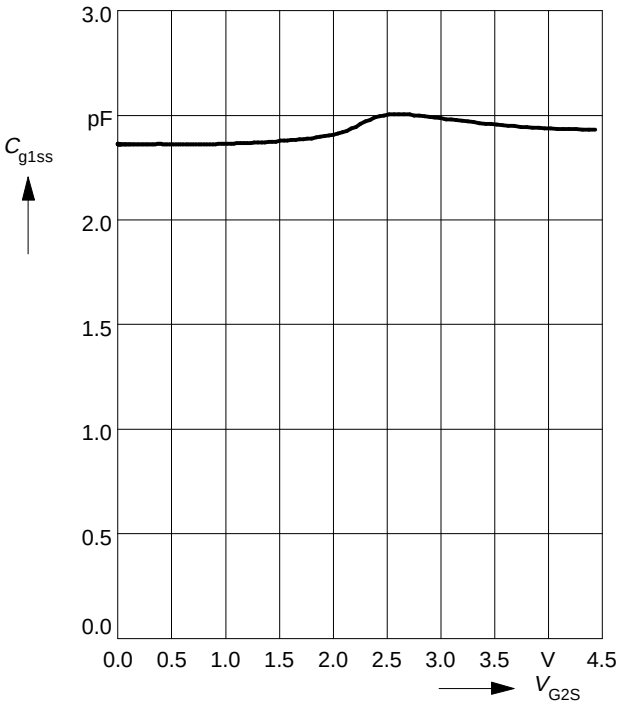
Insertion power gain
$|S_{21}|^2 = f(V_{G2S})$
f = 800MHz



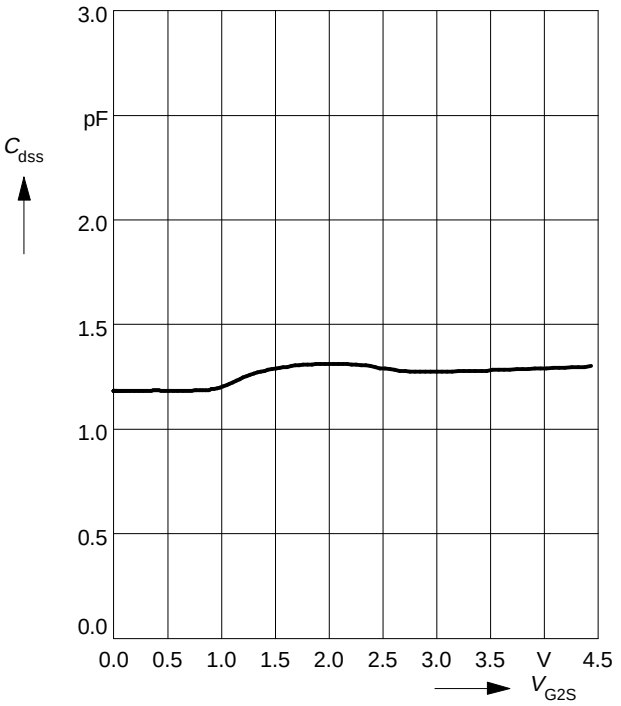
Forward transfer admittance
$|Y_{21}| = f(V_{G2S})$



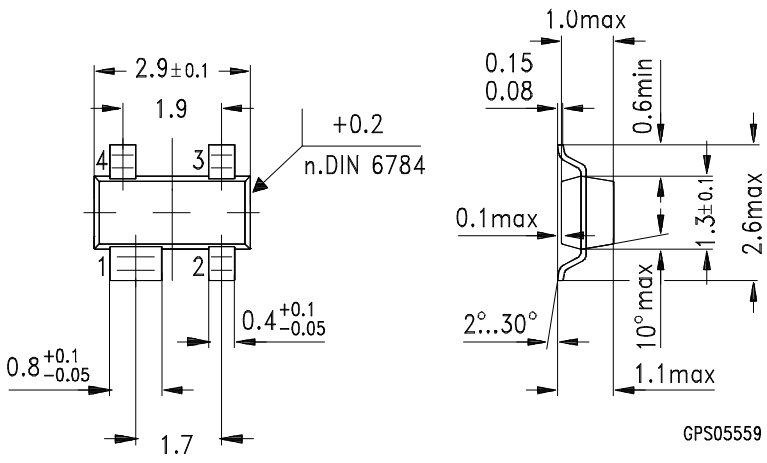
Gate 1 input capacitance $C_{g1ss} = f(V_{g2s})$
f=1MHz



Output capacitance $C_{dss} = f(V_{G2})$
f=1MHz



Package


2.9±0.1
1.9
+0.2
n.DIN 6784
4
3
1
2
0.4 +0.1 −0.05
0.8 +0.1 −0.05
1.7
1.0max
0.15
0.08
0.6min
0.1max
1.3±0.1
2.6max
2°...30°
10° max
1.1max
GPS05559