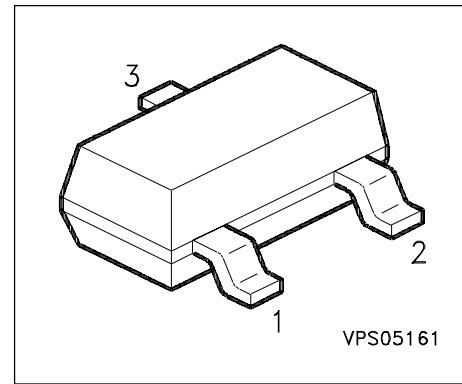
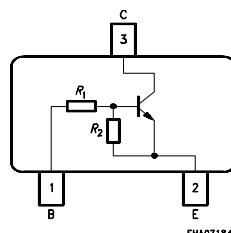


**NPN Silicon Digital Transistor**

- Switching circuit, inverter, interface circuit, driver circuit
- Built in bias resistor ( $R_1=4.7\text{k}\Omega$ ,  $R_2=47\text{k}\Omega$ )



Type	Marking	Ordering Code	Pin Configuration			Package
BCR 116	WG <sub>S</sub>	Q62702-C2337	1 = B	2 = E	3 = C	SOT-23

**Maximum Ratings**

Parameter	Symbol	Values	Unit
Collector-emitter voltage	$V_{CEO}$	50	V
Collector-base voltage	$V_{CBO}$	50	
Emitter-base voltage	$V_{EBO}$	5	
Input on Voltage	$V_{i(on)}$	15	
DC collector current	$I_C$	100	
Total power dissipation, $T_S = 102^\circ\text{C}$	$P_{tot}$	200	
Junction temperature	$T_j$	150	
Storage temperature	$T_{stg}$	- 65 ... + 150	$^\circ\text{C}$

**Thermal Resistance**

Junction ambient 1)	$R_{thJA}$	$\leq 350$	K/W
Junction - soldering point	$R_{thJS}$	$\leq 240$	

1) Package mounted on pcb 40mm x 40mm x 1.5mm / 6cm<sup>2</sup> Cu

**Electrical Characteristics** at  $T_A=25^\circ\text{C}$ , unless otherwise specified

<b>Parameter</b>	<b>Symbol</b>	<b>Values</b>			<b>Unit</b>
		<b>min.</b>	<b>typ.</b>	<b>max.</b>	

### DC Characteristics

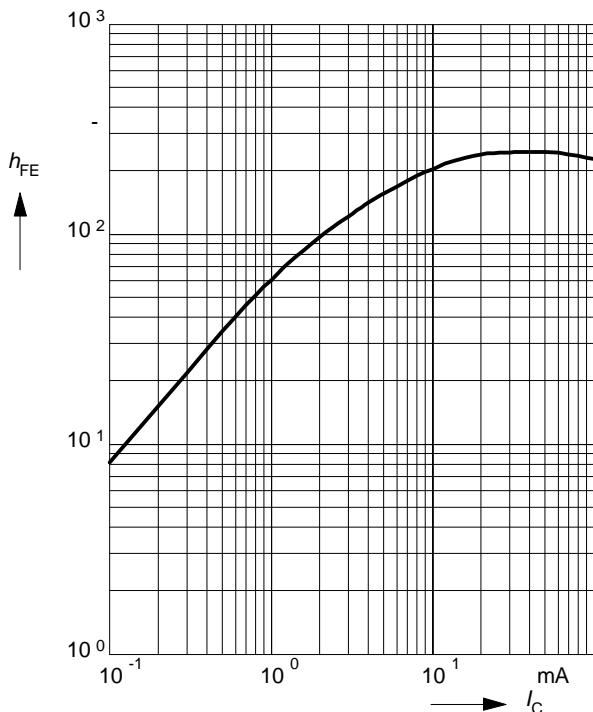
Collector-emitter breakdown voltage $I_C = 100 \mu\text{A}, I_B = 0$	$V_{(\text{BR})\text{CEO}}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10 \mu\text{A}, I_B = 0$	$V_{(\text{BR})\text{CBO}}$	50	-	-	
Collector cutoff current $V_{CB} = 40 \text{ V}, I_E = 0$	$I_{\text{CBO}}$	-	-	100	nA
Emitter cutoff current $V_{EB} = 5 \text{ V}, I_C = 0$	$I_{\text{EBO}}$	-	-	155	µA
DC current gain $I_C = 5 \text{ mA}, V_{CE} = 5 \text{ V}$	$h_{\text{FE}}$	70	-	-	-
Collector-emitter saturation voltage 1) $I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$	$V_{\text{CEsat}}$	-	-	0.3	V
Input off voltage $I_C = 100 \mu\text{A}, V_{CE} = 5 \text{ V}$	$V_{i(\text{off})}$	0.4	-	0.8	
Input on Voltage $I_C = 2 \text{ mA}, V_{CE} = 0.3 \text{ V}$	$V_{i(\text{on})}$	0.5	-	1.4	
Input resistor	$R_1$	3.2	4.7	6.2	kΩ
Resistor ratio	$R_1/R_2$	0.09	0.1	0.11	-

### AC Characteristics

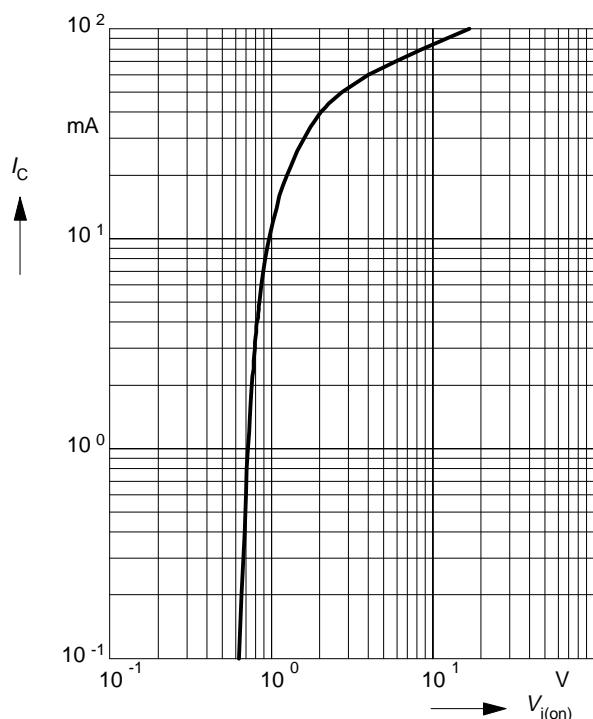
Transition frequency $I_C = 10 \text{ mA}, V_{CE} = 5 \text{ V}, f = 100 \text{ MHz}$	$f_T$	-	160	-	MHz
Collector-base capacitance $V_{CB} = 10 \text{ V}, f = 1 \text{ MHz}$	$C_{cb}$	-	3	-	pF

1) Pulse test:  $t < 300 \mu\text{s}; D < 2\%$

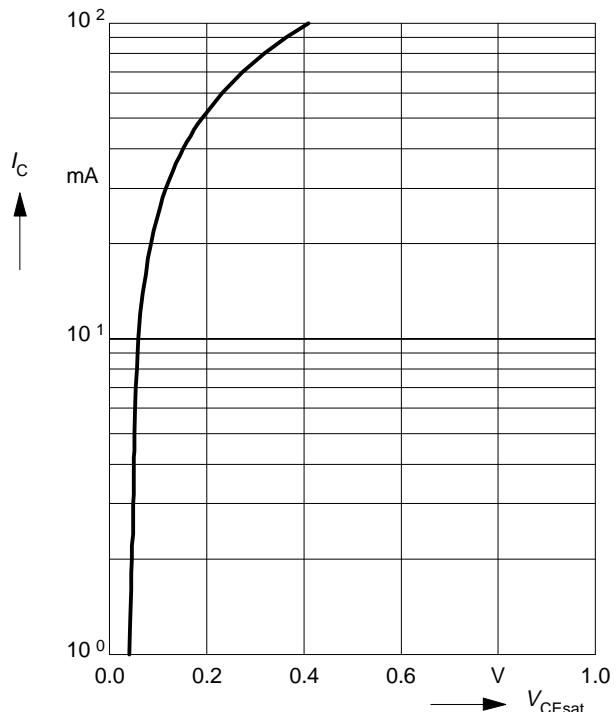
**DC Current Gain**  $h_{FE} = f(I_C)$   
 $V_{CE} = 5V$  (common emitter configuration)



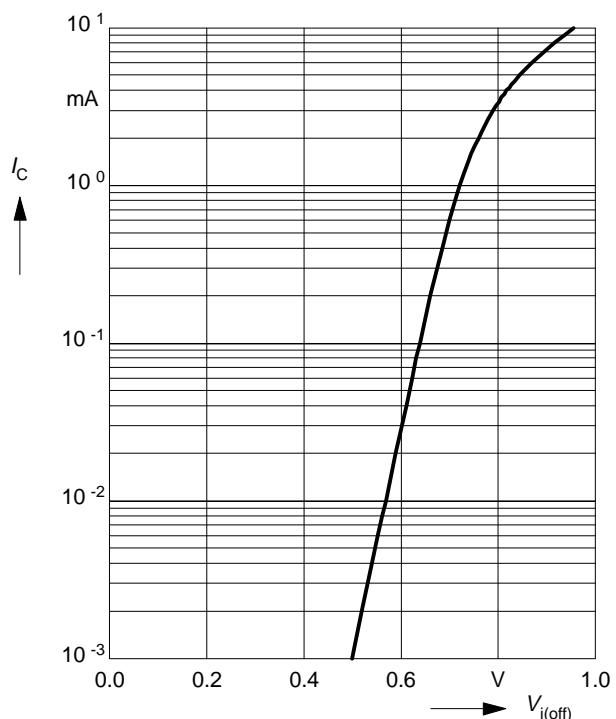
**Input on Voltage**  $V_{i(on)} = f(I_C)$   
 $V_{CE} = 0.3V$  (common emitter configuration)



**Collector-Emitter Saturation Voltage**  
 $V_{CEsat} = f(I_C)$ ,  $h_{FE} = 20$

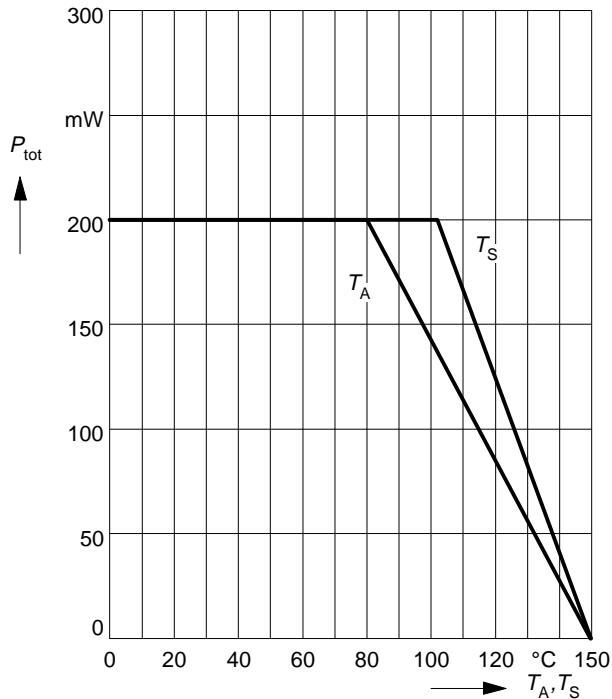


**Input off voltage**  $V_{i(off)} = f(I_C)$   
 $V_{CE} = 5V$  (common emitter configuration)

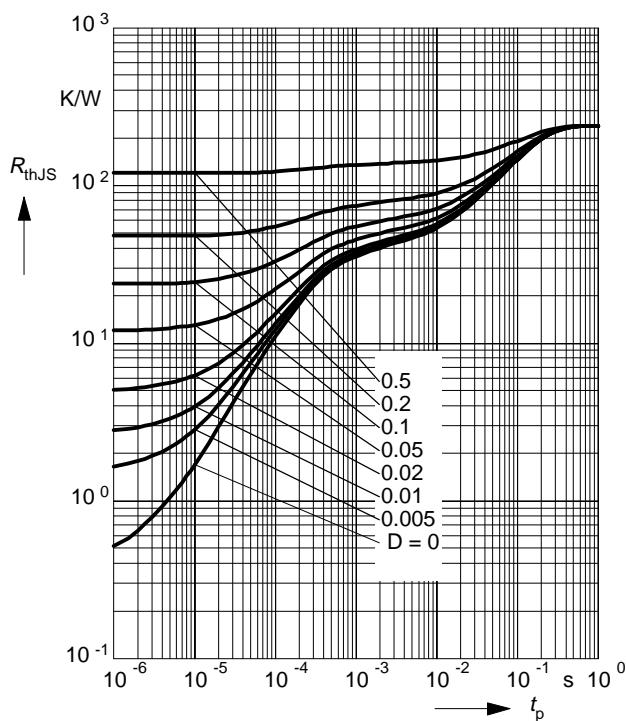


**Total power dissipation**  $P_{\text{tot}} = f(T_A^*; T_S)$

\* Package mounted on epoxy



**Permissible Pulse Load**  $R_{\text{thJS}} = f(t_p)$



**Permissible Pulse Load**  $P_{\text{totmax}} / P_{\text{totDC}} = f(t_p)$

