

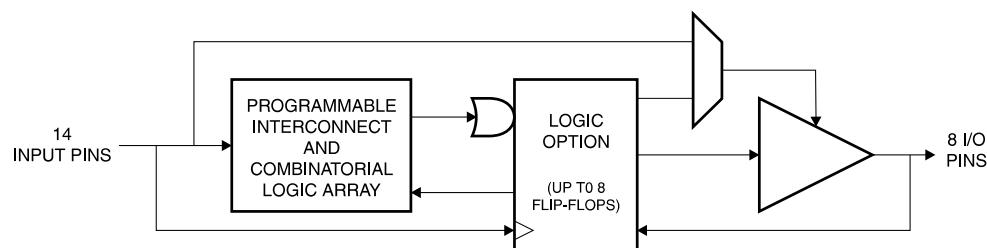
Features

- User-Controlled Power Down Pin
- High Speed Equivalent of ATF20V8B
- Pin-Controlled Zero Standby Power (10 μ A Typical) Option
- Industry Standard Architecture
 - Emulates Many 24-Pin PALs[®]
 - Low Cost Easy-to-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Devices
 - 5 ns Maximum Pin-to-Pin Delay
- CMOS and TTL Compatible Inputs and Outputs
 - Latch Feature Hold Outputs to Previous Logic States
- Advanced Flash Technology
 - Reprogrammable
 - 100% Tested
- High Reliability CMOS Process
 - 20 Year Data Retention
 - 100 Erase/Write Cycles
 - 2,000V ESD Protection
 - 200 mA Latchup Immunity
- Commercial, and Industrial Temperature Ranges
- Dual-in-Line and Surface Mount Packages in Standard Pinouts

**High
Performance
Flash PLD**

**Advance
Information**

Block Diagram



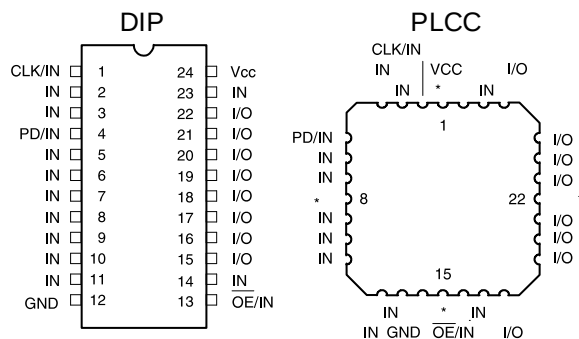
Description

The ATF20V8C is a high performance CMOS (Electrically Erasable) Programmable Logic Devices (PLDs) which utilize Atmel's proven electrically erasable Flash memory technology. Speeds down to 5 ns and power dissipation as low as 10 μ A are offered. All speed ranges are specified over the full 5V $\pm$ 10% range for industrial temperature ranges, and 5V $\pm$ 5% for commercial ranges.

(continued)

Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
*	No Internal Connection
VCC	+5V Supply
PD	Power Down



Top view

0408B

Description (Continued)

The ATF20V8C provides a high-speed CMOS PLD solution with maximum pin to pin delay of 5 ns. The ATF20V8C also has a user-controlled power down feature, offering “zero” standby power (10 μ A typical). The user-controlled power down feature allows the user to manage total system power to meet specific application requirements, enhance reliability all without sacrificing speed. Pin “keeper” circuits on input and output pin reduce static power consumed by pull-up resistors.

The ATF20V8C incorporates a superset of the generic architectures, which allows direct replacement of the 20R8 family and most 24-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allowing highly complex logic functions to be realized.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V _{CC} Power Supply	5V $\pm$ 5%	5V $\pm$ 10%

Functional Description

The ATF20V8C macrocell can be configured in one of three different modes. Each mode makes the ATF20V8C look like a different device. The ATF20V8C can be a registered output, combinatorial I/O, combinatorial output, or dedicated input. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus output with output enable control.

The ATF20V8C has a user controlled power down pin which, when active, allows the user to place the device into a “zero” standby power power down mode. The device can also operate at high speed. Maximum pin-to-pin delays of 5 ns are offered. Static power loss due to pull-up

resistors is eliminated by using input and output pin “keeper” circuits which holds pins to their previous logic levels when idle.

The universal architecture of the ATF20V8C can be programmed to emulate many 24-pin PAL devices. The user can download the subset device JEDEC programming file to the PLD programmer, and the ATF20V8C can be configured to act like the chosen device.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the contents the ATF20V8C. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.