Features

- Incorporates the ARM7TDMI™ ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - Embedded ICE (In-Circuit Emulation)
- 8K Bytes of On-chip SRAM
  - 32-bit Data Bus
  - Single-clock Cycle Access
- 128K Bytes of On-chip ROM
  - 32-bit Data Bus
  - Single-clock Cycle Access
- Fully Programmable External Bus Interface (EBI)
  - Maximum External Address Space of 64M Bytes
  - Up to 8 Chip Selects
  - Software Programmable 8/16-bit External Data Bus
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - 4 External Interrupts, Including a High-priority Low-latency Interrupt Request
- 32 Programmable I/O Lines
- 3-channel 16-bit Timer/Counter
  - 3 External Clock Inputs
  - 2 Multi-purpose I/O Pins per Channel
- 2 USARTs
  - 2 Dedicated Peripheral Data Controller (PDC) Channels per USART
- Programmable Watchdog Timer
- Advanced Power-saving Features
  - CPU and Peripherals Can be Deactivated Individually
- Fully Static Operation:
  - 0 Hz to 16 MHz at 1.8V
  - 0 Hz to 33 MHz at 2.7V
  - 0 Hz to 40 MHz at 3.0V
- 1.8V to 3.6V Operating Range
- Available in a 100-lead TQFP Package

Description

The AT91M40807 microcontroller is a member of the Atmel AT91 16/32-bit microcontroller family, which is based on the ARM7TDMI processor core. This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications.

The AT91M40807 microcontroller features a direct connection to off-chip memory, including Flash, through the fully programmable External Bus Interface (EBI). An eight-level priority vectored interrupt controller, in conjunction with the Peripheral Data Controller, significantly improves the real-time performance of the device.

The device is manufactured using Atmel's high-density CMOS technology. By combining the ARM7TDMI processor core with an on-chip high-speed SRAM and ROM memory and a wide range of peripheral functions on a monolithic chip, the AT91M40807 is a powerful microcontroller that offers a flexible, cost-effective solution to many compute-intensive embedded control applications.

AT91 ARM® Thumb® Microcontrollers

AT91M40807 Electrical Characteristics

Rev. 1391A–09/00

Absolute Maximum Ratings*

Operating Temperature (Industrial)	-40°C to +85°C
Voltage on Any Input Pin with Respect to Ground	-0.5V to +4.0V
Maximum Operating Voltage	4.6V
DC Output Current	6 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	DC Supply		1.8		3.6	V
T_A	Ambient Temperature		-40		85	°C
V_{IL}	Input Low Voltage	V_{DD} = 1.8V to 3.6V	-0.5		0.3 x V_{DD}	V
V_{IH}	Input High Voltage	V_{DD} = 1.8V to 3.6V	0.7 x V_{DD}		3.6	V
V_{OL}	Output Low Voltage	I_{OL} = 0.8 mA, V_{DD} = 3.0V			0.1	V
V_{OH}	Output High Voltage	I_{OH} = 0.8 mA, V_{DD} = 3.0V	V_{DD} - 0.1			V
I_{LEAK}	Input Leakage Current				390	nA
I_{PULL}	Input Pull-up Current	V_{DD} = 3.6V			350	µA
I_{CAP}	Input Capacitance				6	pF
I_{SC}	Static Current	V_{DD} = 3.6V - MCKI = 0 Hz All inputs driven TMS, TDI, TCK, NRST = 1		TBD		µA
		V_{DD} = 1.8V - MCKI = 0 Hz All inputs driven TMS, TDI, TCK, NRST = 1		TBD		

Power Consumption

The values in the following tables are measured values in the operating conditions indicated (i.e., V_{DD} = 3.3V or 2.0V, T = 25°) on the AT91EB40 Evaluation Board.

Table 1. Power Consumption

Mode	Conditions	V_{DD}		Unit
		2.0V	3.3V	
Reset		0.05	0.13	mW/MHz
Normal	Fetch in ARM mode out of Internal SRAM All peripheral clocks activated	1.52	4.13	
	Fetch in ARM mode out of Internal SRAM All peripheral clocks deactivated	1.12	3.06	
Idle	All peripheral clocks activated	0.69	1.88	
	All peripheral clocks deactivated	0.2	0.54	

Table 2. Power Consumption per Peripheral

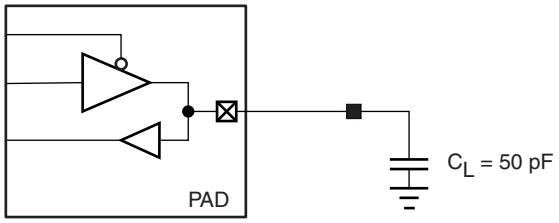
Peripheral	V_{DD}		Unit
	2.0V	3.3V	
PIO Controller	0.01	0.03	mW/MHz
Timer/Counter Channel	0.01	0.02	
Timer/Counter Block (3 Channels)	0.02	0.07	
USART	0.03	0.083	

Conditions

Environment Constraints

The output delays are valid for a capacitive load of 50 pF, as shown in Figure 1.

Figure 1. Output/Bidirectional Pad Capacitive Load



Timing Results

The output delays are for a capacitive load of 50 pF, as shown in Figure 1.

In order to obtain the timing for other capacitance values, the following equation should be used.

$$t = t_{datasheet} + factor \times (C_{load} - 50\text{pF})$$

Table 3. Derating Factor Due to Capacitive Load Variation

Parameter	Industrial	Units
Factor	0.04	ns/pF

Voltage Ranges

Timings are provided for the three operating conditions defined. The core voltage is supplied from 1.8V to 3.6V, but the three following operating conditions have been characterized for timing purposes.

Table 4. Voltage Ranges for Timing Characterization

Operating Conditions	V_{DD}		Maximum Operating Frequency
	Minimum	Maximum	
33 MHz at 2.7V	2.7V	3.6V	33 MHz
40 MHz at 3.0V	3.0V	3.6V	40 MHz
16 MHz at 1.8V	1.8V	3.6V	16 MHz

Clock Waveforms

Table 5. Clock Waveform Parameters

Symbol	Parameter	Minimum			Maximum			Units
		33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	
$1/(t_{CP})$	Oscillator Frequency				33	40	16	MHz
t_{CP}	Main Clock Period	33	25	62				ns
t_{CH}	High Time	12	11	22				
t_{CL}	Low Time	12	11	22				
t_r	Rising Edge				2	2	2	
t_f	Falling Edge				2	2	2	

Table 6. Clock Propagation Times

Symbol	Parameter	Minimum			Maximum			Units
		33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	
t_{CDLH}	Rising Edge Propagation Time	4	4	8	10	9	18	ns
t_{CDHL}	Falling Edge Propagation Time	5	5	10	12	11	22	

Figure 2. Clock Waveform

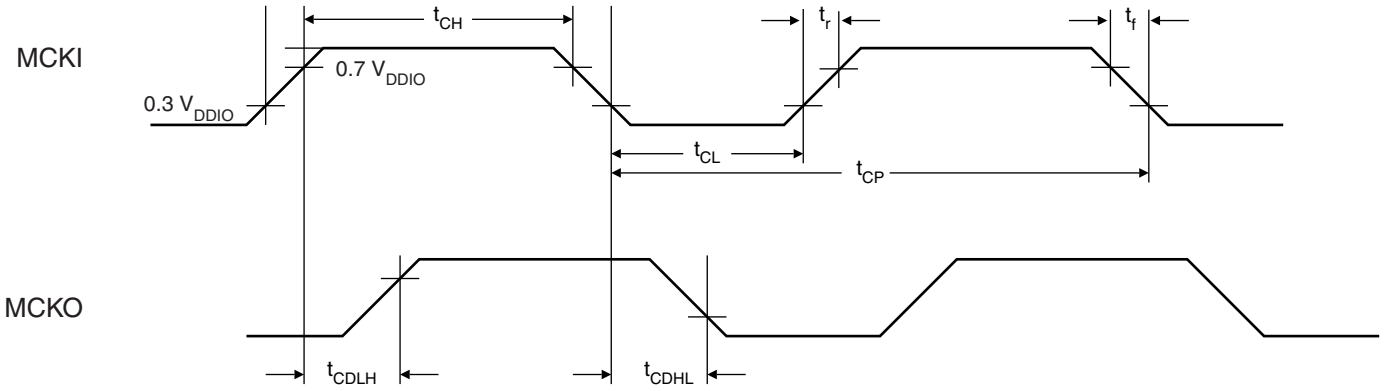
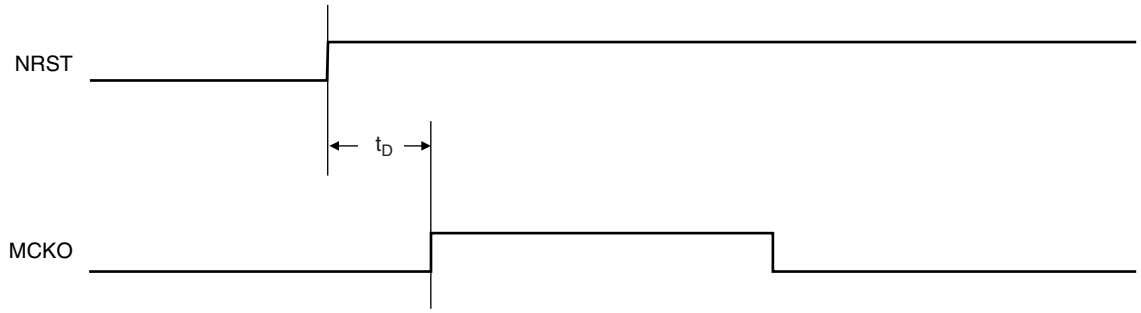


Table 7. NRST to MCKO

Symbol	Parameter	Minimum			Maximum			Units
		33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	
t_D	NRST Rising Edge to MCKO Valid Time	$3(t_{CP}/2)$	$3(t_{CP}/2)$	$3(t_{CP}/2)$	$7(t_{CP}/2)$	$7(t_{CP}/2)$	$7(t_{CP}/2)$	ns

Figure 3. MCKO Relative to NRST



AC Characteristics

EBI Signals Relative to MCKI

The following tables show timings relative to operating condition limits defined in Table 4. See Figure 4.

Table 8. General-purpose EBI Signals

Symbol	Parameter	Minimum			Maximum			Units
		33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	
EBI_1	MCKI Falling to NUB Valid	4	4	8	14	12	24	ns
EBI_2	MCKI Falling to NLB/A0 Valid	3	3	6	10	8	16	
EBI_3	MCKI Falling to A7 - A1 Valid	3	3	6	10	8	16	
EBI_4	MCKI Falling to A23 - A8 Valid	3	3	6	10	8	16	
EBI_5	MCKI Falling to Chip Select	5	5	10	17	15	30	
EBI_6	NWAIT Setup before MCKI Rising				10	8	16	
EBI_7	NWAIT Hold after MCKI Rising	2	1	2				

Table 9. EBI Write Signals

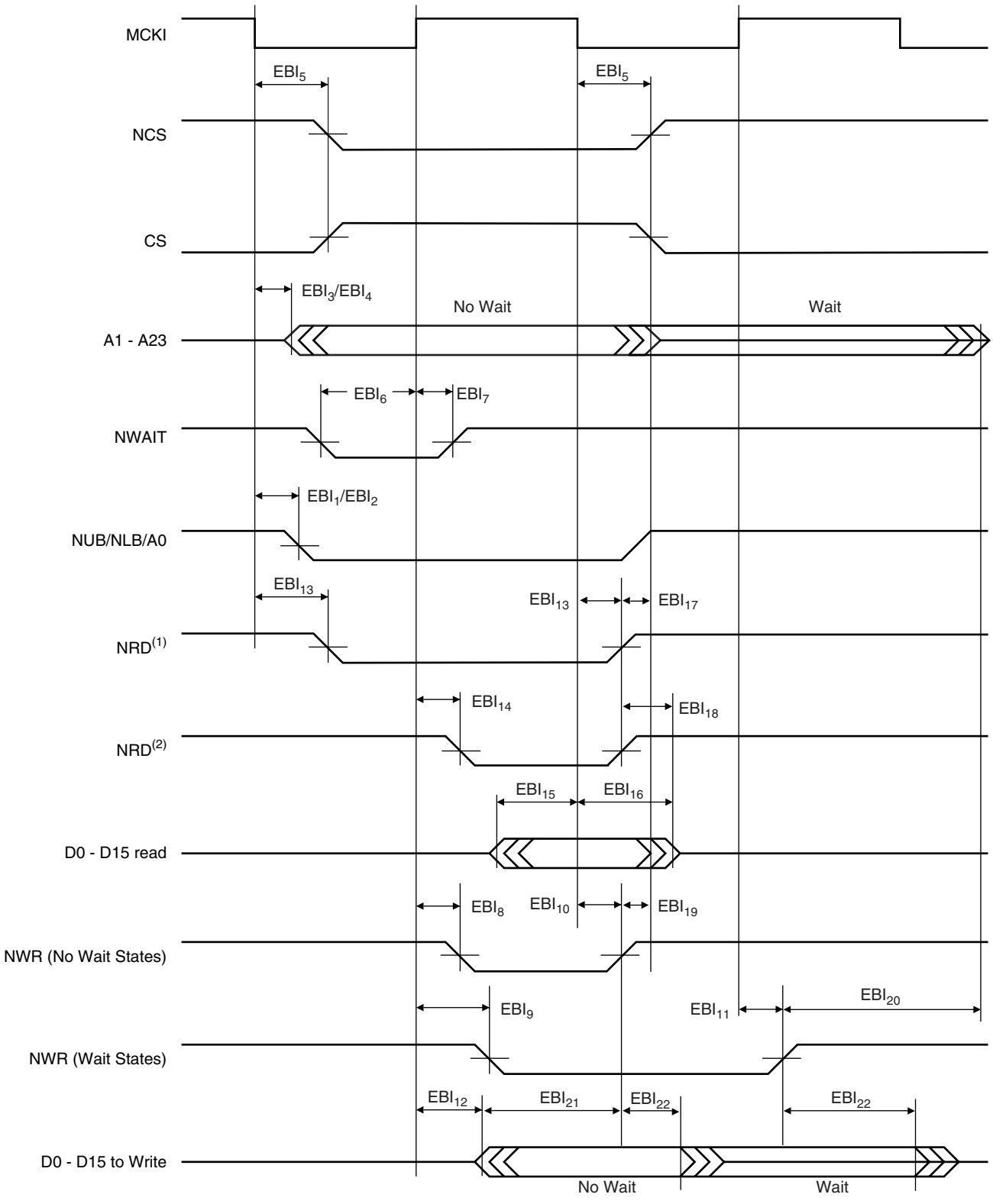
Symbol	Parameter	Minimum			Maximum			Units
		33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	
EBI_8	MCKI Rising to NWR Active (No Wait States)	5	5	10	13	11	22	ns
EBI_9	MCKI Rising to NWR Active (Wait States)	5	5	10	13	11	22	
EBI_{10}	MCKI Falling to NWR Inactive (No Wait States)	5	5	10	14	12	24	
EBI_{11}	MCKI Rising to NWR Inactive (Wait States)	5	5	10	14	12	24	
EBI_{12}	MCKI Rising to D0 - D15 Out Valid	5	5	10	17	15	30	
EBI_{19}	NWR High to A23 - A1, NUB/NLB/A0, NCS, CS Changes (No Wait States)	3	2	4				
EBI_{20}	NWR High to A23 - A1, NCS, CS Changes (Wait States)	$t_{CP/2}$	$t_{CP/2}$	$t_{CP/2}$				
EBI_{21}	Data Out Valid before NWR High	11	10	20				
EBI_{22}	Data Out Valid after NWR High	3	3	6				

Table 10. EBI Read Signals

Symbol	Parameter	Minimum			Maximum			Units
		33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	
EBI_{13}	MCKI Falling to NRD Valid(1)	5	5	10	15	13	26	ns
EBI_{14}	MCKI Rising to NRD Valid(2)	4	4	8	12	10	20	
EBI_{15}	D0 - D15 in Setup before MCKI Falling				4	4	8	
EBI_{16}	D0 - D15 in Hold after MCKI Falling	3	3	6				
EBI_{17}	NRD High to A23 - A1, NCS, CS Changes	0	0	0				
EBI_{18}	Data Hold after NRD High	0	0	0				

Notes: 1. Early Read Protocol
2. Standard Read Protocol

Figure 4. EBI Signals Relative to MCKI



Notes: 1. Early Read Protocol
2. Standard Read Protocol

Peripheral Signals Relative to MCKI

USART Signals

The inputs have to meet the minimum pulse width and period constraints as shown in Table 11 and Table 12, and represented in Figure 5.

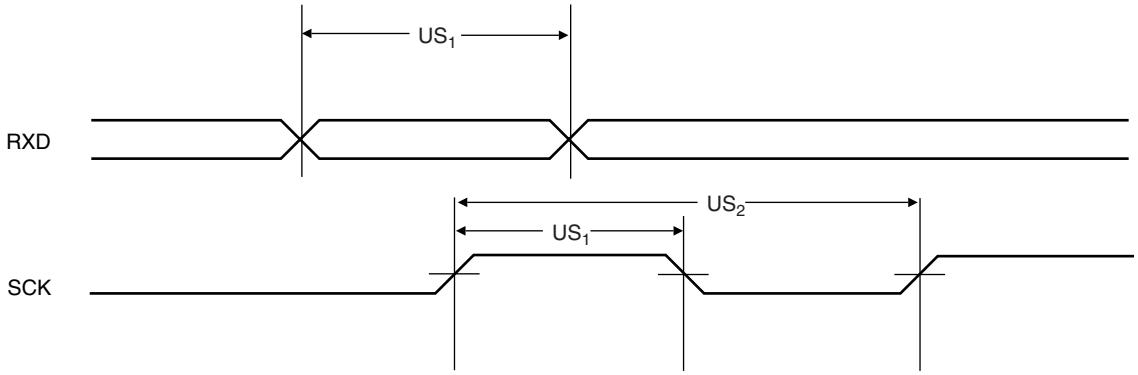
Table 11. USART Input Minimum Pulse Width

Symbol	Parameter	Minimum Pulse Width	Units
US_1	SCK/RXD Minimum Pulse Width	$3(t_{CP}/2)$	ns

Table 12. USART Minimum Input Period

Symbol	Parameter	Minimum Input Period	Units
US_2	SCK Minimum Input Period	$5(t_{CP}/2)$	ns

Figure 5. USART Signals



Timer/Counter Signals

Due to internal synchronization of input signals, there is a delay between an input event and a corresponding output event. This delay is $3(t_{CP})$ in Waveform Event Detection mode and $4(t_{CP})$ in Waveform Total Count Detection mode. The inputs have to meet the minimum pulse width and minimum input period shown in Tables 13 and 14, and as represented in Figure 6.

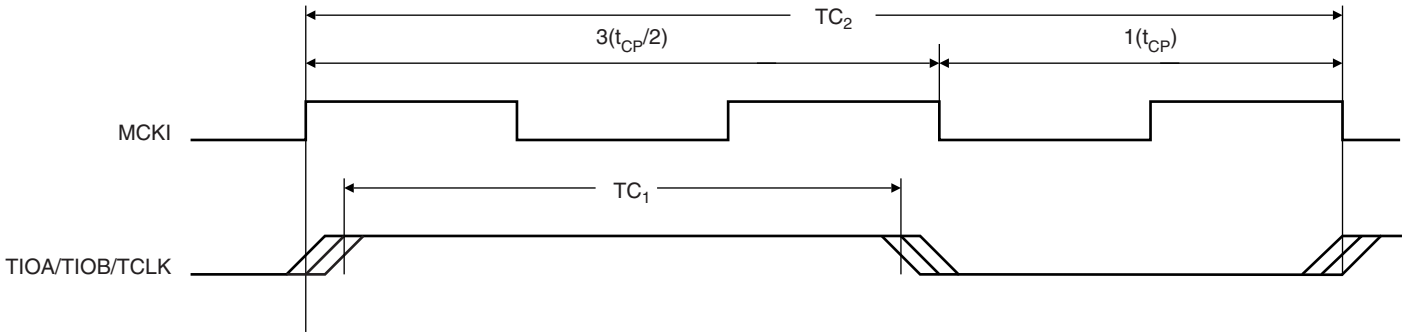
Table 13. Timer Input Minimum Pulse Width

Symbol	Parameter	Minimum Pulse Width	Units
TC_1	TCLK/TIOA/TIOB Minimum Pulse Width	$3(t_{CP}/2)$	ns

Table 14. Timer Input Minimum Input Period

Symbol	Parameter	Minimum Input Period	Units
TC_2	TCLK/TIOA/TIOB Minimum Input Period	$5(t_{CP}/2)$	ns

Figure 6. Timer Input

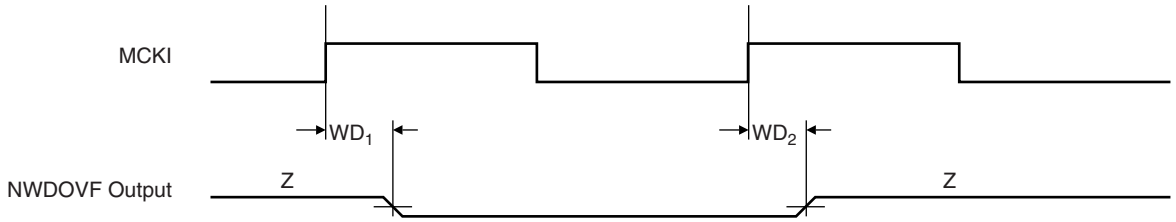


Watchdog Timer Signals

Table 15. Watchdog Timer Outputs

Symbol	Parameter	Minimum			Maximum			Units
		33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	
WD_1	MCKI Rising to NWDOVF Rising	2	2	4	10	8	16	ns
WD_2	MCKI Rising to NWDOVF Falling	2	2	4	10	8	16	

Figure 7. Watchdog Signals Relative to MCKI



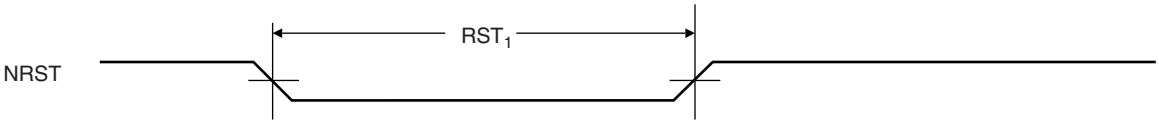
Reset Signals

A minimum pulse width is necessary, as shown in Table 16 and as represented in Figure 8.

Table 16. Reset Minimum Pulse Width

Symbol	Parameter	Minimum Pulse Width	Units
RST_1	NRST Minimum Pulse Width	$10(t_{CP})$	ns

Figure 8. Reset Signal



Only the NRST rising edge is synchronized with MCKI. The falling edge is asynchronous.

Advanced Interrupt Controller Signals

Inputs have to meet the minimum pulse width and minimum input period shown in Tables 17 and 18 and represented in Figure 9.

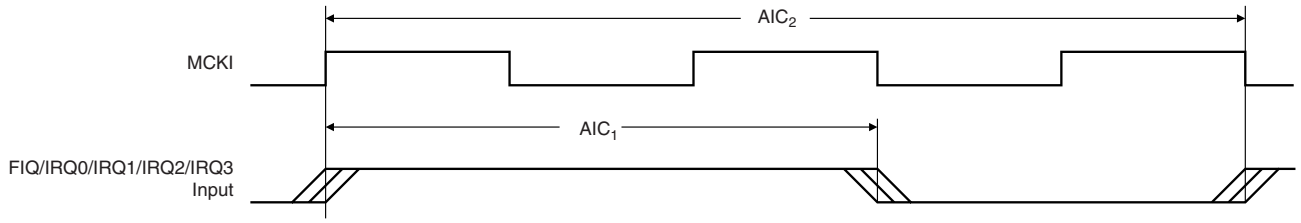
Table 17. AIC Input Minimum Pulse Width

Symbol	Parameter	Minimum Pulse Width	Units
AIC_1	FIQ/IRQ0/IRQ1/IRQ2/IRQ3 Minimum Pulse Width	$3(t_{CP}/2)$	ns

Table 18. AIC Input Minimum Input Period

Symbol	Parameter	Minimum Input Period	Units
AIC_2	AIC Minimum Input Period	$5(t_{CP}/2)$	ns

Figure 9. AIC Signals



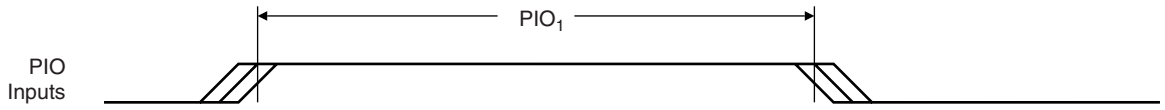
Parallel I/O Signals

The inputs have to meet the minimum pulse width shown in Table 19 and represented in Figure 10.

Table 19. PIO Input Minimum Pulse Width

Symbol	Parameter	Minimum Pulse Width	Units
PIO_1	PIO Input Minimum Pulse Width	$3(t_{CP}/2)$	ns

Figure 10. PIO Signal

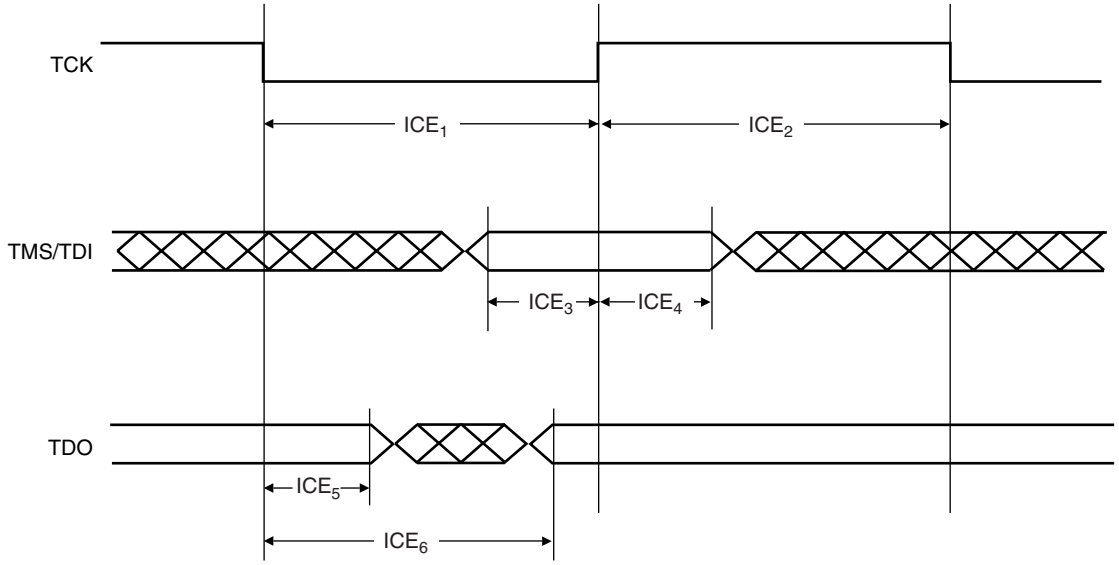


ICE Interface Signals

Table 20. ICE Interface Timing Specifications

Symbol	Parameter	Minimum			Maximum			Units
		33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	33 MHz at 2.7V	40 MHz at 3.0V	16 MHz at 1.8V	
ICE_1	TCK Low Period	50	50	50				ns
ICE_2	TCK High Period	50	50	50				
ICE_3	TDI, TMS Setup to TCK				0	-1	2	
ICE_4	TDI, TMS Hold from TCK	3	2	4				
ICE_5	TDO Hold Time	3	3	6				
ICE_6	TCK to TDO Valid	3	3	6	15	13	26	

Figure 11. ICE Interface Signal



Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

Printed on recycled paper.

1391A–09/00/0M