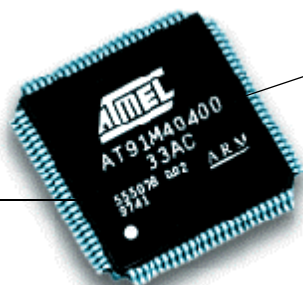


Errata Sheet V3.2

This errata sheet refers to devices with the following marking:

Internal product
reference 55568A



AT91M40400
25AC, 25AI or 33AC

- I/O Pads are not 5V Tolerant
- One Half-cycle NUB on First Access to a Chip Select Bank
- EBI Abort Generation

Summary of Previous Errata Sheets

Errata Sheet V2.1

- Power Saving not Functional

Errata Sheet V1.3

- The Timer Trigger on Compare RC add one Cycle
- The Internal Reset does not Work

Errata Sheet V1.2

- The Maximum Operating Frequency is 25 MHz, not 33 MHz

Errata Sheet V1.1

- Incorrect Timer TC_BMR Read Access
- EBI: Incorrect THUMB Fetches on External 16-bit Memory

Errata Sheet V1.0

- EBI Address Bus During Internal Access
- PDC Transfer not Possible While Core Clock is Deactivated
- PIO Cannot Select Each Filter Separately
- USART TX Break Management Does not Ensure Minimum Break Character Time
- AIC Does not Return the Interrupt Vector When the Interrupt is Disabled or Disappears
- Timer Overflow/Compare may be set at Counter Restart
- Clock Selection for Channels 0 and 1 of the Timer



AT91 ARM® Thumb® Microcontrollers

AT91M40400 Errata Sheet V3.2

Rev. 1362A-04/00



Errata Sheet V3.2

17. I/O Pads are not 5V Tolerant

The maximum acceptable voltage on each pad is 4.0V maximum.

16. One Half-cycle NUB on First Access to a Chip Select Bank

The NWR1/NUB signal is activated only after one half-cycle during each first access to a chip select bank. Following accesses are performed with the correct waveform, i.e. NUB is active at the start of the access.

15. EBI Abort Generation

When the core performs an access to an undefined address in the address space reserved for the EBI, the device does not guarantee that the Abort mode is entered.

Summary of Previous Errata Sheets

Errata Sheet 2.1

14. Power Saving not Functional

This problem has been fixed

Errata Sheet 1.3

13. The Timer Trigger on Compare RC add one Cycle

This problem has been fixed

12. The Internal Reset Does not Work

This problem has been fixed

Errata Sheet 1.2

11. The Maximum Operating Frequency is 25 MHz, not 33 MHz

Parts are marked according to maximum frequency

Errata Sheet 1.1

10. Incorrect Timer TC_BMR Read Access

This problem has been fixed

9. EBI: Incorrect THUMB Fetches on External 16-bit Memory

This problem has been fixed

8. Warning: Maximum Value Limit for Input Pull-down Resistor

There is a 5K Ohm maximum limit to the size of a pull-down resistor that can be used on any input.

Errata Sheet 1.0

7. EBI Address Bus During Internal Access

This problem has been fixed

6. PDC Transfer not Possible While Core Clock is Deactivated

This problem has been fixed

5. PIO Cannot Select Each Filter Separately

This problem has been fixed

4. USART TX Break Management Does not Ensure Minimum Break Character Time

This problem has been fixed

3. AIC Does not Return the Interrupt Vector When the Interrupt is Disabled or Disappears

This problem has been fixed

2. Timer Overflow/Compare may be set at Counter Restart

This problem has been fixed

1. Clock Selection for Channels 0 and 1 of the Timer

This problem has been fixed



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