## Features

- **Incorporates the ARM7TDMI™ ARM Thumb Processor**
  - **High-performance 32-bit RISC Architecture**
  - **High-density 16-bit Instruction Set**
  - **Leader in MIPS/Watt**
  - **Embedded ICE In Circuit Emulation**
- **4K Bytes Internal RAM**
- **Fully Programmable External Bus Interface (EBI)**
  - **Maximum External Address Space of 64M Bytes**
  - **Up to Eight Chip Selects**
  - **Software Programmable 8/16-bit External Databus**
- **Eight-level Priority, Individually Maskable, Vectored Interrupt Controller**
  - **Four External Interrupts, Including a High-priority Low-latency Interrupt Request**
- **32 Programmable I/O Lines**
- **Three-channel 16-bit Timer/Counter**
  - **Three External Clock Inputs**
  - **Two Multi-purpose I/O Pins per Channel**
- **Two USARTs**
  - **Two Dedicated Peripheral Data Controller (PDC) Channels per USART**
- **Programmable Watchdog Timer**
- **Low-power Idle and Power-down Modes**
- **Fully Static Operation: 0 Hz to 33 MHz**
- **2.7V to 3.6V Operating Range**
- **Available in a 100-lead TQFP Package**

## Description

The AT91M40400 is a member of the Atmel AT91 16/32-bit Microcontroller family which is based on the ARM7TDMI embedded processor. This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally-banked registers result in very fast exception handling, making the device ideal for real-time control applications. The AT91 ARM-based MCU family also features Atmel's high-density, nonvolatile memory technology. The on-chip Flash program memory is in-system programmable.

The AT91M40400 has a direct connection to off-chip memory, including Flash, through the External Bus Interface (EBI).

The device is manufactured using Atmel's high-density CMOS technology. By combining the ARM7TDMI microcontroller core with an on-chip RAM and a wide range of peripheral functions on a monolithic chip, the Atmel AT91M40400 is a powerful microcontroller that provides a flexible, cost-effective solution to many compute-intensive embedded control applications.

# 16/32-Bit Microcontroller

# AT91M40400 Electrical and Mechanical Characteristics

Rev. 1078A–10/98

## Pin Configuration

**Figure 1.** AT91M40400 Pinout (Top View)

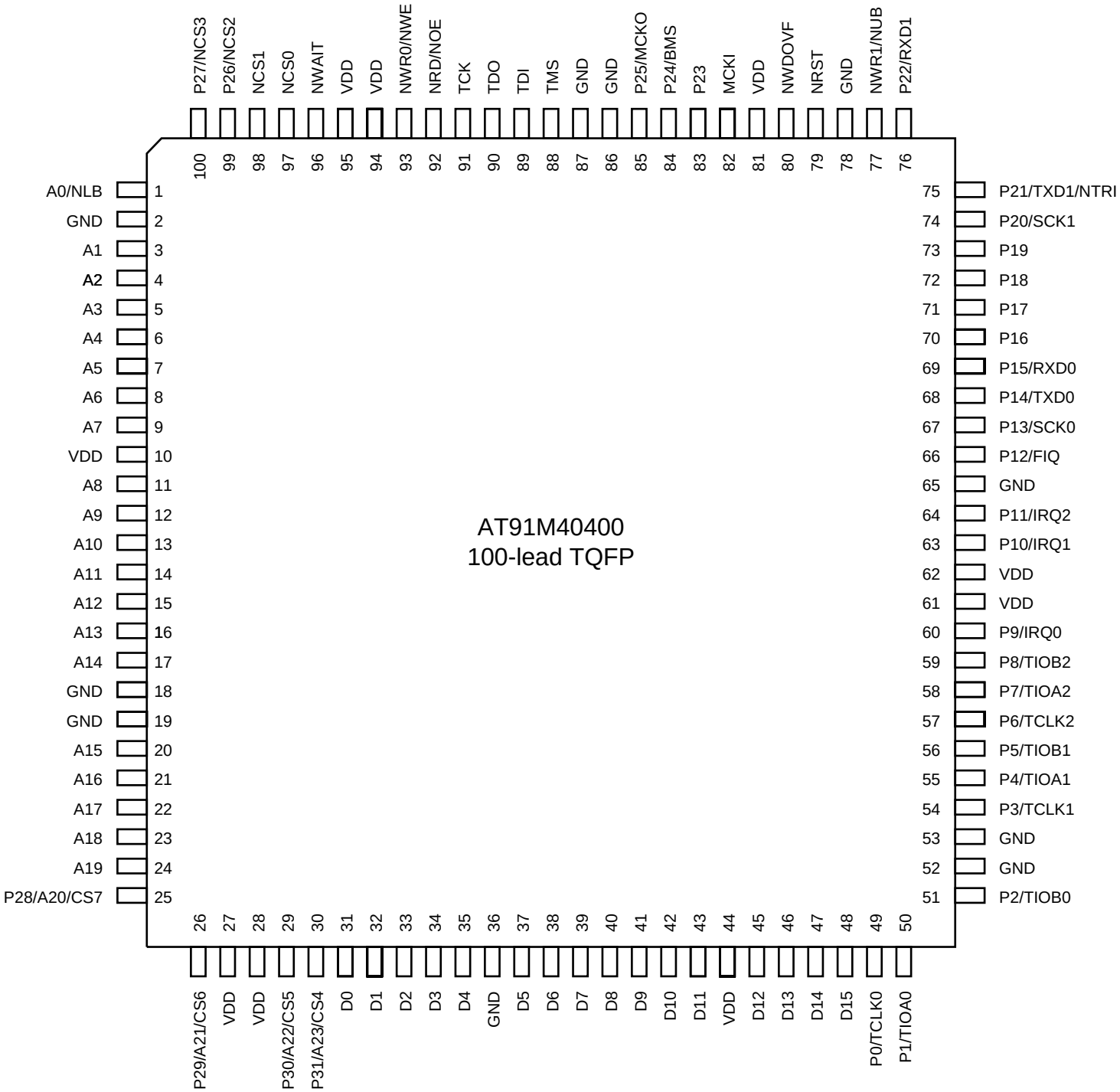


**Table 1.** AT91M40400 Pin Description

| Module | Name | Function | Type | Active Level | Comments |
|---|---|---|---|---|---|
| EBI | A0-A23 | Address Bus | Output | -- | All valid after reset |
| | D0-D15 | Data Bus | I/O | -- | |
| | NCS0-NCS3 | Chip Select | Output | low | |
| | CS4-CS7 | Chip Select | Output | high | A23-A20 after reset |
| | NWR0 | Lower Byte 0 Write Signal | Output | low | Used in Byte Write Option |
| | NWR1 | Upper Byte 1 Write Signal | Output | low | Used in Byte Write Option |
| | NRD | Read Signal | Output | low | Used in Byte Write Option |
| | NWE | Write Enable | Output | low | Used in Byte Select Option |
| | NOE | Output Enable | Output | low | Used in Byte Select Option |
| | NUB | Upper Byte Select | Output | low | Used in Byte Select Option |
| | NLB | Lower Byte Select | Output | low | Used in Byte Select Option |
| | NWAIT | Wait Input | Input | low | |
| | BMS | Boot Mode Select | Input | -- | Sampled during reset |
| AIC | FIQ | Fast Interrupt Request | Input | -- | PIO controlled after reset |
| | IRQ0-IRQ2 | External Interrupt Request | Input | -- | PIO controlled after reset |
| Timer | TCLK0-TCLK2 | Timer External Clock | Input | -- | PIO controlled after reset |
| | TIOA0-TIOA2 | Multipurpose Timer I/O pin A | I/O | -- | PIO controlled after reset |
| | TIOB0-TIOB2 | Multipurpose Timer I/O pin B | I/O | -- | PIO controlled after reset |
| USART | SCK0-SCK1 | External Serial Clock | I/O | -- | PIO controlled after reset |
| | TXD0-TXD1 | Transmit Data Output | Output | -- | PIO controlled after reset |
| | RXD0-RXD1 | Receive Data Input | Input | -- | PIO controlled after reset |
| PIO | P0-P31 | Parallel IO line | I/O | -- | |
| WD | NWDOVF | Watchdog overflow | Output | low | Open drain |
| Clock | MCKI | Master Clock Input | Input | -- | Schmidt trigger |
| | MCKO | Master Clock Output | Output | -- | |
| Reset | NRST | Hardware Reset Input | Input | low | Schmidt trigger, internal pull-up |
| | NTRI | Tristate Mode Select | Input | low | Sampled during reset |
| ICE | TMS | Test Mode Select | Input | -- | Schmidt trigger, internal pull-up |
| | TDI | Test Data Input | Input | -- | Schmidt trigger, internal pull-up |
| | TDO | Test Data Output | Output | -- | |
| | TCK | Test Clock | Input | -- | Schmidt trigger, internal pull-up |
| Power | VDD | Power | | | |
| | GND | Ground | | | |

## Absolute Maximum Ratings*

| |
|---|
| Operating Temperature (Commercial) .....0 to +70°C |
| Operating Temperature (Industrial).....-40°C to +85°C |
| Voltage on any input Pin with respect to Ground .....-0.5V to +5.5V |
| Maximum Operating Voltage .....4.6V |
| DC Output Current .....2 mA |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

$T_A$ = -40°C to 85°C, $V_{CC}$ = 2.7V to 3.6V unless otherwise specified. All pads are 5V tolerant.

**Table 2.** DC Characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | $V_{CC}$ = 2.7V to 3.6V | -0.5 | | 0.3 x Vcc | V |
| $V_{IH}$ | Input High Voltage | $V_{CC}$ = 2.7V to 3.6V | 0.7 x $V_{CC}$ | | $V_{CC}$ + 0.5 | V |
| $V_{IH}$ | Input High Voltage | $V_{CC}$ = 2.7V to 3.6V | 0.7 x $V_{CC}$ | | 5.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 0.8 mA, $V_{CC}$ = 3.0V | | | $V_{SS}$ + 0.1 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = 0.8 mA, $V_{CC}$ = 3.0V | $V_{CC}$ - 0.1 | | | V |
| $I_{CC}$ | Power Supply Current | Active Mode, 33 MHz | | 41 | 77 | mA |
| | | Active Mode, 25 MHz | | 32 | 60 | mA |
| | | Active Mode, 16 MHz | | 21 | 40 | mA |
| | | Active Mode, 8 MHz | | 11 | 22 | mA |
| | | Active Mode, 4 MHz | | 6 | 12 | mA |
| | | Idle Mode after reset, 3.6V | | 30 | | µA |
| $I_{OH}$ | Output Source Current | $V_{CC}$ = 3.0V, $V_{OH}$ = 2.4V | | | 2 | mA |
| $I_{OL}$ | Output Sink Current | $V_{CC}$ = 3.0V, $V_{OL}$ = 0.4 | | | 2 | mA |
| $I_{LEAK}$ | Input Leakage Current | | | | 100 | nA |
| $I_{PULL}$ | Input Pull-up Current | $V_{CC}$ = 3.3V, $V_{IN}$ = 0 | -400 | | -80 | µA |
| $I_{CAP}$ | Input Capacitance for all Pins | | | | 12 | pF |

# Conditions

## Environment Constraints

The output delays are valid for a capacitive load of 50pF as shown in the diagram below.

**Figure 2.** Output/Bidir Pad Capacitive Load

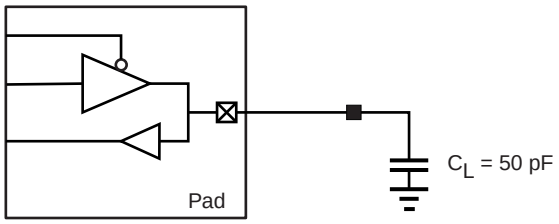



**Table 3.** Environment Constraints

| Parameter | Best Case | Nominal Case | Worst Case | |
|---|---|---|---|---|
| | | | Commercial | Industrial |
| Ambient Temperature | -40°C | 25°C | 70°C | 85°C |
| Supply Voltage, Vdd | 3.6V | 3.3V | 2.7V | 2.7V |

## Timing Results

The output delays are for a capacitive load of 50pF as shown in Figure 2 above.

In order to obtain the timing for other capacitance values, the following equation should be used.

$$t = t_{datasheet} + factor \times (C_{load} - 50pF)$$

**Table 4.** Derating Factor Due to Capacitive Load Variation

| Parameter | Best Case | Nominal Case | Worst Case | | Units |
|---|---|---|---|---|---|
| | | | Commercial | Industrial | |
| Factor | 0.0019 | 0.034 | 0.052 | 0.058 | ns/pF |

## AC Characteristics

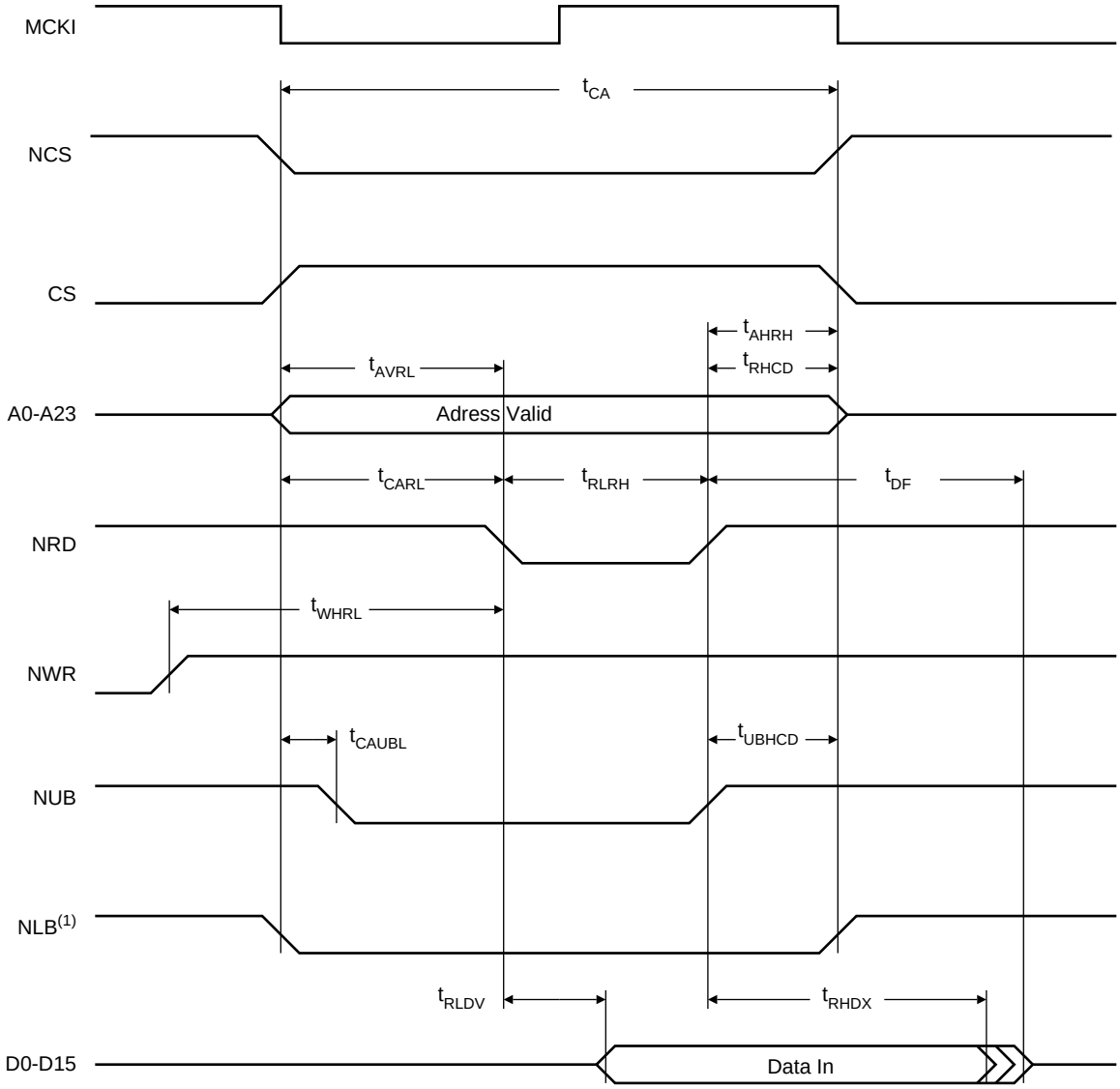
The following table shows the Minimum and Maximum timings for external memory read/write (valid for all conditions of operation). See Figures 3 and 4.

**Table 5.** External Memory Read/Write Timings

| Symbol | Parameter | Minimum | Maximum | | | Units |
|---|---|---|---|---|---|---|
| | | | AT91M40400 -25AC | AT91M40400 -25AI | AT91M40400 -33AC | |
| $t_{AHRH}$ | Address Hold After NRD High | 0 | | | | ns |
| $t_{AHWH}$ | Address Hold After NWR High | 2 | | | | ns |
| $t_{AVRL}$ | Address Valid to NRD Low | 0 | | | | ns |
| $t_{AVWL}$ | Address Valid to NWR Low | $t_{CL}$ - 6 | | | | ns |
| $t_{CA}$ | Chip Select Active Pulse Width | $t_{CP}$ - 2 | | | | ns |
| $t_{CARL}$ | Chip Select Active to NRD Low | 0 | | | | ns |
| $t_{CAUBL}$ | Chip Select Active to NUB Low | 0 | | | | ns |
| $t_{DF}$ | Data Float After NRD High | | $7(t_{CP})$ | | | ns |
| $t_{DVWH}$ | Data Out Valid Before NWR High | $t_{CH}$ - 5 | | | | ns |
| $t_{RHCD}$ | NRD High to Chip Select Disabled | 0 | | | | ns |
| $t_{RHDX}$ | Data Hold After NRD High | 0.6 | | | | ns |
| $t_{RLDV}$ | NRD Low to Valid Data (0 Wait States) | | $t_{CP}$ - 21 (1) | $t_{CP}$ - 21 (1) | $t_{CP}$ - 14.7 (1) | ns |
| | | | $t_{CH}$ - 13 (2) | $t_{CH}$ - 13 (2) | $t_{CH}$ - 9.1(2) | ns |
| $t_{RLRH}$ | NRD Pulse Width | $t_{CP}$ - 2 (1) | | | | ns |
| | | $t_{CP}$ /2 - 2 (2) | | | | ns |
| $t_{UBHCD}$ | NUB High to Chip Select Disabled | 0 | | | | ns |
| $t_{WACK}$ | NWAIT Setup Before MCKI High | 8 | | | | ns |
| $t_{WAHCK}$ | NWAIT Hold After MCKI High | 4 | | | | ns |
| $t_{WHCD}$ | NWR High to Chip Select Disabled | 2 | | | | ns |
| $t_{WHDX}$ | Data Out Hold After NWR High | 2 | | | | ns |
| $t_{WHRL}$ | NWR High to NRD Low | $t_{CL}$ | | | | ns |
| $t_{WHUBH}$ | NWR High to NUB High | 2 | | | | ns |
| $t_{WLWH}$ | NWR Pulse Width | $t_{CP}$ /2 - 2 | | | | ns |

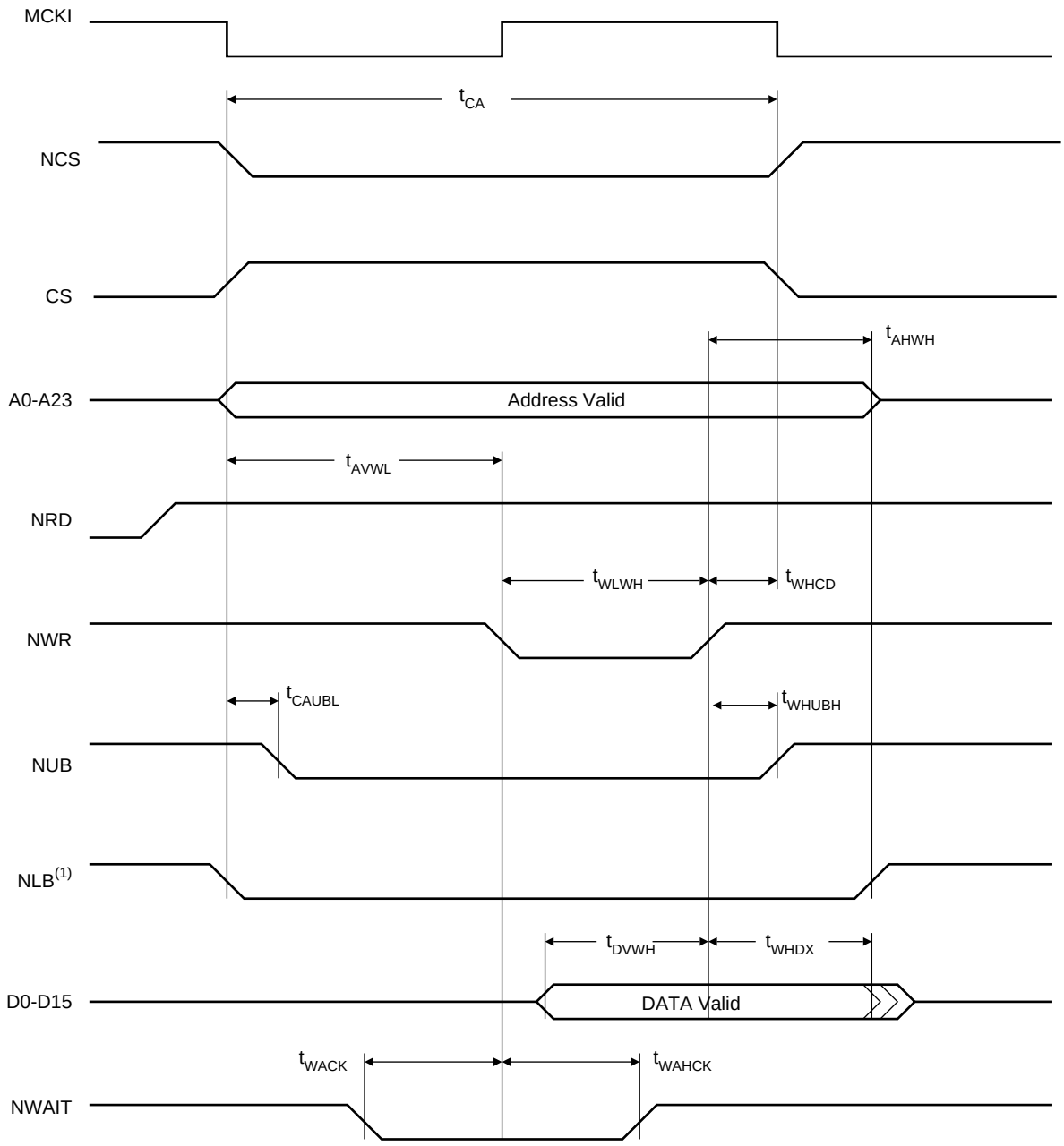
Notes: 1. Early Read Protocol
2. Standard Read Protocol

**Figure 3.** External Data Memory Read Cycle




Note: 1. Timing of NLB is equal to timing of A0-A23.

**Figure 4.** External Data Memory Write Cycle




Note: 1. Timing of NLB is equal to timing of A0-A23.

## EBI Signals Relative to MCKI

The following tables show timings relative to operating condition limits (best case and worst case). See Figure 5.

**Table 6.** General Purpose EBI Signals

| Symbol | Parameter | Best Case | Worst Case | | | Units |
|---|---|---|---|---|---|---|
| | | | -25AC | -25AI | -33AC | |
| $EBI_1$ | MCKI Falling to NUB Valid | 6 | 21 | 22 | 15 | ns |
| $EBI_2$ | MCKI Falling to NLB/A0 Valid | 6 | 21 | 23 | 15 | ns |
| $EBI_3$ | MCKI Falling to A7-A1 Valid | 6 | 21 | 22 | 15 | ns |
| $EBI_4$ | MCKI Falling to A23-A8 Valid | 6 | 20 | 21 | 14 | ns |
| $EBI_5$ | MCKI Falling to Chip Select | 5 | 20 | 21 | 14 | ns |
| $EBI_6$ | NWAIT Setup Before MCKI Rising | 4 | 8 | 8 | 6 | ns |
| $EBI_7$ | NWAIT Hold After MCKI Rising | 1 | 5 | 5 | 4 | ns |

**Table 7.** EBI Write Signals

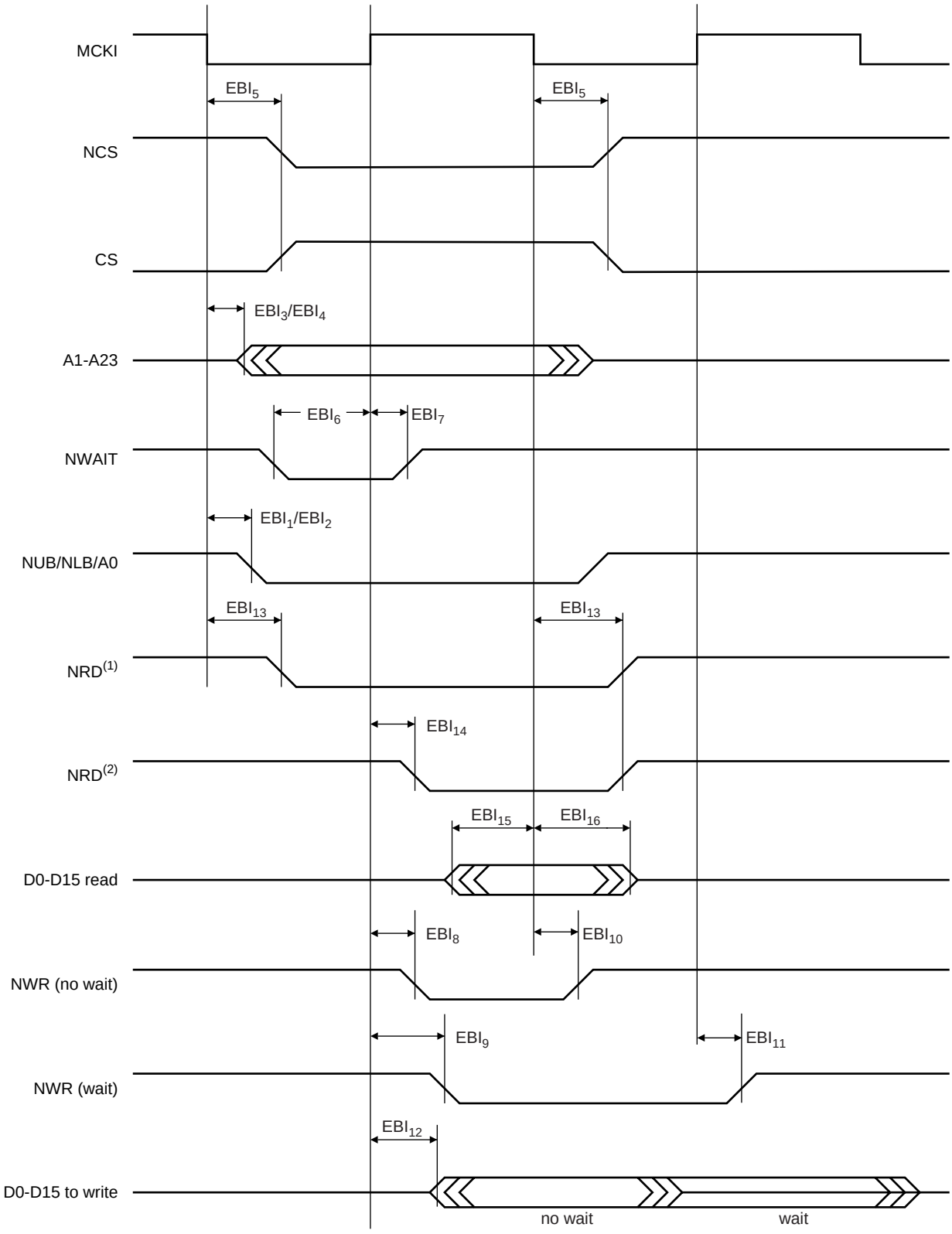
| Symbol | Parameter | Best Case | Worst Case | | | Units |
|---|---|---|---|---|---|---|
| | | | -25AC | -25AI | -33AC | |
| $EBI_8$ | MCKI Rising to NWR Active (No Wait) | 4 | 16 | 17 | 12 | ns |
| $EBI_9$ | MCKI Rising to NWR Active (Wait) | 4 | 17 | 18 | 12 | ns |
| $EBI_{10}$ | MCKI Falling to NWR Inactive (No Wait) | 5 | 19 | 20 | 14 | ns |
| $EBI_{11}$ | MCKI Rising to NWR Inactive (Wait) | 4 | 18 | 19 | 13 | ns |
| $EBI_{12}$ | MCKI Rising to D0-D15 Out Valid | 5 | 21 | 22 | 15 | ns |

**Table 8.** EBI Read Signals

| Symbol | Parameter | Best Case | Worst Case | | | Units |
|---|---|---|---|---|---|---|
| | | | -25AC | -25AI | -33AC | |
| $EBI_{13}$ | MCKI Falling to NRD (1) and (2) | 5 | 17 | 18 | 12 | ns |
| $EBI_{14}$ | MCKI Rising to NRD Valid (2) | 4 | 16 | 17 | 12 | ns |
| $EBI_{15}$ | D0-D15 in Setup Before MCKI Falling | 2 | 3 | 3 | 3 | ns |
| $EBI_{16}$ | D0-D15 in Hold After MCKI Falling | 1 | 2 | 2 | 2 | ns |

Notes: 1. Early Read Protocol
2. Standard Read Protocol

**Figure 5.** EBI Signals Relative to MCKI




Notes: 1. Early Read Protocol
2. Standard Read Protocol

## Peripheral Signals Relative to MCKI

### USART Signals

**Table 9.** USART Outputs

| Symbol | Mode | Parameter | Best Case | Worst Case | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | -25AC | -25AI | -33AC | |
| $US_1$ | Asynchronous | MCKI Rising to SCK Output Rising/Falling | 6 | 23 | 25 | 17 | ns |
| $US_2$ | Asynchronous | MCKI Rising to TXD Toggling | 7 | 25 | 27 | 18 | ns |
| $US_3$ | Synchronous | SCK Output Falling to TXD Toggling | 1 | 4 | 4 | 3 | ns |
| $US_4$ | Synchronous | SCK Input Falling to TXD Toggling | $t_{CP}$ + 7 | $2(t_{CP})$ + 25 | $2(t_{CP})$ + 27 | $2(t_{Cp})$ + 18 | ns |

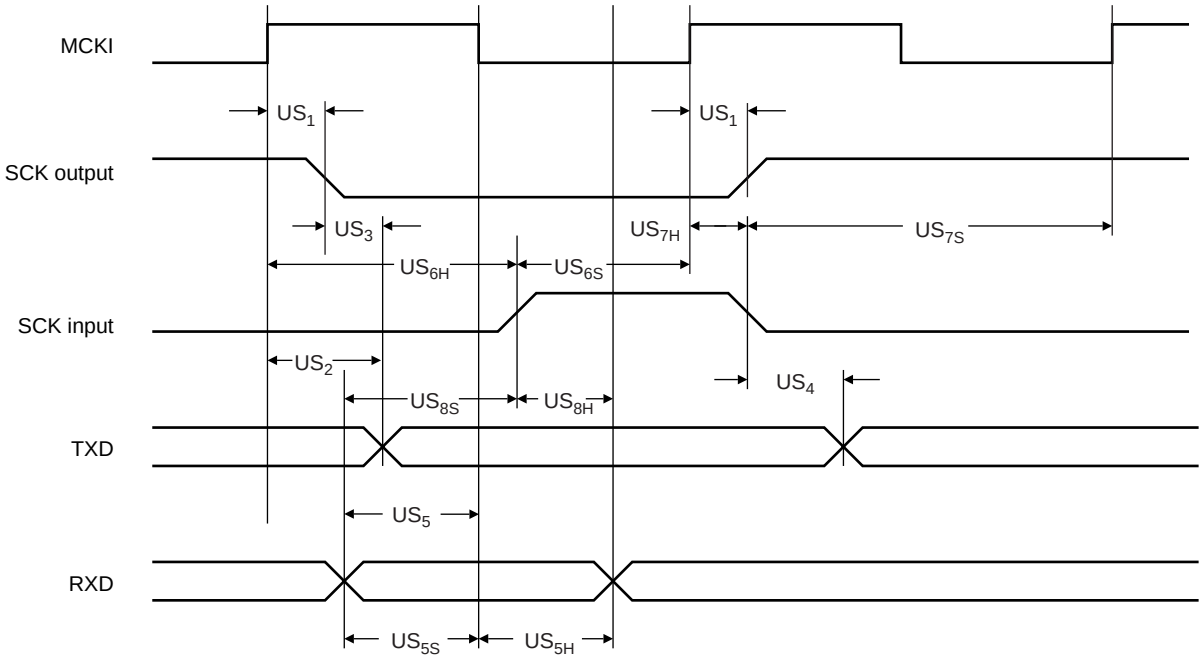
The inputs can be used synchronously or asynchronously (in relation to MCKI).

For synchronous USART inputs, certain setup/hold constraints must be met. These constraints are shown in the Table 10 and are represented in Figure 6.

**Table 10.** USART Setup/Hold Constraints

| Symbol | Mode | Parameter | Setup | Hold | Units |
|---|---|---|---|---|---|
| $US_5$ | Asynchronous | RXD Toggling Relative to MCKI Falling | 6 | 2 | ns |
| $US_6$ | Asynchronous | SCK Input Rising Relative to MCKI Rising | 7 | 1 | ns |
| $US_7$ | Asynchronous | SCK Input Falling Relative to MCKI Rising | 6 | 1 | ns |
| $US_8$ | Synchronous | RXD Toggling Relative to SCK Input Rising | $t_{CP}$ /2 - 1 | $t_{CP}$ /2 + 1 | ns |

**Figure 6.** USART Signals Relative to MCKI



### Timer Counter Signals

Due to internal synchronization of input signals, there is a delay between an input event and a corresponding output event. This delay is 3($t_{CP}$) in Waveform Event Detection Mode and 4($t_{CP}$) in Waveform Total-Count Detection Mode.

**Table 11.** Timer Outputs

| Symbol | Parameter | Best Case | Worst Case | | | Units |
|---|---|---|---|---|---|---|
| | | | -25AC | -25AI | -33AC | |
| $TC_1$ | MCKI Rising to TIOA Rising | 5 | 17 | 18 | 12 | ns |
| $TC_2$ | MCKI Rising to TIOA Falling | 4 | 16 | 17 | 12 | ns |
| $TC_3$ | MCKI Rising to TIOB Rising | 5 | 18 | 19 | 13 | ns |
| $TC_4$ | MCKI Rising to TIOB Falling | 5 | 17 | 18 | 12 | ns |

The inputs can be used synchronously or asynchronously (in relation to MCKI).

For synchronous Timer inputs, certain setup/hold constraints must be met. These constraints are shown in the Table 12 and are represented in Figure 7.

For asynchronous inputs, a minimum pulse width and a minimum input period are necessary as shown in Tables 13 and 14 and as represented in Figure 7.

**Table 12.** Timer Synchronous Inputs

| Symbol | Type of Input | Parameter | Setup | Hold | Units |
|---|---|---|---|---|---|
| $TC_5$ | Synchronous | TIOA/TIOB Rising Relative to MCKI Rising | 5 | 2 | ns |
| $TC_6$ | Synchronous | TIOATIOB Falling Relative to MCKI Rising | 4 | 2 | ns |
| $TC_7$ | Synchronous | TCLK Rising Relative to MCKI Rising | 6 | 1 | ns |
| $TC_8$ | Synchronous | TCLK Falling Relative to MCKI Rising | 5 | 2 | ns |

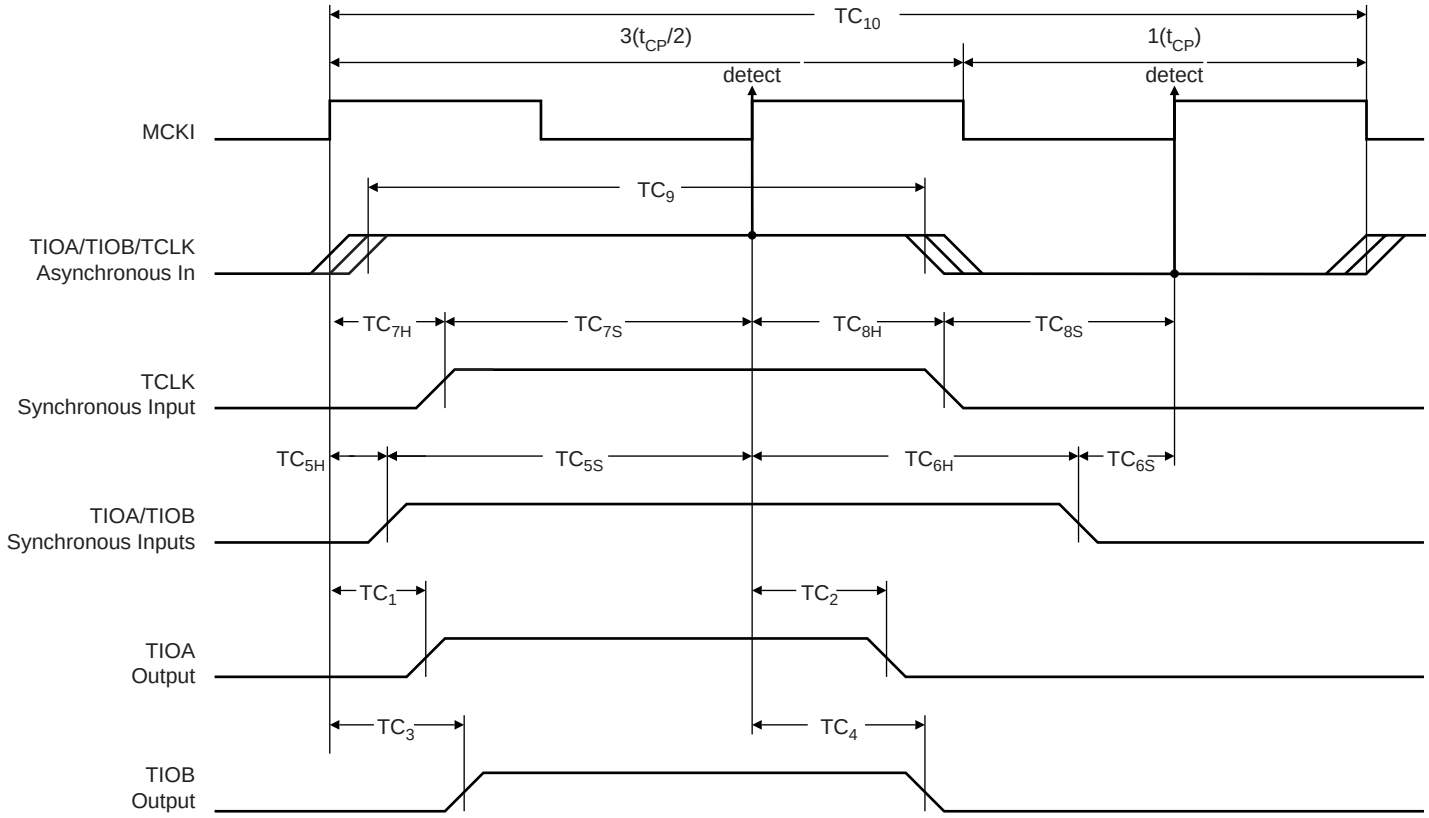
**Table 13.** Timer Asynchronous Input Minimum Pulse Width

| Symbol | Type of Inputs | Parameter | Pulse Width | Units |
|---|---|---|---|---|
| $TC_9$ | Asynchronous | TCLK/TIOA/TIOB Minimum Pulse Width | 3($t_{CP}$/2) | ns |

**Table 14.** Timer Asynchronous Input Minimum Input Period

| Symbol | Type of Inputs | Parameter | Input Period | Units |
|---|---|---|---|---|
| $TC_{10}$ | Asynchronous | TCLK/TIOA/TIOB Minimum Input Period | 5($t_{CP}$/2) | ns |

**Figure 7.** Timer Relative to MCKI

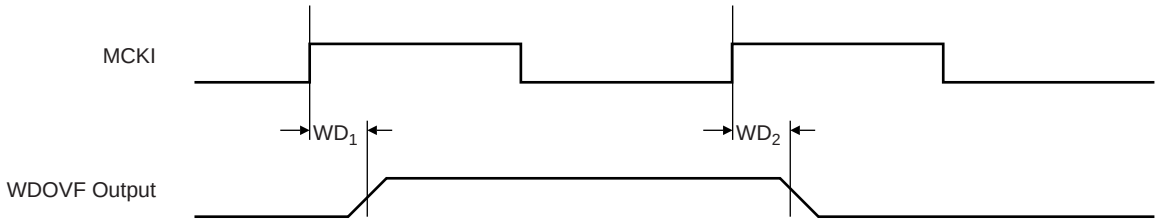


### Watchdog Timer Signals

**Table 15.** Watchdog Timer Outputs

| Symbol | Parameter | Best Case | Worst Case | | | Units |
|---|---|---|---|---|---|---|
| | | | -25AC | -25AI | -33AC | |
| $WD_1$ | MCKI Rising to WDOVF Rising | 3 | 12 | 13 | 9 | ns |
| $WD_2$ | MCKI Rising to WDOVF Falling | 4 | 13 | 14 | 10 | ns |

**Figure 8.** Watchdog Signals Relative to MCKI




### Reset Signals

Certain setup/hold constraints must be met. These constraints are shown in Table 16 and are represented in Figure 9.

**Table 16.** Reset Setup/Hold Constraints

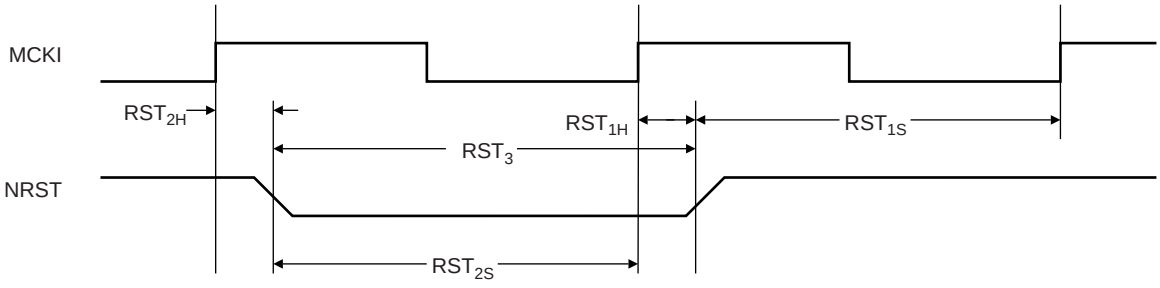
| Symbol | Parameter | Setup | Hold | Units |
|---|---|---|---|---|
| $RST_1$ | NRST Rising Related to MCKI Rising | 2 | 2 | ns |
| $RST_2$ | NRST Falling related to MCKI Rising | 2 | 1 | ns |

A minimum pulse width is necessary as shown in Table 17 and as represented in Figure 9.

**Table 17.** Reset Minimum Pulse Width

| Symbol | Parameter | Pulse Width | Units |
|---|---|---|---|
| $RST_3$ | NRST Minimum Pulse Width | $10(t_{CP})$ | ns |

**Figure 9.** Reset Signals Relative to MCKI



### Advanced Interrupt Controller Signals

The inputs can be used synchronously or asynchronously (in relation to MCKI).

For synchronous AIC inputs, certain setup/hold constraints must be met. These constraints are shown in Table 18 and are represented in Figure 10.

For asynchronous inputs, a minimum pulse width is necessary as shown in Table 19 and as represented in Figure 10.

**Table 18.** AIC Synchronous Input Setup/Hold Constraints

| Symbol | Type | Parameter | Setup | Hold | Units |
|---|---|---|---|---|---|
| $AIC_1$ | Synchronous | P24/FIQ/IRQ Rising Relative to MCKI Rising | 5 | 1 | ns |
| $AIC_2$ | Synchronous | P24/FIQ/IRQ Falling Related to MCKI Rising | 5 | 1 | ns |
| $AIC_3$ | Synchronous | IRQ Rising Related to MCKI Rising | 7 | 1 | ns |
| $AIC_4$ | Synchronous | IRQ Falling Related to MCKI Rising | 6 | 1 | ns |

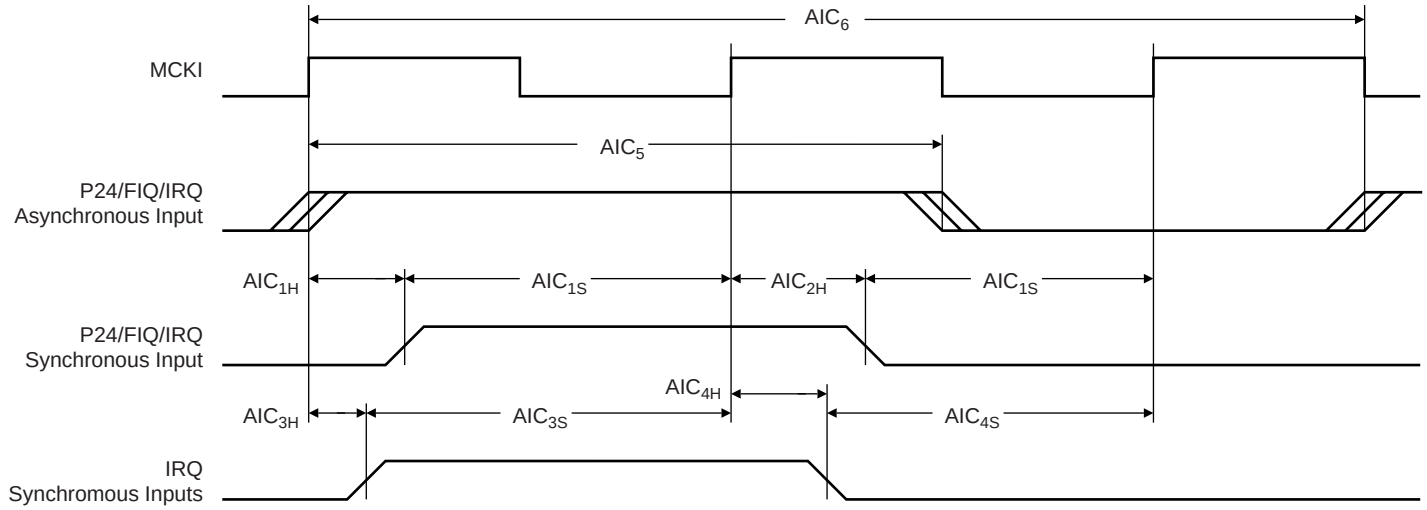
**Table 19.** AIC Asynchronous Input Minimum Pulse Width

| Symbol | Type | Parameter | Pulse Width | Units |
|---|---|---|---|---|
| $AIC_5$ | Asynchronous | P24/FIQ/IRQ Minimum Pulse Width | $3(t_{CP}/2)$ | ns |

**Table 20.** AIC Asynchronous Input Minimum Input Period

| Symbol | Type | Parameter | Input Period | Units |
|---|---|---|---|---|
| $AIC_6$ | Asynchronous | AIC Minimum Input Period | $5(t_{CP}/2)$ | ns |

**Figure 10.** AIC Signals Relative to MCKI



### Parallel I/O Signals

**Table 21.** PIO Outputs

| Symbol | Parameter | Best Case | Worst Case | | | Units |
|---|---|---|---|---|---|---|
| | | | -25AC | -25AI | -33AC | |
| $PIO_1$ | MCKI Falling to PIO Output Rising | 4 | 20 | 21 | 15 | ns |
| $PIO_2$ | MCKI Falling to PIO Output Falling | 5 | 17 | 18 | 13 | ns |

The inputs can be used synchronously or asynchronously (in relation to MCKI).

For synchronous PIO inputs, certain setup/hold constraints must be met. These constraints are shown in the Table 22 and are represented in Figure 11.

For asynchronous inputs, a minimum pulse width is necessary as shown in Table 23 and as represented in Figure 11.

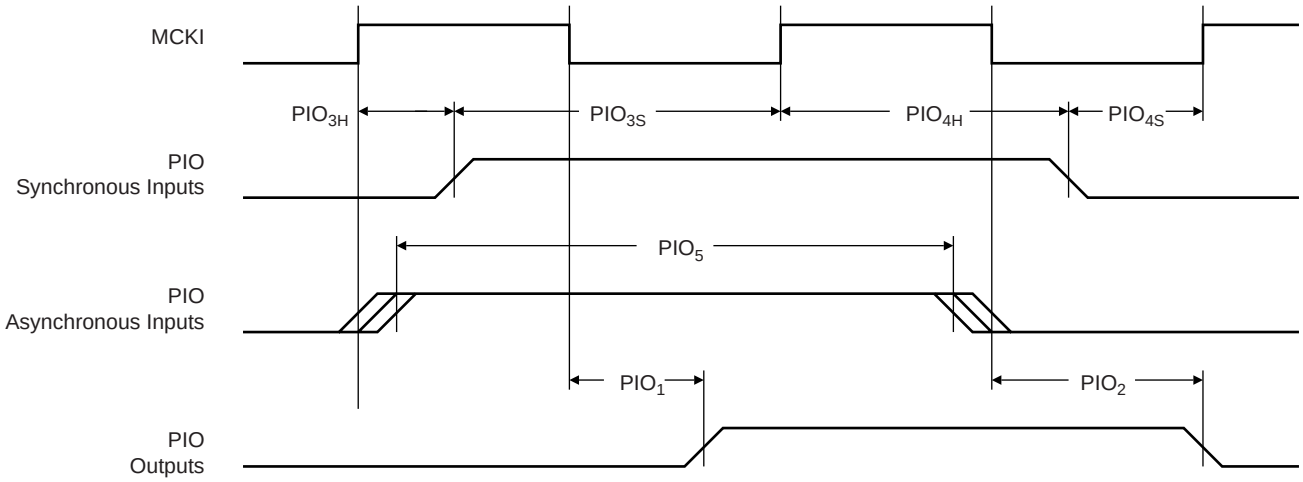
**Table 22.** PIO Synchronous Input Setup/Hold Constraints

| Symbol | Type | Parameter | Setup | Hold | Units |
|---|---|---|---|---|---|
| $PIO_3$ | Synchronous | PIO Input Rising Related to MCKI Rising | 3 | 4 | ns |
| $PIO_4$ | Synchronous | PIO Input Falling Related to MCKI Rising | 4 | 4 | ns |

**Table 23.** PIO Asynchronous Input Minimum Pulse Width

| Symbol | Type | Parameter | Pulse Width | Units |
|---|---|---|---|---|
| $PIO_5$ | Asynchronous | PIO Input Minimum Pulse Width | $3(t_{CP}/2)$ | ns |

**Figure 11.** PIO Signals Relative to MCKI



## Clock Waveforms

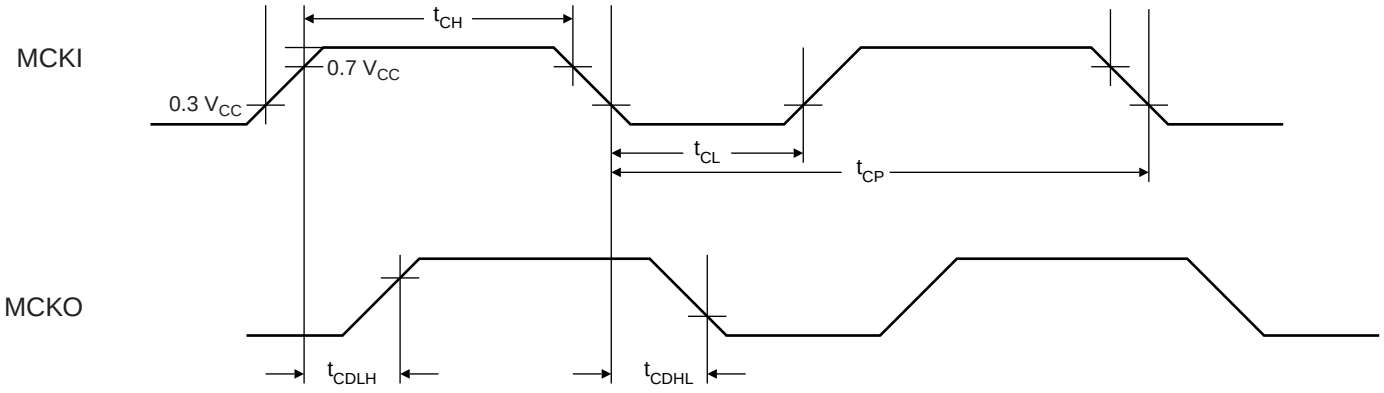
**Table 24.** Clock Waveform Parameters

| Symbol | Parameter | Minimum | | Maximum | | Units |
|---|---|---|---|---|---|---|
| | | -33AC | -25AI | -33AC | -25AI | |
| $1/t_{CP}$ | Oscillator Frequency | | | 33 | 25 | MHz |
| $t_{CP}$ | Main Clock Period | 30 | 40 | | | ns |
| $t_{CH}$ | High Time | 12 | 17 | | | ns |
| $t_{CL}$ | Low Time | 12 | 17 | | | ns |

**Table 25.** Clock Propagation Times

| Symbol | Parameter | Best Case | Nominal Case | Worst Case | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | -25AC | -25AI | -33AC | |
| $t_{CDLH}$ | Rising Edge Propagation Time | 3 | 6 | 11 | 12 | 9 | ns |
| $t_{CDHL}$ | Falling Edge Propagation Time | 3 | 6 | 11 | 12 | 9 | ns |

**Figure 12.** Clock Waveform



# Package Outline TQPF 100

## 100-Lead, Thin (1.4 mm) Quad Flat Pack

**Table 26.** Common Dimensions (mm)

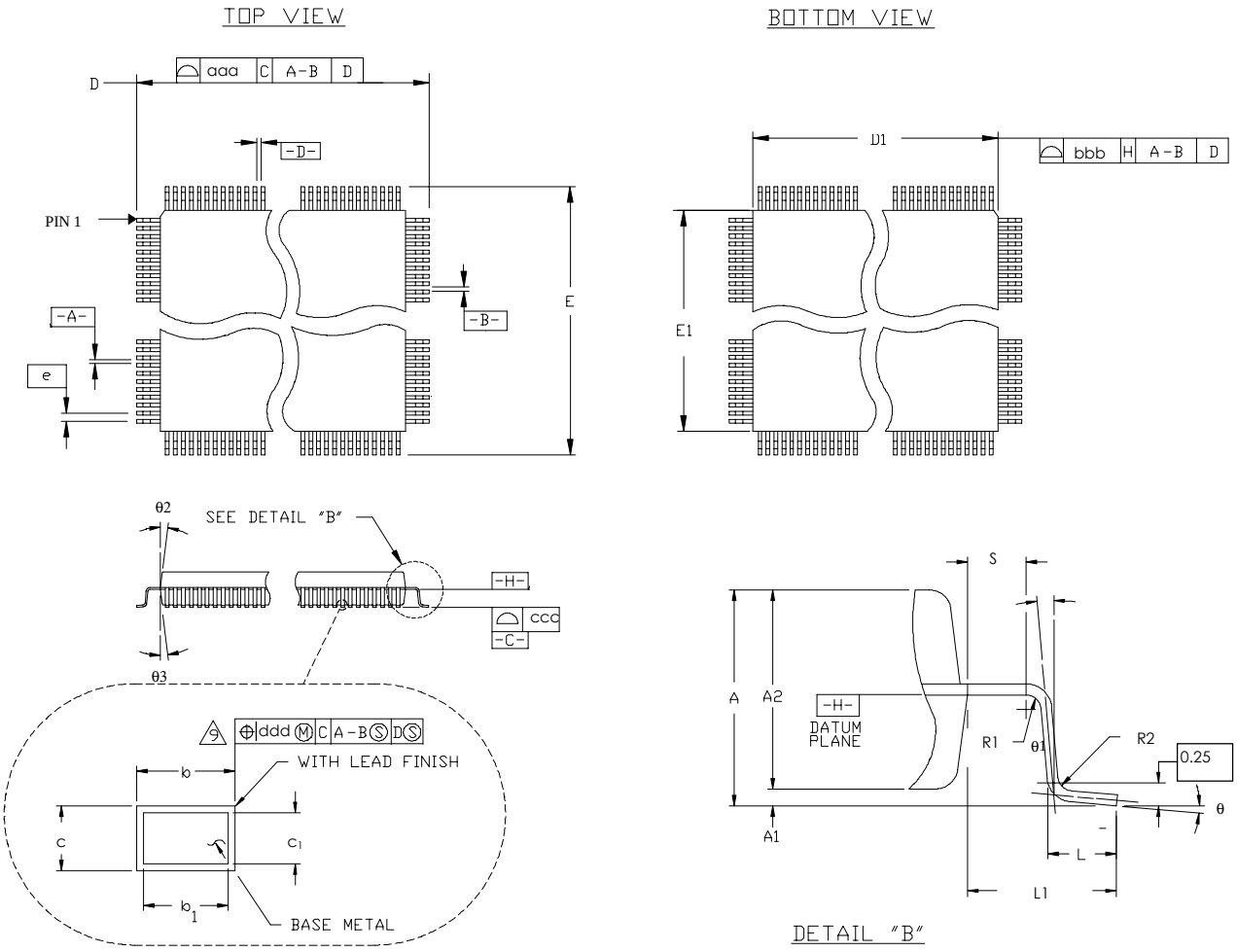
| Symbol | Min | Nom | Max |
|---|---|---|---|
| c | 0.09 | | 0.2 |
| c1 | 0.09 | | 0.16 |
| L | 0.45 | 0.6 | 0.75 |
| L1 | | 1.00 REF | |
| R2 | 0.08 | | 0.2 |
| R1 | 0.08 | | |
| S | 0.2 | | |
| θ | 0° | 3.5° | 7° |
| θ1 | 0° | | |
| θ2 | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° |
| A | | | 1.6 |
| A1 | 0.05 | | 0.15 |
| A2 | 1.35 | 1.4 | 1.45 |
| **Tolerances of form and position** | | | |
| aaa | | 0.2 | |
| bbb | | 0.2 | |

**Table 27.** Lead Count Dimensions

| Pin Count | D/E BSC | D1/E1 BSC | b | | | b1 | | | e BSC | ccc | ddd |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | Min | Nom | Max | | | |
| 100 | 16.0 | 14.0 | 0.17 | 0.22 | 0.27 | 0.17 | 0.2 | 0.23 | 0.50 | 0.10 | 0.06 |

Thermal resistance of package: 40°C/W.

**Figure 13.** TQFP 100 Package Drawing



## Ordering Information

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|---|---|---|---|---|
| 25 | 2.7V to 3.6V | AT91M40400-25AC | TQFP 100 | Commercial (0°C to 70°C) |
| | | AT91M40400-25AI | TQFP 100 | Industrial (-40°C to 85°C) |
| 33 | 2.7V to 3.6V | AT91M40400-33AC | TQFP 100 | Commercial (0°C to 70°C) |