Features

- **ARM7TDMI™ ARM® Thumb® Processor Core**
  - **High-performance 32-bit RISC Architecture**
  - **High-density 16-bit Instruction Set**
  - **Leader in MIPS/Watt**
  - **Embedded ICE (In-Circuit Emulation)**
- **4K Bytes RAM**
- **1M 16-bit Words Flash Memory**
  - **Single Voltage Read/Write**
  - **100 ns Access Time**
  - **Sector Erase Architecture**
  - **Fast Word Program Time: 20 µs**
  - **Fast Sector Erase Time: 200 ms**
  - **Dual Plane Organization allows Concurrent Read and Program/Erase**
  - **Erase Suspend Capability**
  - **Low-power Operation: 25 mA Active — 10 µA Standby**
  - **Data Polling, Toggle Bit and Ready/Busy End of Program Cycle Detection**
  - **RESET Input for Device Initialization**
  - **Sector Program Unlock Command**
- **Fully Programmable External Bus Interface (EBI)**
  - **Maximum External Address Space of 64M Bytes**
  - **Up to 8 Chip Selects**
  - **Software Programmable 8/16-bit External Data Bus**
- **8-level Priority, Individually Maskable, Vectored Interrupt Controller**
  - **4 External Interrupts, including a High-priority Low-latency Interrupt Request**
- **32 Programmable I/O Lines**
- **3-channel 16-bit Timer/Counter**
  - **3 External Clock Inputs**
  - **2 Multi-purpose I/O Pins per Channel**
- **2 USARTs**
  - **2 Dedicated Peripheral Data Controller (PDC) Channels per USART**
- **Programmable Watchdog Timer**
- **Low-power Idle Mode**
- **Fully Static Operation: 0 Hz to 25 MHz**
- **2.7V to 3.6V Operating Range**
- **-40°C to 85°C Operating Temperature Range**
- **Available in a 120-ball BGA Package**

Description

The AT91F40416 is a member of the Atmel AT91 16/32-bit Microcontroller family which is based on the ARM7TDMI processor core.

The processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The eight-level priority-vectored interrupt controller, together with the Peripheral Data Controller, significantly enhance real-time device performance.

By combining the microcontroller, featuring on-chip RAM and a wide range of peripheral functions, with 16M bits of Flash memory in a single compact 120-ball BGA package, the Atmel AT91F40416 provides a powerful, flexible and cost-effective solution to many compute-intensive embedded control applications and offers significant board size and system cost reductions.

The Flash memory may be programmed while powered by the single device supply, making the AT91F40416 ideal for in-system programmable applications.

AT91
ARM® Thumb® Microcontrollers

AT91F40416

Rev. 1317A–10/99

Pin Configuration

Figure 1. AT91F40416 Pinout (120-ball BGA, Top View)

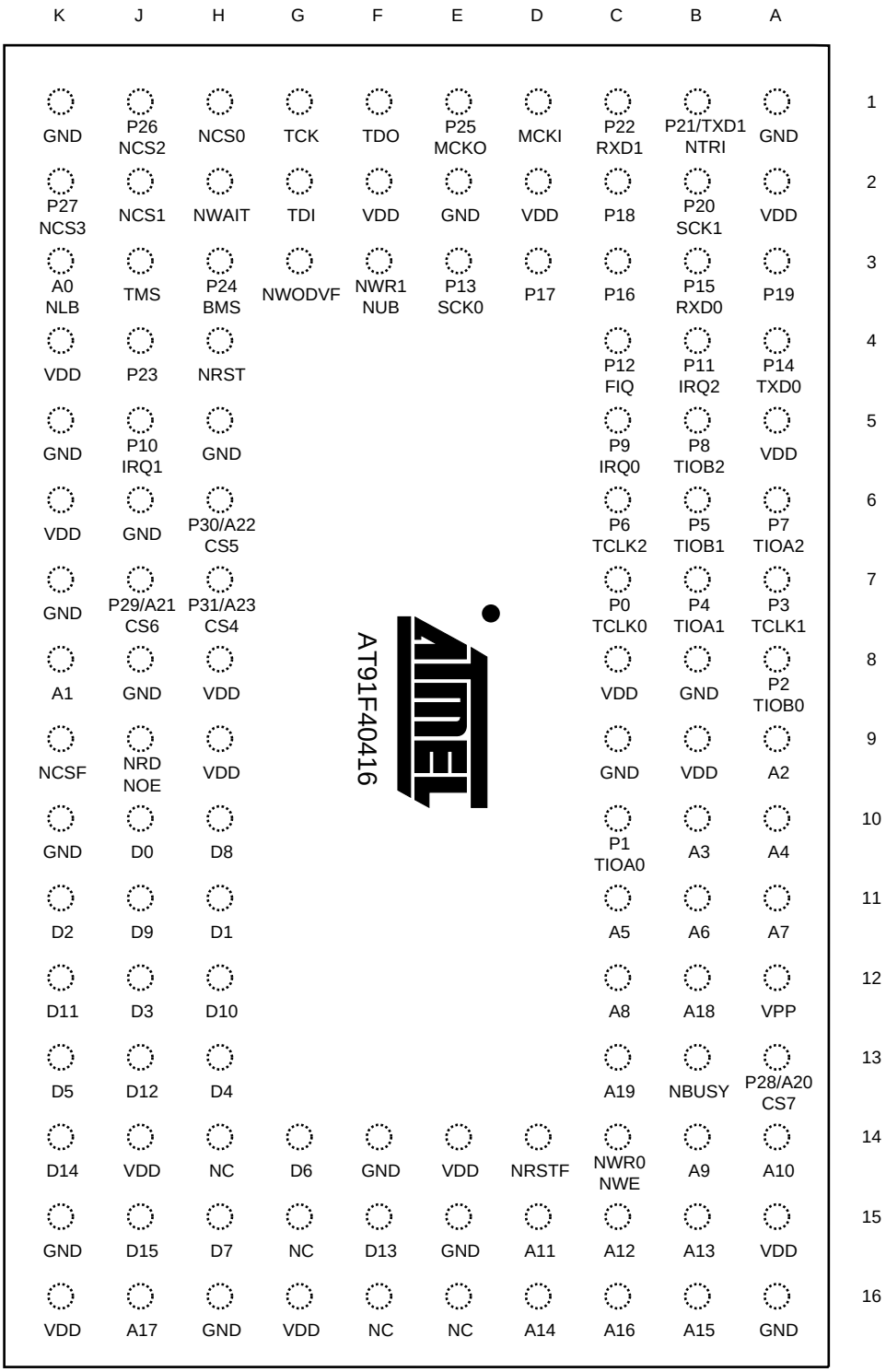
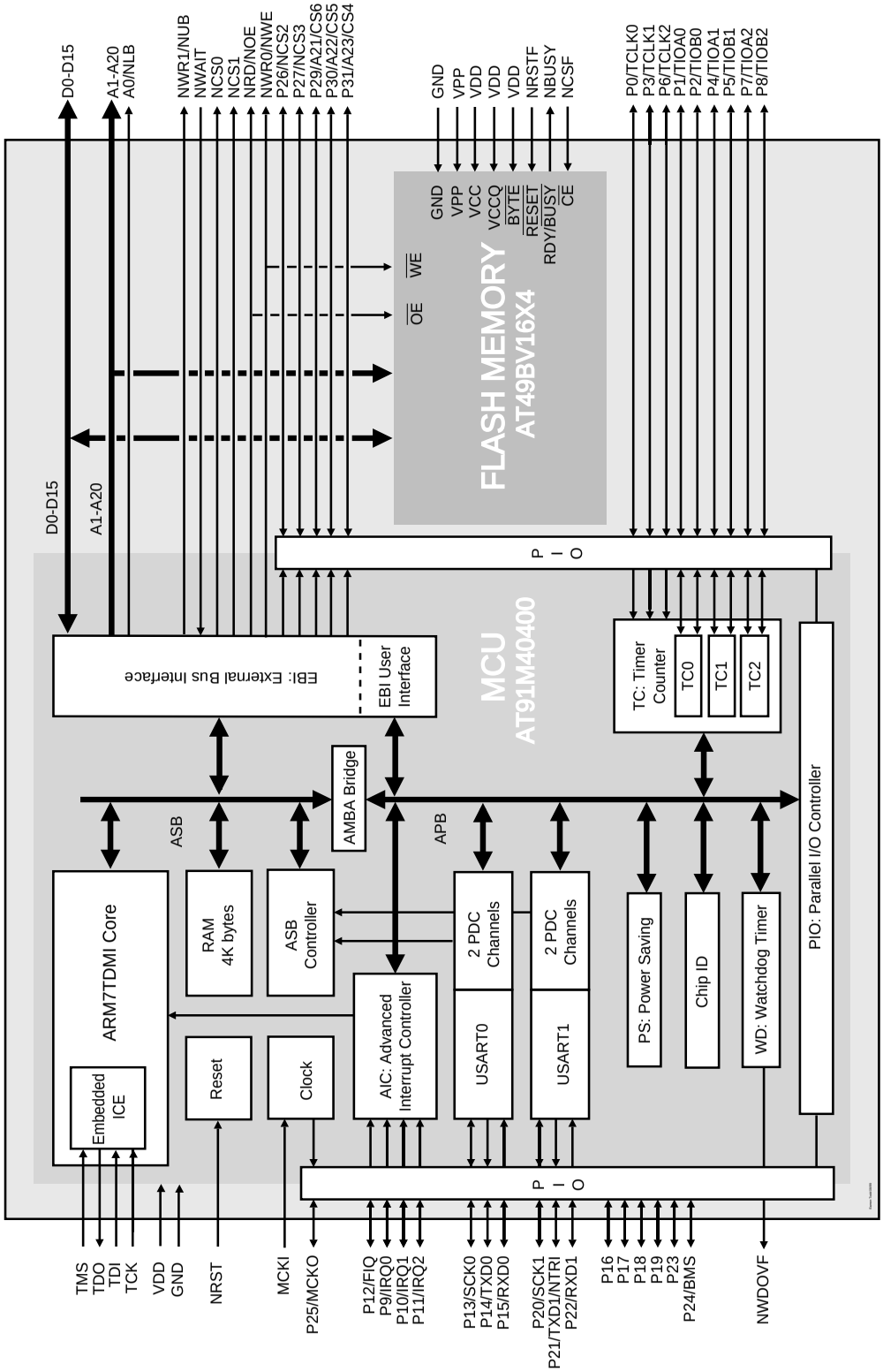


Table 1. AT91F40416 Pin Description

Module	Name	Function	Type	Active Level	Comments
EBI	A0-A23	Address Bus	Output	—	Valid after reset; do not reprogram A20 to I/O, as it is MSB of Flash address
	D0-D15	Data Bus	I/O	—	
	NCS0-NCS3	External Chip Select	Output	Low	Used to select external devices
	CS4-CS7	External Chip Select	Output	High	A23-A20 after reset
	NWR0	Lower Byte 0 Write Signal	Output	Low	Used in Byte Write option
	NWR1	Upper Byte 1 Write Signal	Output	Low	Used in Byte Write option
	NRD	Read Signal	Output	Low	Used in Byte Write option
	NWE	Write Enable	Output	Low	Used in Byte Select option
	NOE	Output Enable	Output	Low	Used in Byte Select option
	NUB	Upper Byte Select	Output	Low	Used in Byte Select option
	NLB	Lower Byte Select	Output	Low	Used in Byte Select option
	NWAIT	Wait Input	Input	Low	
	BMS	Boot Mode Select	Input	—	Sampled during reset; must be low for Flash to be used as boot memory
AIC	FIQ	Fast Interrupt Request	Input	—	PIO controlled after reset
	IRQ0-IRQ2	External Interrupt Request	Input	—	PIO controlled after reset
Timer	TCLK0-TCLK2	Timer External Clock	Input	—	PIO controlled after reset
	TIOA0-TIOA2	Multipurpose Timer I/O Pin A	I/O	—	PIO controlled after reset
	TIOB0-TIOB2	Multipurpose Timer I/O Pin B	I/O	—	PIO controlled after reset
USART	SCK0-SCK1	External Serial Clock	I/O	—	PIO controlled after reset
	TXD0-TXD1	Transmit Data Output	Output	—	PIO controlled after reset
	RXD0-RXD1	Receive Data Input	Input	—	PIO controlled after reset
PIO	P0-P31	Parallel IO line	I/O	—	
WD	NWDOVF	Watchdog Overflow	Output	Low	Open drain
Clock	MCKI	Master Clock Input	Input	—	Schmidt trigger
	MCKO	Master Clock Output	Output	—	
Reset	NRST	Hardware Reset Input	Input	Low	Schmidt trigger, internal pull-up
	NTRI	Tristate Mode Select	Input	Low	Sampled during reset
ICE	TMS	Test Mode Select	Input	—	Schmidt trigger, internal pull-up
	TDI	Test Data Input	Input	—	Schmidt trigger, internal pull-up
	TDO	Test Data Output	Output	—	
	TCK	Test Clock	Input	—	Schmidt trigger, internal pull-up
Flash Memory	NCSF	Flash Memory Select	Input	Low	Enables Flash Memory when pulled low
	NBUSY	Flash Memory Busy Output	Output	Low	Flash RDY/$\overline{\text{BUSY}}$ signal; open-drain
	NRSTF	Flash Memory Reset Input	Input	Low	Resets Flash to standard operating mode
Power	VDD	Power	Power	—	All VDD and all GND pins **MUST** be connected to their respective supplies by the shortest route
	GND	Ground	Ground	—	
	VPP	Faster Program/Erase Voltage	Power	—	Contact Atmel

Block Diagram

Figure 1. AT91F40416



Architectural Overview

The AT91F40416 integrates Atmel's AT91M40400 ARM Thumb MCU and its AT49BV16X4 16-Mbit Flash memory die in a single compact 120-ball BGA device. The address, data and control signals, except the Flash memory enable, are internally interconnected.

The AT91F40416 is built around two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). The ASB is designed for maximum performance. It interfaces the processor with the on-chip 32-bit memories, as well as with external memories and devices via the External Bus Interface (EBI). The APB is designed for accesses to on-chip peripherals and is optimized for low power consumption. The AMBA Bridge provides an Atmel-enhanced interface between the ASB and the APB.

The Flash memory is organized as 1M 16-bit words, accessed via the EBI. Its main intended function is as a program memory. A 16-bit Thumb instruction can be loaded from Flash memory in a single clock cycle. Separate MCU and Flash memory Reset inputs (NRST and NRSTF) are provided for maximum flexibility: the user is thus free to tailor reset operation to his application.

An on-chip Peripheral Data Controller (PDC) transfers data between the on-chip USARTs and the on and off-chip memories without processor intervention. Most importantly, the PDC removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64k contiguous bytes without reprogramming the starting address. As a result, the performance of the microcontroller is enhanced and its power consumption reduced.

The AT91F40416 peripherals are designed to be programmed with a minimum number of instructions. Each peripheral has a 16K-byte address space allocated in the upper 3M bytes of the 4G byte address space. Except for the interrupt controller, the peripheral base address is the lowest address of its memory space. The peripheral register set is composed of control, mode, data, status and interrupt registers.

To maximize the efficiency of bit manipulation, frequently written registers are mapped into three memory locations. The first address is used to set individual register bits, the second resets the bits and the third address reads the value stored in the register. A bit can be set or reset by writing a one to the corresponding bit position at the appropriate register address. Writing a zero has no effect. Individual bits can thus be modified without having to use lengthy read-modify-write or complex bit manipulation instructions.

All the external signals associated with the on-chip peripherals are under the control of the Parallel I/O controller. The PIO controller may be programmed to insert an input glitch filter on any pin; generation of an interrupt on a input signal level change may also be programmed for any PIO controlled pin. After reset, the user must carefully program the PIO User Interface Registers in order to define which peripheral signals are connected with I/O pins.

The ARM7TDMI processor operates in little-endian mode in the microcontroller. The Processor's internal architecture and the ARM and Thumb instruction sets are described in the "ARM7TDMI (Thumb) Datasheet", Literature No. 0673.

For further detailed information the user may also consult the following Atmel documents:

- "AT91M40400 Datasheet"
  Literature No. 0768
- "AT91M40400 Electrical and Mechanical Characteristics"
  Literature No. 1078
- AT49BV16x4 "16-megabit 3-volt Only Flash Memory"
  Literature No. 0925

The ARM Standard In-Circuit-Emulation debug interface is supported via the ICE port of the microcontroller. (This is not a standard IEEE 1149.1 JTAG Boundary Scan interface).

PDC: Peripheral Data Controller

The AT91F40416 has a 4-channel PDC dedicated to the two on-chip USARTs. One PDC channel is connected to the receiving channel and one to the transmitting channel of each USART.

A PDC channel user interface is integrated within the memory space of each USART channel: it contains a 32-bit address pointer register and a 16-bit byte count register. When the programmed number of bytes have been transferred, an end-of-transfer interrupt is generated by the corresponding USART.

Flash Memory

The 16-Mbit Flash memory is organized as 1,048,576 16-bit words whose contents appear on D0-D15. The Flash memory is addressed as 16-bit words via the EBI. It uses address lines A1 to A20. Address line A20 must on no account be reprogrammed as an I/O pin or as a chip select, as it is the most significant bit of the Flash memory address.

The address, data and control signals, except the Flash memory enable, are internally interconnected. The user should connect the Flash memory enable (NCSF) to one of the active-low chip selects on the EBI; NCS0 must be used if the Flash memory is to be the boot memory device. In addition, if the Flash memory is to be used as boot memory, the BMS input must be pulled down externally in order for the processor to perform correct 16-bit fetches on reset. The user must ensure that all VDD and all GND pins are connected to their respective supplies by the shortest route.

The Flash memory powers-on in the read mode. Command sequences are used to place the device in other operating modes, such as program and erase.

A separate Flash memory reset input pin (NRSTF) is provided for maximum flexibility: the user is thus free to tailor reset operation to his application. When this input is at a logic high level, the memory is in its standard operating mode; a low level on this input halts the current memory operation and puts its outputs in a high impedance state.

The Flash memory features data polling to detect the end of a program cycle: while a program cycle is in progress, an attempted read of the last word written will return the complement of the written data on I/O7. An open drain READY/BUSY output pin provides another method of detecting the end of a program or erase cycle. This pin is pulled low while program and erase cycles are in progress and is released at the completion of the cycle. A toggle bit feature provides a third means of detecting the end of a program or erase cycle.

The Flash memory is segmented into two memory planes. Reads from one memory plane may be performed even while program or erase functions are being executed in the other memory plane. This feature enhances performance by not requiring the system to wait for a program or erase cycle to complete before a read may be performed.

The Flash memory is divided into 40 sectors for erase operations. To further enhance device flexibility, an Erase Suspend feature is offered. This feature puts the erase cycle on hold for an indefinite period and allows the user to read data from, or to write data to, any other sector within the same memory plane. There is no need to suspend an erase cycle if the data to be read is in the other memory plane. The device has the capability to protect data stored in any sector. Once the data protection for a sector is enabled, the data in that sector cannot be changed while input levels lie between ground and V_{DD}.

An optional VPP pin is available to enhance program/erase times. Please contact Atmel for more information regarding the use of this feature.

A 6-byte command sequence (Bypass Unlock) allows the device to be written to directly, using single pulses on the write control lines. This mode (Single Pulse Programming) is exited by powering down the device or by pulsing the NRSTF pin low for a minimum of 50 ns and then bringing it back to V_{DD}.

The following hardware features protect against inadvertent programming of the Flash memory:

- V_{DD} Sense: if V_{DD} is below 1.8V (typical), the program function is inhibited.
- V_{DD} Power-on Delay: once V_{DD} has reached the V_{DD} sense level, the device will automatically time out 10 ms (typically) before programming.
- Program Inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles.
- Noise Filter: pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

Electrical Characteristics, Device Operation and Command Sequences are fully documented in the AT49BV16X4 Flash Memory Datasheet entitled “16-megabit 3-volt Only Flash Memory”, Literature No. 0925.

EBI: External Bus Interface

The EBI generates the signals which control the access to the external memory or peripheral devices. The EBI is fully programmable and can address up to 64M bytes. It has eight chip selects and a 24-bit address bus, the upper four bits of which are multiplexed with a chip select.

The 16-bit data bus can be configured to interface with 8- or 16-bit external devices. Separate read and write control signals allow for direct memory and peripheral interfacing.

The EBI supports different access protocols allowing single clock cycle memory accesses.

The main features are:

- External memory mapping
- Up to eight chip select lines
- 8- or 16-bit data bus
- Byte-write or byte-select lines
- Remap of boot memory
- Two different read protocols
- Programmable wait state generation
- External wait request
- Programmable data float time

AIC: Advanced Interrupt Controller

The AT91F40416 has an 8-level priority, individually maskable, vectored interrupt controller. This feature substantially reduces the software and real time overhead in handling internal and external interrupts.

The interrupt controller is connected to the NFIQ (fast interrupt request) and the NIRQ (standard interrupt request) inputs of the ARM7TDMI processor. The processor's NFIQ line can only be asserted by the external fast interrupt request input: FIQ. The NIRQ line can be asserted by the interrupts generated by the on-chip peripherals and the external interrupt request lines: IRQ0 to IRQ2.

An 8-level priority encoder allows the customer to define the priority between the different NIRQ interrupt sources.

Internal sources are programmed to be level sensitive or edge triggered. External sources can be programmed to be positive or negative edge triggered or high or low level sensitive.

PIO: Parallel I/O Controller

The AT91F40416 has 32 programmable I/O lines. Five pins on the AT91F40416 are available as general purpose I/O pins (P16, P17, P18, P19, and P23). Other I/O lines are multiplexed with on-chip peripheral signals in order to optimize the use of available package pins. The PIO controller enables generation of a bit-maskable interrupt on input level change as well as the insertion of bit-enablable input glitch filter on any of the PIO pins.

USART: Universal Synchronous/ Asynchronous Receiver/Transmitter

The AT91F40416 provides two identical, full-duplex, universal synchronous/asynchronous receiver/transmitters which are connected to the Peripheral Data Controller.

The main features are:

- Programmable baud rate generator
- Parity, framing and overrun error detection
- Line break generation and detection
- Automatic echo, local loopback and remote loopback channel modes
- Multi-drop mode: address detection and generation
- Interrupt generation
- Two dedicated peripheral data controller channels
- 5-, 6-, 7- and 8-bit character length

TC: Timer Counter

The AT91F40416 features a Timer Counter (TC) block which includes three identical 16-bit timer counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

Each timer counter channel has three external clock inputs, five internal clock inputs, and two multi-purpose input/output signals which can be configured by the user. Each channel drives an internal interrupt signal which can be programmed to generate processor interrupts via the AIC (Advanced Interrupt Controller).

The Timer Counter block has two global registers which act upon all three TC channels. The Block Control Register allows the three channels to be started simultaneously with the same instruction. The Block Mode Register defines the external clock inputs for each timer counter channel, allowing them to be chained.

WD: Watchdog Timer

The AT91F40416 has an internal watchdog timer which can be used to reset the system if the software becomes trapped in a deadlock. An active-low signal, NWDOVF, is generated for external use, on watchdog overflow.

PS: Power Saving

The AT91F40416 Power Saving module provides a low-power idle mode. In Idle mode, the CPU clock is deactivated while all on-chip peripherals and the RAM remain active. The contents of the on-chip RAM and all the special function registers remain unchanged during this mode. The Idle mode can be terminated by any enabled interrupt or by a hardware Reset.

SF: Special Function

The AT91F40416 provides registers which implement the following special functions.

- Chip identification
- RESET status

Emulation Functions

Tristate Mode

The AT91F40416 features a tristate mode, which is used for debug purposes in order to connect an emulator probe to an application board.

ICE Debug Mode

ARM standard embedded In-Circuit Emulation is supported via the ICE port. It is connected to a host computer via an external ICE Interface.

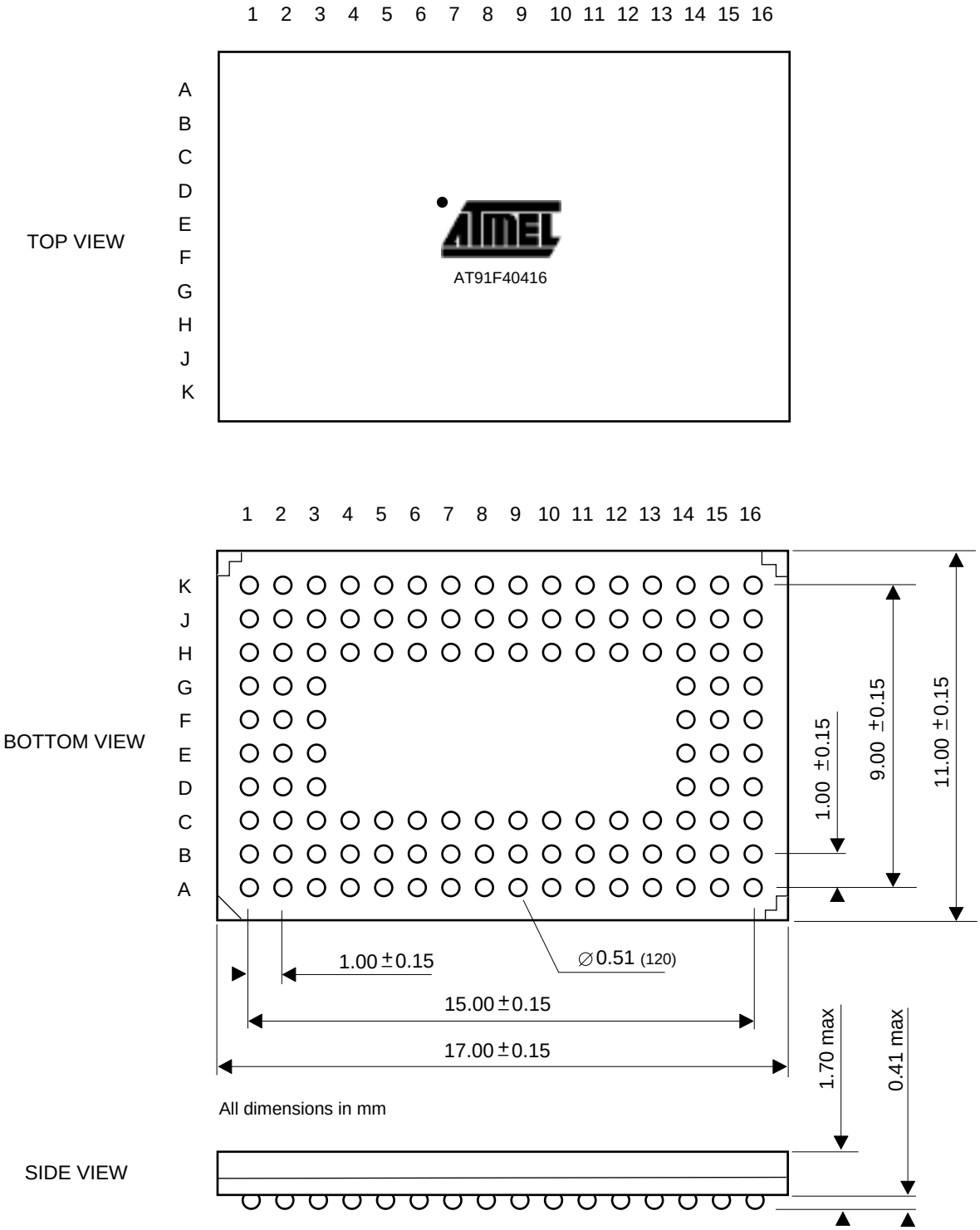
In ICE Debug Mode the ARM core responds with a non-JTAG chip ID which identifies the core to the ICE system. This is not JTAG IEEE 1149.1 compliant.

Ordering Information

Speed (MHz)	Power Supply Operating Range	Ordering Code	Package	Temperature Operating Range
25	2.7V to 3.6V	AT91M40416-25CC	BGA 120	Commercial (0°C to 70°C)
		AT91M40416-25CI	BGA 120	Industrial (-40°C to 85°C)

Package Outline BGA 120

Figure 2. 120-ball Ball Grid Array Package



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