Features

- **Compatible with MCS-51™ products**
- **On-chip Flash Program Memory**
  - **Endurance: 1,000 Write/Erase Cycles**
- **On-chip EEPROM Data Memory**
  - **Endurance: 100,000 Write/Erase Cycles**
- **512 x 8-bit RAM**
- **ISO 7816 I/O Port**
- **Random Word Generator**
- **Two 16-bit Timers**
- **Six Interrupt Sources, Two-Level Interrupt Priority**
- **Security features**
  - **Power-Down Protection**
  - **Low-Frequency Protection and High-Frequency Filter**
- **Low-Power Idle and Power-Down Modes**
- **Bond Pads Locations Conform to ISO 7816-3**
- **Temperature Range: 0 to 70°C**

Description

The AT89SC series is a low-power, high-performance 8-bit microcontroller family with Flash programmable and erasable read only memory and EEPROM data memory. The devices are manufactured using Atmel's high-density CMOS technology and are compatible with the industry standard 80C51 and 80C52 instruction set.

By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89SC is a powerful microcontroller which provides a highly flexible and cost-effective solution to many smart card applications.

The AT89SC family provides the following standard features: 16K to 24K bytes of system programmable Flash, 8K to 16K bytes of EEPROM, 512 bytes of RAM, two 16-bit timers, a six-vector, two-level interrupt and clock circuitry.

In addition, this product has the following dedicated features to smart card applications: ISO 7816 I/O Port, random word generator, and power and frequency protection logic.

Table 1. The AT89SC Family

Device Name	Flash	EEPROM	RAM
AT89SC168[1]	16K bytes	8K bytes	256 bytes
AT89SC168A	16K bytes	8K bytes	512 bytes
AT89SC1616A	16K bytes	16K bytes	512 bytes
AT89SC248A	24K bytes	8K bytes	512 bytes

Note: 1. The description of the AT89SC family of products found in this datasheet is not valid for the AT89SC168. For this particular product, please refer to the first edition of AT89SC Microcontrollers for Smart Cards datasheet (literature number 0674A).

8-Bit Flash Microcontroller for Smart Cards

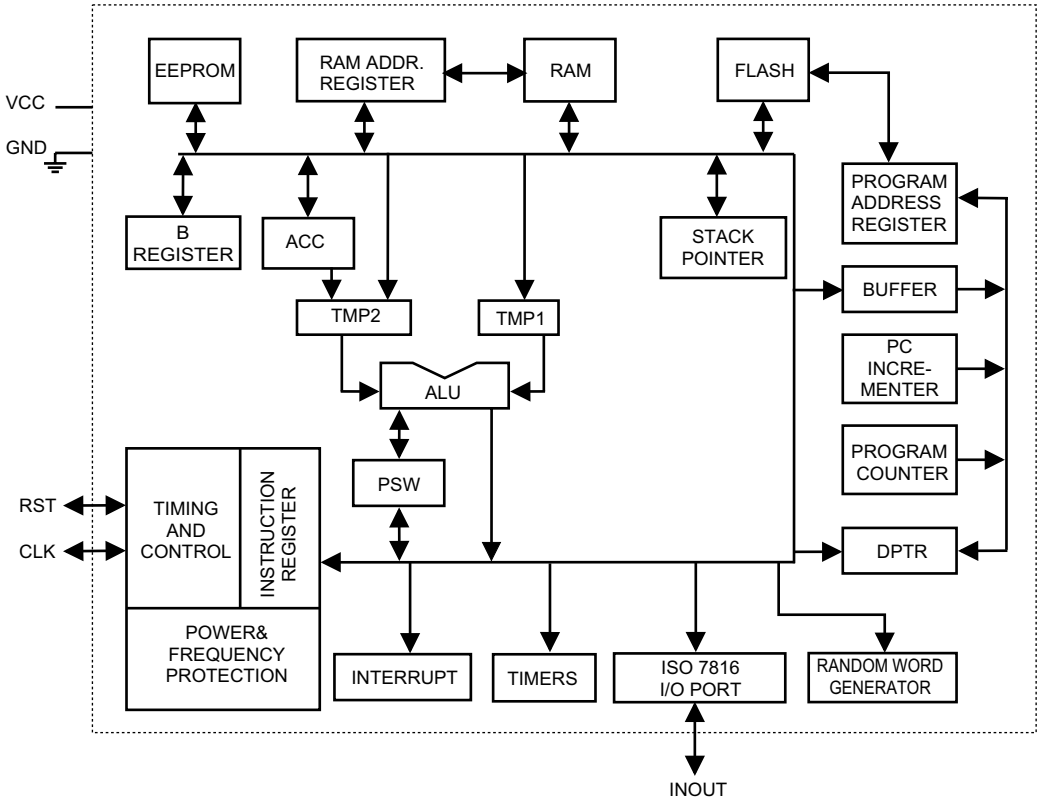
AT89SCXXXXA Summary

Complete datasheet available under NDA

Rev. 0674BS–04/98

Block Diagram

Figure 1. AT89SC System Block Diagram



Overview

CPU

The CPU is compatible with the industry standard 80C51 and 80C52 instruction set.

Reduced Power Modes

To exploit the power savings for smart cards available in CMOS circuitry, Atmel's microcontrollers have two software-invoked reduced power modes.

IDLE MODE: The CPU is turned off while the RAM and other on-chip peripherals continue operating. In this mode, current draw is reduced to approximately 15 percent of the current drawn when the device is fully active.

POWER-DOWN MODE: All on-chip activities are suspended while the on-chip RAM continues to hold its data. In this mode, the device typically draws less than 200 µA.

In addition, the devices are designed using static logic which does not require continuous clocking. That is, the clock frequency can be slowed or even stopped while waiting for an internal event.

Security Features

The AT89SC microcontroller provides the following security features:

- Power-down protection
- Low frequency protection against static analysis
- High-frequency filter against intrusion
- Shipping and initialization protected by Transport Code
- Unique serial number
- Hardware Protection: layout, bus scrambling, others (undisclosed)

Memory Organization

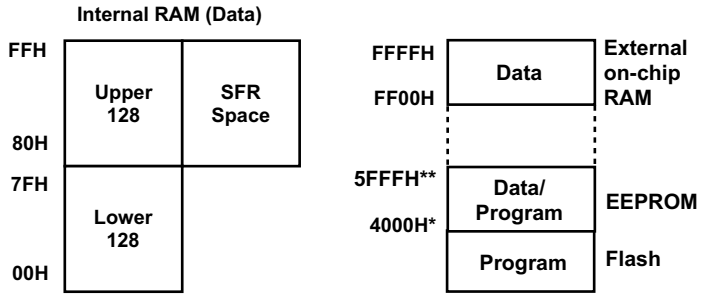
The AT89SC microcontrollers have the following memory organization, as shown in Figure 2.

- 16-bit addressable Flash programmable and erasable read-only memory
- 16-bit addressable data/program memory (EEPROM)
- 16-bit addressable data memory (external on-chip RAM)
- 8-bit addressable data memory (internal RAM plus SFRs)

The logical separation of program and data memory allows the data memory to be accessed by 8-bit addresses, which can be more quickly stored and manipulated by an 8-bit CPU. Nevertheless, 16-bit data memory can also be generated through the DPTR register.

Program memory is read-only in normal operational mode. Both Flash memory and EEPROM memory program locations are directly addressable. The EEPROM memory program locations follow the Flash memory space.

Figure 2. The AT89SC Memory(1)



Note: 1. These addresses apply to the AT89SC168A. The address should be scaled according to the memory size of the device as shown in the table below.

Device	*	**
AT89SC168A	4000H	5FFFH
AT89SC1616A	4000H	7FFFH
AT89SC248A	6000H	7FFFH

Program Memory

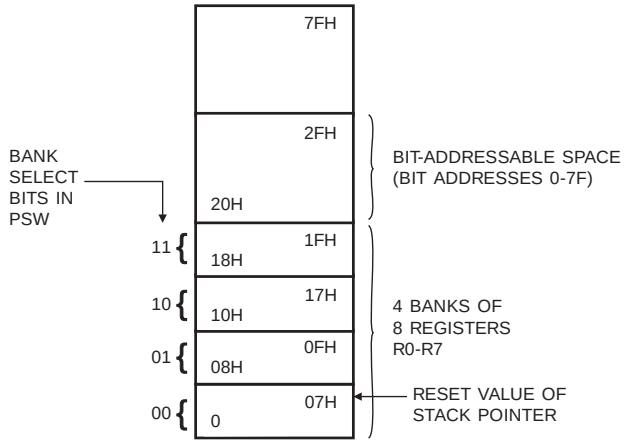
The AT89SC Microcontroller has separate address spaces for program memory and data memory. Each product contains 16K or 24K bytes of Flash program memory. The EEPROM can be optionally used as a program memory extension if more space is needed.

Data Memory

The AT89SC can directly address up to 16K bytes of EEPROM data memory. The MOVX instruction accesses the EEPROM data memory (refer to the “Instruction Set” section in this datasheet for a more detailed description of instructions).

The AT89SC family also features 256 bytes of internal RAM including a number of Special Function Registers (SFR). The lower 128 bytes of RAM can be accessed either by direct addressing (MOV data addr) or by indirect addressing (MOV @ Ri). The upper 128 bytes of RAM can only be accessed by indirect addressing. Figure 2 shows the AT89SC data memory organization. In addition, 256 bytes of external on-chip RAM are accessible with the MOVX @ DPTR instruction from address FF00H to FFFFH.

Figure 3. The Lower 128 Bytes of Internal RAM



The Instruction Set

All members of the Atmel AT89SC 8-bit microcontroller family execute the same instruction set. This instruction set is optimized for 8-bit control applications and provides a variety of fast addressing modes for accessing the RAM to facilitate byte operations on small data structures. The instruction set provides extensive support for 1-bit variables as a separate data type, allowing direct bit manipulation in control and logic systems that require Boolean processing.

Addressing Modes

The AT89SC microcontroller instruction set includes the following addressing modes:

- Direct Addressing: Operand is specified by an 8-bit address field.
- Indirect Addressing: Operand is specified by an 8- or 16-bit register.
- Register Instructions: Operand is a register (R0-R7) of selected bank.
- Register-Specific Instructions: Instruction is specific to a certain register and operand is implicit.
- Immediate Constants: Operand is specified by an 8- or 16-bit register field.
- Indexed Addressing: Access to program memory.

Instruction Type

- Data Transfers
  - From/to internal RAM
  - From/to external on-chip RAM (except AT89SC168)
  - From/to EEPROM
  - From Flash
- Arithmetic and logical Instructions
  - Manipulations on bytes
- Boolean Instructions
  - Manipulations and test on bits
- Jump Instructions
  - Unconditional jump
  - Conditional jump
  - Subroutine call and return
  - Interrupt Return

Download Mode

The AT89SC microcontroller has a special functional mode which allows the Flash to be written for new software download. The new software is loaded through the ISO port and written into the Flash memory. This download mode is software controlled, so if the software in use does not contain the download facility, no new program can be loaded.

Master Clock Generation

The master clock of the CPU is generated from the external ISO 7816 clock. In the rest of this document, all timing values will be given with reference to the master clock MCLK.

Interrupt Structure

The AT89SC core provides up to five interrupt sources: two timer interrupts, a security interrupt, a memory interrupt, and an external interrupt.

Each of the interrupt sources can be individually enabled or disabled by setting or clearing the corresponding Interrupt Enable (IE) bit in the SFR. This register also contains a global disable bit, which can be cleared to disable all interrupts at once, disregarding the state of each individual bit enable.

Each interrupt source can also be individually programmed to one of two priority levels by setting or clearing the corresponding Interrupt Priority (IP) bit in the SFR.

Some applications require more than the two priority levels that are provided by on-chip hardware in Atmel microcontrollers. In this case, relatively simple software can be written to produce the same effect as a third priority level.

Random Word Generator

The random word generator provides a 32-bit random word located in four SFRs: RDW0, RDW1, RDW2, RDW3. These four registers operate as a 32-bit shift register with feedback. The feedback loop gives the longest cycle (number of clock runs between two occurrences of the same sequence) and the maximum spread between two consecutive generated numbers (two snapshots separated by one clock pulse).

The random word generator is driven by an internal ring oscillator which runs much faster than the CPU clock. The speed of the oscillator depends on the process used, the supply voltage and the substrate temperature for each product.

Reset

The active low RST pin is filtered to generate an active high internal reset signal. Holding this RST pin low for at least two machine cycles (12 MCLK periods) while the oscillator is running accomplishes a CPU reset. A clock frequency over 10 MHz or a power supply lower than 2.6V automatically drives the internal reset line high. It is released once the power supply or the clock frequency has returned to its normal operating value.

Power-On Reset

The AT89SC microcontrollers have an internal Power-On reset. When power is turned on, the circuit holds this signal high for three machine cycles. The CPU reset is a logical OR between power-on reset and the internal reset signal.

Timers

The AT89SC features two 16-bit timer registers: Timer 0 and Timer 1. These registers are incremented every machine cycle. Thus, the register counts machine cycles. Since a machine cycle consists of 6 MCLK periods, the count rate is 1/6 of the MCLK frequency.

In addition to the timer functions, Timer 0 and Timer 1 have four operating modes: 13-bit timer, 16-bit timer, 8-bit autoreload, split timer.

ISO 7816 I/O Port

The I/O Port is supported by a single I/O port line. It is managed by software which conforms to ISO 7816 standards. An interrupt can be generated on each falling edge of the I/O line.

CPU Timing

The internal clock generator defines the sequence of states that make up the microcontroller machine cycle.

Machine Cycles

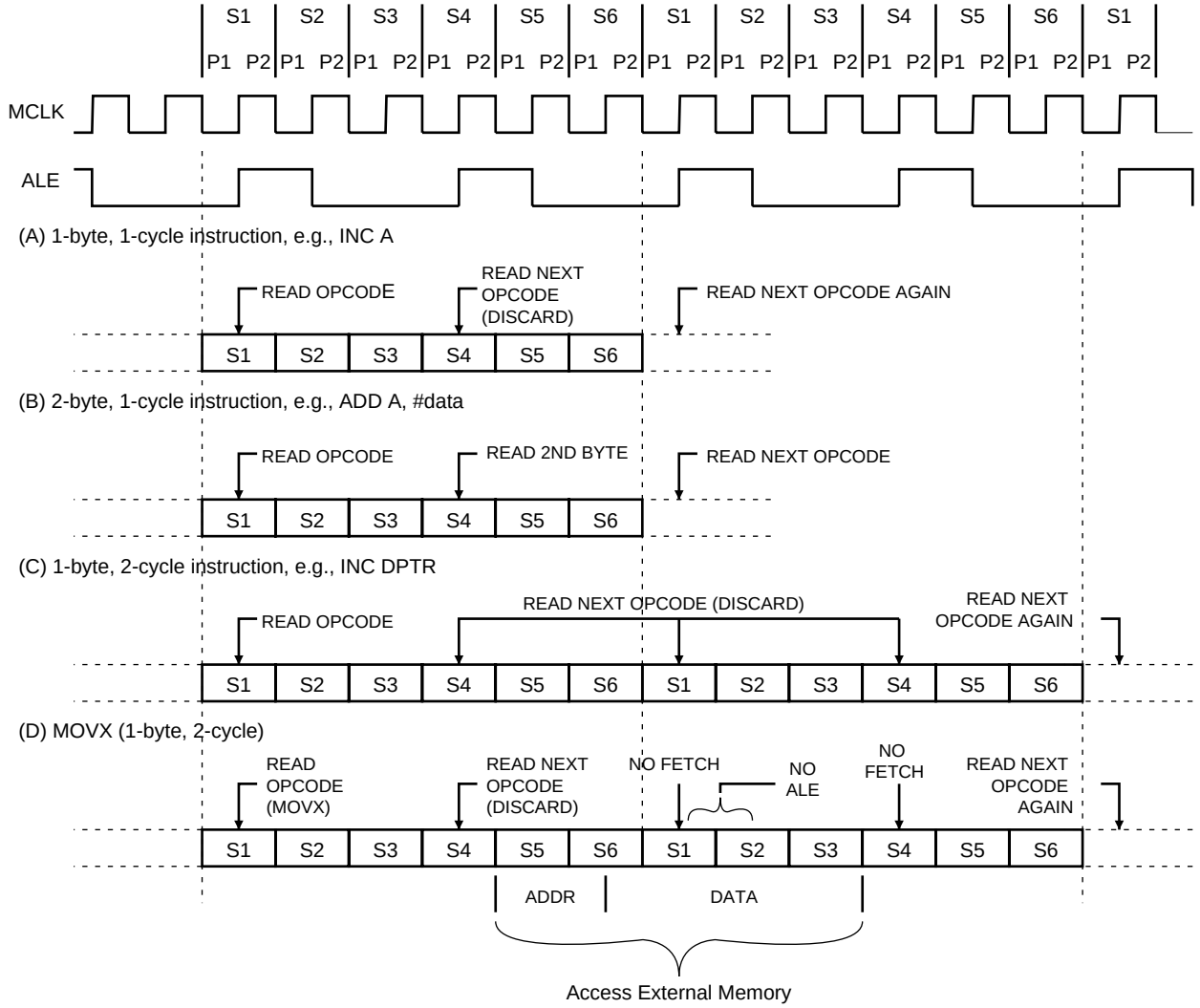
A machine cycle consists of a sequence of 6 states, numbered S1 through S6. Each state time lasts 1 MCLK period. Thus, a machine cycle lasts 6 MCLK periods or 1 ms if the clock frequency is 6 MHz.

Each state is divided into a Phase 1 half and a Phase 2 half. Figure 4 shows the fetch/execute sequences in states and phases for various kinds of instructions. Normally two program fetches are generated during each machine cycle, even if the instruction being executed does not require it. If the instruction being executed does not need more code bytes, the CPU ignores the extra fetch, and the Program Counter is not incremented.

Execution of a one-cycle instruction (Figure 4, A and B) begins during State 1 of the machine cycle, when the opcode is latched into the Instruction register. A second fetch occurs during S4 of the same machine cycle. Execution is complete at the end of State 6 of this machine cycle.

The MOVX instructions take two machine cycles to execute. No program fetch is generated during the second cycle of a MOVX instruction. This is the only time program fetches are skipped. The fetch/execute sequence for MOVX instructions is shown in Figure 4 (D).

Figure 4. State Sequences



DC/AC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Supply voltage		2.7		5.5	V
F_{OSC}	Clock input frequency		1		5	MHz
T_{CYC}	CPU cycle time			6 x MCLK		ns
W_{CT}	Memory Write Cycle Time				4.0	ms
V_{IH}	Input high voltage	I_{IH} = ± 500µA	2		Vcc	V
	INOUT CLK RST	I_{IH} = ± 20µA	0.7Vcc		Vcc	V
V_{IL}	Input low voltage INOUT CLK RST	I_{IL} = ± 1mA	0		0.8	V
V_{OH}	Output high voltage	I_{OH} = -100µA	2.4		Vcc	V
	INOUT	I_{OH} = -20µA	3.8		Vcc	V
V_{OL}	Output low voltage INOUT	I_{OL}=2mA	0		0.4	V
T_R, T_F	Output rise/fall time	C_{OUT}=30pF			1	µs
I_{CC}	Power Consumption	Active mode, 5V				
	Power Consumption	Power-down mode, 5V			200	µA

Notes: 1. A 200 Kohms pull-up resistor has been added to all the input ports.

2. A Schmitt trigger has been added to all the input ports to improve the noise immunity.

3. MCLK is the master clock period which is $1/F_{OSC}$ for the AT89SCXXXXA products