AT89SC

SECURE MICROCONTROLLERS FOR SMART CARDS

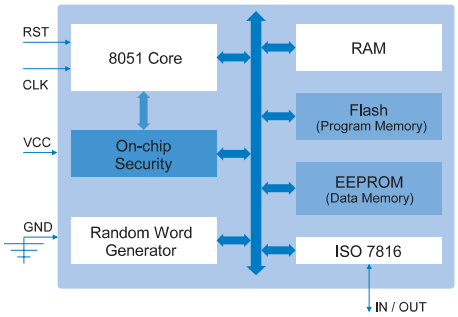
- Flash-based microcontroller
- Up to 32K Bytes of nonvolatile memory
- Flexible cost-effective solution for many smart card applications
- 8051™ architecture
  - Industry-standard
  - Two 16-bit timers
- Flash program memory
  - No delay for new release introduction
  - Same product can cope with several applications
  - Reduced time-to-market
- ISO 7816 compliant serial-interface
- Random word generator
- Many security features including:
  - Power-down protection
  - Low-frequency protection and high-frequency filter
- Low-power design
  - Low-power idle mode
  - Power-down mode
- Software Development Tool Kit available:
  - Emulator
  - Debugger (KEIL™)

Name	Flash Bytes	EEPROM Bytes	RAM Bytes	T=0 Hardware	Power Supply	Available
AT89SC168	16K	8K	256	Yes	5V	Now
AT89SC168A	16K	8K	512	No	2.7 - 5.5V	January 98
AT89SC1616A	16K	16K	512	No	2.7 - 5.5V	May 98
AT89SC248A	24K	8K	512	No	2.7 - 5.5V	June 98

The AT89SC family: 8051-based architecture & Flash program memory

AT89SC Low-power, high-performance Flash program memory

The AT89SC series is a low-power, high-performance 8-bit microcontroller with Flash program memory and EEPROM data memory. The devices are manufactured using Atmel's high-density CMOS nonvolatile memory technology.



AT89SC Block Diagram

RST - Reset input. A low on this pin for two machine cycles while the oscillator is running resets the device. This pin includes an internal pull-up resistor.

CLK - Clock input to internal clock operating circuit. This pin includes an internal pull-up resistor.

VCC - Supply voltage.

GND - Ground.

IN/OUT - IN/OUT is a single bit open drain bidirectional I/O port. As an output, the pin can sink eight TTL inputs. When 1 is written to INOUT, the pin can be used as a high-impedance input. This bidirectional pin includes a pull-up resistor.

FLASH Program Memory

- Single voltage read/write
- 64-byte page size
- Page erase/write cycle: 3.5 ms. Write Only time: 1.5 ms
- Full memory loading time: <1 s
- Minimum endurance of 1,000 write/erase cycles
- Minimum data retention of 10 years
- Self-timed memory

EEPROM Data Memory

- Single-voltage read/write
- Byte-by-byte or page-by-page write/erase (64 Bytes)
- Erase plus Write time: 3.5 ms
- Minimum endurance of 100,000 write/erase cycles
- Minimum data retention of 10 years
- 64-byte one-time-programmable security zone
- Self-timed memory

Security Features

- Shipping and Initialization protected by Transport Code
- Power-down protection
- Over-voltage protection
- Low-frequency protection against static analysis
- High-frequency filter against intrusion
- Unique serial number

If the clock frequency is lower than 500 kHz, or if the power supply is less than 4V, a security interrupt is generated and the security SFR is written to indicate the type of violation that caused the interrupt. A clock frequency over 10 MHz, or a power supply lower than 2.7V, automatically drives low the RESET line. The RESET is released once the power supply or the clock frequency has returned to its normal operating value.

Programmable Serial Interface

The ISO 7816 interface performs byte transfers as defined by the ISO 7816 standard. The parity checking is performed by the interface, and an interrupt is generated after each transaction (AT89SC168 only).

Timer 0 and 1

Timer 0 and Timer 1 in the AT89SC operate in the same way as Timer 0 and Timer 1 in the AT89C51.

Interrupts

The AT89SC has a total of six interrupt vectors: two timer interrupts (Timer 0 and 1), the serial port interrupt, external interrupt, memory interrupt and a security interrupt. Each of these interrupt sources can be individually enabled or disabled.

Idle Mode

In the Idle mode, the CPU is disabled while all on-chip peripherals (RAM, timer/counters, serial port, random word generator and interrupt system) remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode.

Power-Down Mode

In the power-down mode, the clock circuitry is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain

Secure Microcontroller Product Group

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
Tel : (+33)(0)4 42 53 60 00
Fax : (+33)(0)4 42 53 60 01

Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel : (+1)(408) 441 0311
Fax : (+1)(408) 436 4300

Europe
Atmel U.K. Ltd
Coliseum Business Centre
Riverside Way, Camberley
Surrey GU15 3YL, England
Tel : (+44)(0)(1276) 68 66 77
Fax : (+44)(0)(1276) 68 66 97

Asia
Atmel Asia Ltd
Room 1219
Chinachem Golden Plaza
77 Mody Road
Tsimshatsui East, Kowloon
Hong Kong
Tel : (+852) 272 19 778
Fax : (+852) 272 21 369

Japan
Atmel Japan KK
Tonetsu Shinkawa Bldg, 9F
1-24-8 Shinkawa
Chuo-Ku, Tokyo 104-0033
Japan
Tel : (+81) 3 3523 3551
Fax : (+81) 3 3523 7581

E-mail
literature@atmel.com

Web Site
http://www.atmel.com

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