AT5801

Preliminary Product Information

4-Channel Motor driver for Portable CD Player

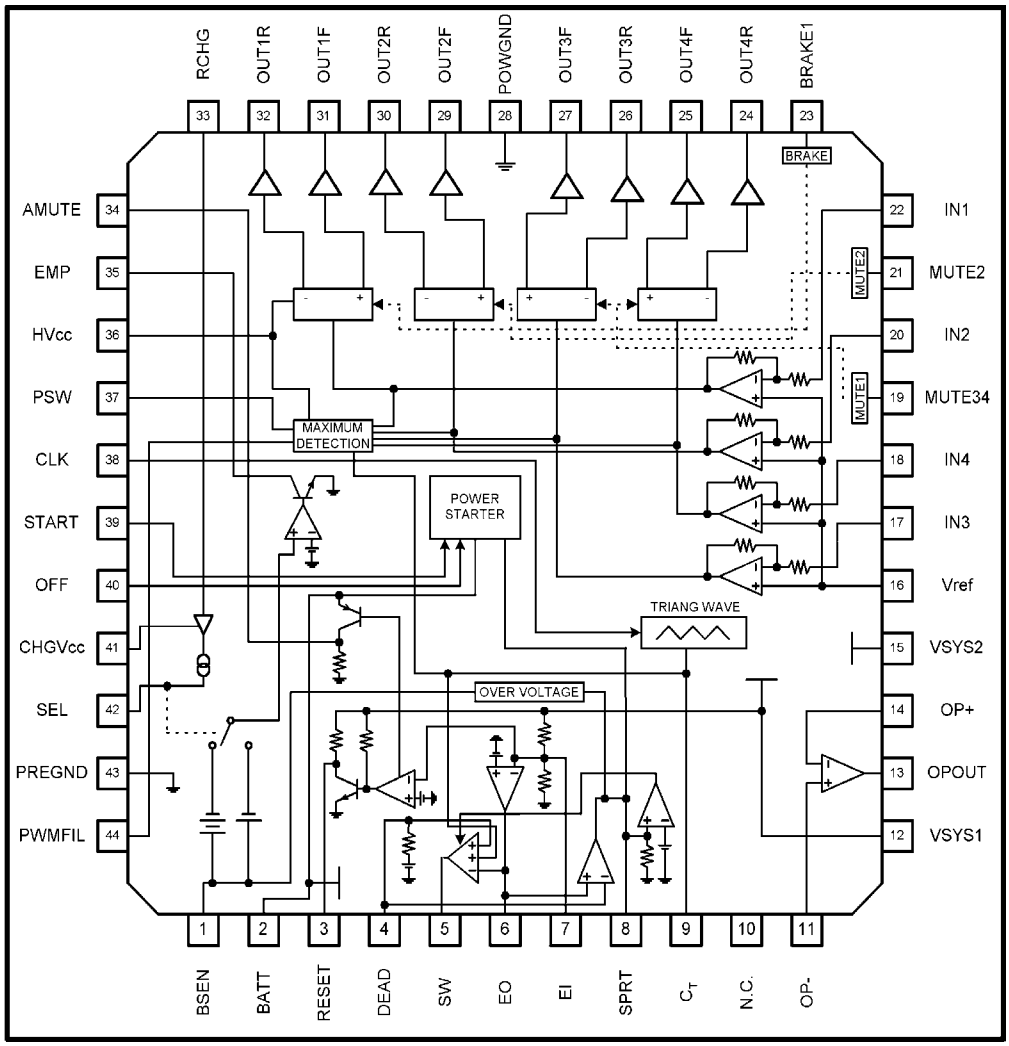
Features

- Built-in 4 channels H-bridge drivers.
- DC/DC converter control circuit on a chip.
- With reset output inversion circuit.
- Battery charging circuit on Chip.
- Built-in thermal shutdown protection.
- QFP44 package.

Applications

- Disc-man
- Other portable compact disc media

Block Diagram



Aimtron reserves the right without notice to change this circuitry and specifications.

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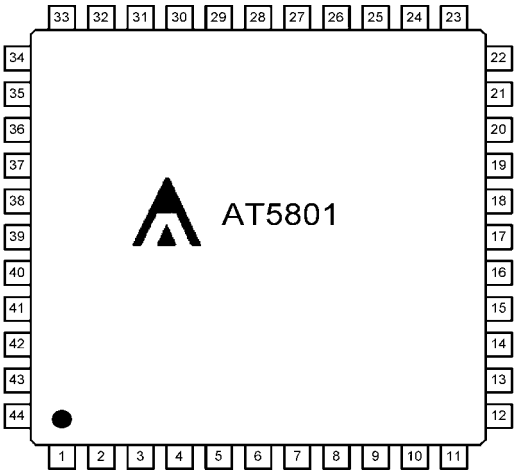
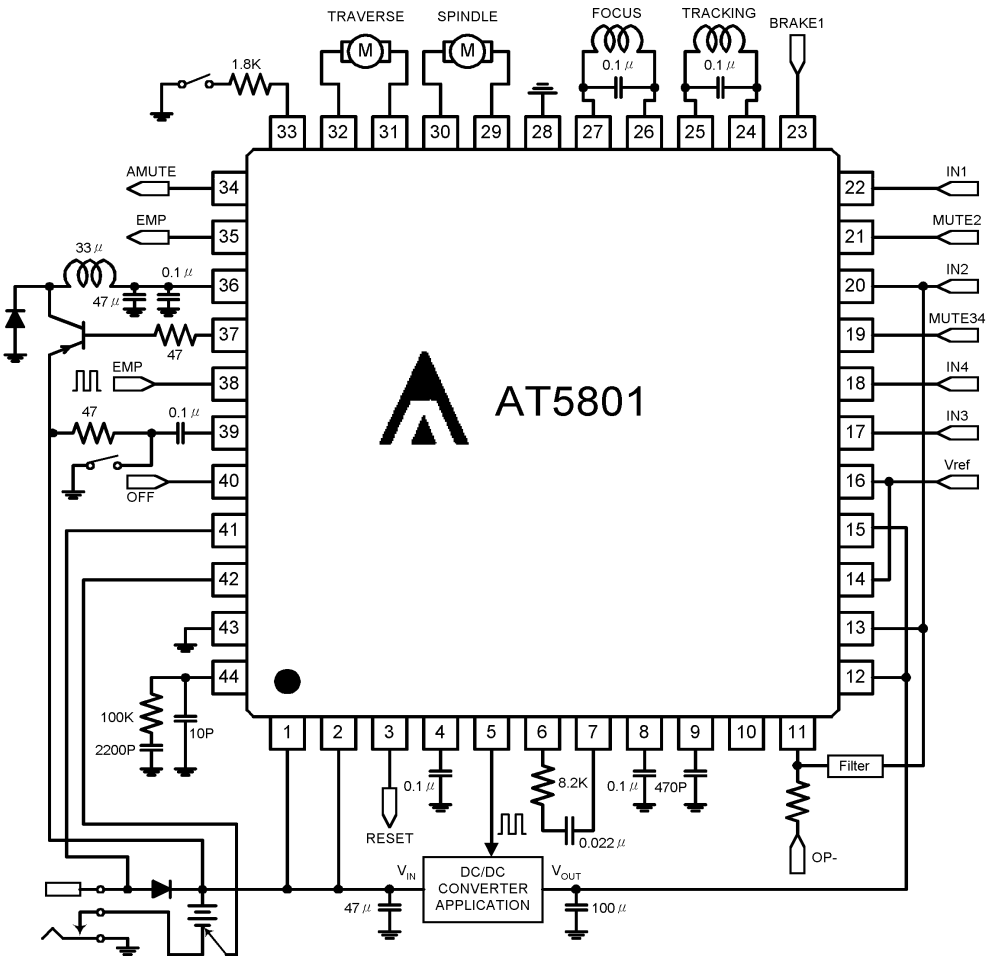
Pin Descriptions

Pin No.	Pin name	Function
1	BSEN	Battery voltage monitor
2	BATTY	Battery power supply input
3	RESET	Reset detection output
4	DEAD	Dead-time setting
5	SW	Booster transistor drive
6	EO	Error amplifier output
7	EI	Error amplifier input
8	SPRT	Short-circuit protection setting
9	CT	Triangular wave output
10	N.C.	
11	Op-	Operational amplifier negative input
12	VSYS1	Control circuit power supply input
13	OPOUT	Operational amplifier output
14	Op+	Operational amplifier positive input
15	VSYS2	Pre-driver power supply input
16	VREF	Reference power supply input
17	IN3	CH3 control signal input
18	IN4	CH4 control signal input
19	MUTE34	CH3/CH4 mute
20	IN2	CH2 control signal input
21	MUTE2	CH2 mute
22	IN1	CH1 control signal input
23	BRAKE1	CH1 brake
24	OUT4R	CH4 negative output
25	OUT4F	CH4 positive output
26	OUT3R	CH3 negative output
27	OUT3F	CH3 positive output
28	POWGND	Power unit power ground
29	OUT2F	CH2 positive output
30	OUT2R	CH2 negative output
31	OUT1F	CH1 positive output
32	OUT1R	CH1 negative output
33	RCHG	Charging current setting
34	AMUTE	Reset inversion output
35	EMP	“Empty” detection output
36	HVCC	H-bridge power supply input
37	PSW	PWM transistor drive
38	CLK	External clock synchronization input
39	START	Boost DC/DC converter starting
40	OFF	Boost DC/DC converter OFF
41	CHGVCC	Charging circuit power supply input
42	SEL	“Empty” detection level switching
43	PREGND	Pre-unit power supply ground
44	PWMFIL	PWM phase compensation

Pin Assignments





Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	unit
Supply voltage	V_{CC*1}	13.5	V
Driver output current	Io	500	mA
Power dissipation	Pd	625*	mW
Operating temperature range	Topr	-30~+85	°C
Storage temperature range	Tstg	-55~+150	°C

∗ Derating is done 5mW/ °C for operation above Ta=25°C.

Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	unit
Control circuit power supply voltage	VSYS1	2.7	3.2	5.5	V
Pre-driver power supply voltage	VSYS2	2.7	3.2	5.5	V
H-bridge power supply voltage	HVCC	-	PWM	BATT	V
Power unit power supply voltage	BATT	1.5	2.4	8.0	V
Charging circuit power supply voltage	CHGVCC	3.0	4.5	8.0	V
Ambient temperature	Ta	-10	25	70	°C

Electrical characteristics

(Unless specified particular, Ta = 25°C, BATT=2.4V, VSYS1= VSYS2=3.2V, VREF=1.6V, CHGVCC=0V, CLK=88.2KHz)

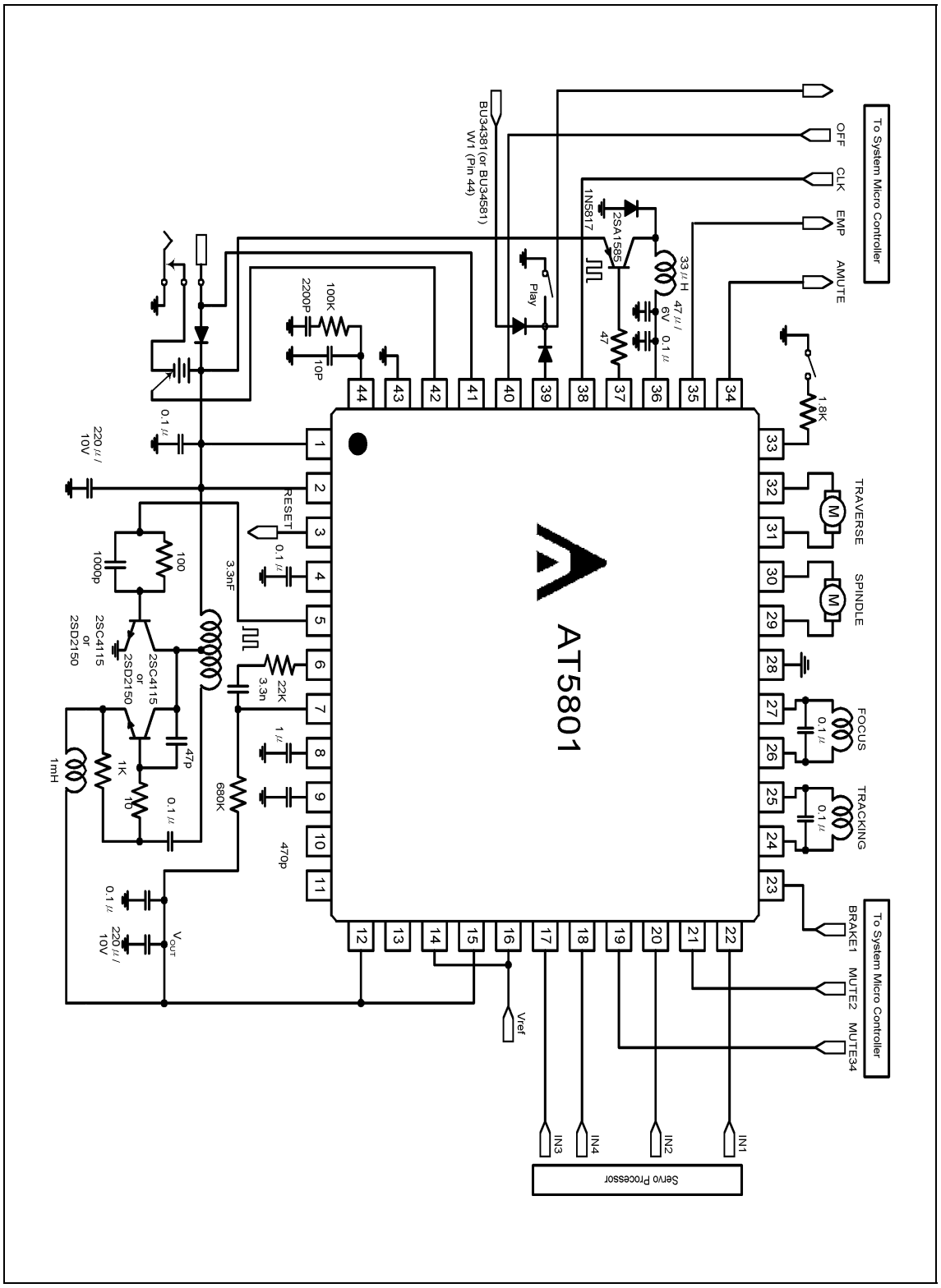
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Common section						
BATT stand-by current	I_{ST}	—	0	3	μA	BATT=9V VSYS1= VSYS2=Vref=0V
BATT supply current at no-load	I_{BAT}	—	2.5	4.0	mA	HVcc=0.45V, MUTE34=3.2V
VSYS1 supply current at no-load	I_{SYS1}	—	4.7	6.4	mA	HVcc=0.45 MUTE34=3.2V, EI=0V
VSYS2 supply current at no-load	I_{SYS2}	—	4.1	5.5	mA	HVcc=0.45V, MUTE34=3.2V
CHGVCC supply current at no-load	I_{CGVCC}	—	0.65	2.0	mA	CHGVcc=4.5V, ROUT=OPEN
H-bridge driver section						
Voltage gain (CH1、3、4)	G_{VC134}	12	14	16	dB	
(CH2)	G_{VC2}	21.5	23.5	24.5	dB	
Gain error by polarity	ΔGvc	−2	0	2	dB	
IN pin (CH1、3、4)	R_{IN134}	9	11	13	kΩ	IN=1.7 and 1.8V
Input resistance (CH2)	R_{IN2}	6	7.5	9	kΩ	
Maximum output voltage	V_{OUT}	1.9	2.1	—	V	RL=8Ω、HVCC=BATT=4V、IN=0~3.2V
Lower transistor saturated voltage	V_{SATL}	—	240	400	mV	I_O=-300mA、IN=0 and 3.2V
Upper transistor saturated voltage	V_{SATU}	—	240	400	mV	I_O=300mA、IN=0 and 3.2V

Input offset voltage	V_{OI}	-8	0	8	mV	
Output (CH1、3、4)	V_{OO134}	-50	0	50	mV	Vref=IN=1.6V
offset voltage (CH2)	V_{OO2}	-130	0	130	mV	
Dead zone	V_{DB}	-10	0	10	mV	
BRAKE1 ON threshold voltage	V_{BRON}	2.0	—	—	V	IN1=1.8V
BRAKE1 OFF threshold voltage	V_{BROFF}	—	—	0.8	V	IN1=1.8V
MUTE2 ON threshold voltage	V_{M2ON}	2.0	—	—	V	IN2=1.8V
MUTE2 OFF threshold voltage	V_{M2OFF}	—	—	0.8	V	IN2=1.8V
MUTE34 ON threshold voltage	V_{M34ON}	—	—	0.8	V	IN3= IN4=1.8V
MUTE2 OFF threshold voltage	V_{M34OFF}	2.0	—	—	V	IN3= IN4=1.8V
VREF ON threshold voltage	$Vref_{ON}$	1.1	—	—	V	IN1=IN2=IN3=IN4=1.8V
VREF OFF threshold voltage	$Vref_{OFF}$	—	—	0.8	V	IN1= IN2=IN3=IN4=1.8V
BRAKE1 brake current	I_{BRAKE1}	4	7	10	mA	BRAKE1 pin The current Difference between “H” and “L”
PWM power supply driving section						
PSW sink current	I_{PSW}	10	13	17	mA	IN1=2.1V
HVCC level shift voltage	V_{SHIF}	0.35	0.45	0.55	V	IN1=1.8V,HVCC－OUT1F
HVCC leak current	I_{HLK}	—	0	5	μA	HVCC=8V VSYS1= VSYS2=BATT=0V
PWM amplifier transfer gain	G_{PWM}	1/60	1/50	1/40	1/kΩ	IN1=1.8V, HVCC=1.2~1.4V
DC/DC converter section						
(Error amplifier section)						
VSYS1 pin threshold voltage	V_{SITH}	3.05	3.20	3.35	V	
EO pin output voltage H	V_{EOH}	1.4	1.6	—	V	EI=0.7V, I_O=－100 μA
EO pin output voltage L	V_{EOL}	—	—	0.3	V	EI=1.3V, I_O=100 μA
(Short-circuit protection)						
SPRT pin voltage(normal)	V_{SPR}	—	0	0.1	V	EI=1.3V
SPRT pin current 1 EO=H	I_{SPR1}	-6	-10	-16	μA	EI=0.7V
SPRT pin current 2 EO=L	I_{SPR2}	-12	-20	-32	μA	EI=1.3V, OFF=0V
SPRT pin current 3 (over-voltage)	I_{SPR3}	-12	-20	-32	μA	EI=1.3V, BATT=9V
SPRT pin impedance	R_{SPR}	175	220	265	kΩ	
SPRT pin threshold voltage	V_{SPTH}	1.10	1.245	1.30	V	EI=0.7V, CT=0V
Over-voltage	V_{OV}	8.0	8.4	9.0	V	BSEN pin voltage

protection detect						
(Transistor driving section)						
SW pin output voltage 1H	V_{SW1H}	0.78	0.98	1.13	V	BATT=C_T=1.5V, I_O=－2mA, VSYS1= VSYS2=0V, at start
SW pin output voltage 2H	V_{SW2H}	1.0	1.50	—	V	C_T=0V, I_O=－10mA, EI=0.7V, SPRT=0V
SW pin output voltage 2L	V_{SW2L}	—	0.3	0.45	V	C_T=2V, I_O=10mA,
SW pin oscillating frequency 1	f_{SW1}	65	80	95	kHz	C_T=470pF, VSYS1= VSYS2=0V, at start
SW pin oscillating frequency 2	f_{SW2}	60	70	82	KHz	C_T=470pF, CLK=0V
SW pin oscillating frequency 3	f_{SW3}	—	88.2	—	KHz	C_T=470pF
SW pin minimum pulse width	T_{SWMIN}	0.01	—	0.6	μsec	C_T=470pF, EO=0.5~0.7V sweep
Pulse duty at start	D_{SW1}	40	50	60	%	C_T=470pF, VSYS1= VSYS2=0V
Max. pulse duty at self-running	D_{SW2}	70	80	90	%	EI=0.7V, C_T=470pF, CLK=0V
Max. pulse duty at CLK synchronization	D_{SW3}	65	75	85	%	EI=0.7V, C_T=470pF
(Dead time section)						
DEAD pin impedance	R_{DEAD}	52	65	78	kΩ	
DEAD pin output voltage	V_{DEAD}	0.78	0.88	0.98	V	
(Interface section)						
OFF pin threshold voltage	V_{OFTH}	—	—	VSYS1 -2.0	V	EI=1.3V
OFF pin bias current	I_{OFF}	-75	-95	-115	μA	OFF=0V
START pin ON threshold voltage	V_{STATH1}	—	—	BATT -1.0	V	VSYS1= VSYS2=0V, C_T=2V
START pin OFF threshold voltage	V_{STATH2}	BATT -0.3	—	—	V	VSYS1= VSYS2=0V, C_T=2V
START pin bias current	I_{START}	-13	-16	-19	μA	START=0V
CLK pin threshold voltage H	V_{CLKTHH}	2.0	—	—	V	
CLK pin threshold voltage L	V_{CLKTHL}	—	—	0.8	V	
CLK pin bias current	I_{CLK}	—	—	10	μA	CLK=3.2V
(Starter circuit section)						
Starter switching voltage	V_{STMM}	2.3	2.5	2.7	V	VSYS1= VSYS2=0V~3.2V, START=0V
Starter switching hysteresis width	V_{SNHS}	130	200	300	mV	START=0V
Discharge release voltage	V_{DIS}	1.63	1.83	2.03	V	
(Empty detection section)						
Empty detection voltage 1	V_{EMPT1}	2.1	2.2	2.3	V	VSEL=0V
Empty detection voltage 2	V_{EMPT2}	1.7	1.8	1.9	V	ISEL=-2 μA
Empty detection	V_{EMHS1}	25	50	100	mV	VSEL=0V

hysteresis width 1						
Empty detection hysteresis width 2	V_{EMHS2}	25	50	100	mV	ISEL=-2 μA
EMP pin output voltage	V_{EMP}	—	—	0.5	V	I_O=1mA, BSEN=1V
EMP pin output leak current	I_{EMPL}	—	—	1.0	μA	BSEN=2.4V
BSEN pin input resistance	R_{BSEN}	17	23	27	kΩ	VSEL=0V
BSEN pin leak current	I_{BSNL}	—	—	1.0	μA	VSYS1=VSYS2=0V, BSEN=4.5V
SEL pin detection voltage	V_{SELTH}	1.5	—	—	V	V_{SELTH}=BATT-SEL, BSEN=2V
SEL pin detection current	I_{SELT}	−2	—	—	μA	
(Reset circuit)						
VSYS1 reset threshold voltage ratio	H_{SRT}	85	90	95	%	Ratio of VSYS1 voltage and error-amp threshold voltage
Reset detection hysteresis width	V_{RSTHS}	25	50	100	mV	
RESET pin output voltage	V_{RST}	—	—	0.5	V	I_O=1mA, VSYS1=VSYS2=2.8V
RESET pin pull up resistance	R_{RST}	72	90	108	kΩ	
AMUTE pin output voltage 1	V_{AMT1}	BATT −0.4	—	BATT	V	I_O=−1mA, VSYS1=VSYS2=2.8V
AMUTE pin output voltage 2	V_{AMT2}	BATT −0.4	—	BATT	V	I_O=−1mA, START=0V VSYS1=VSYS2=2.8V
AMUTE pin pull down resistance	R_{AMT}	77	95	113	kΩ	
(Operational amplifier section)						
Input bias current	I_{BIAS}	—	—	-300	nA	OP+=1.6V
Input offset voltage	V_{OIOP}	−5.5	0	5.5	mV	
High level output voltage	V_{OHOP}	2.8	—	—	V	RL=OPEN
Low level output voltage	V_{OLOP}	—	—	0.2	V	RL=OPEN
Output drive current (source)	I_{SOU}	—	-6.5	-3.0	mA	Output short to GND by 50Ω
Output drive current (sink)	I_{SIN}	0.4	0.7	—	mA	Output short to VSYS by 50Ω
Open loop voltage gain	GVO	—	70	—	dB	VIN=−75dBV,f=1kHz
Slew rate	SR	—	0.5	—	V/μs	
(Charging circuit section)						
RCHG pin bias voltage	V_{RCHG}	0.71	0.81	0.91	V	CHGVcc=4.5V, RCHG=1.8kΩ
RCHG pin output resistance	R_{RCHG}	0.75	0.95	1.20	kΩ	CHGVcc=4.5V, RCHG=0.5 and 0.6V
SEL pin leak current 1	I_{SELLK}	—	—	1.0	μA	CHGVcc=4.5V,RCHG=OPEN
SEL pin leak current 2	I_{SELLK}	—	—	1.0	μA	CHGVcc=0.6V,RCHG=1.8kΩ

Application



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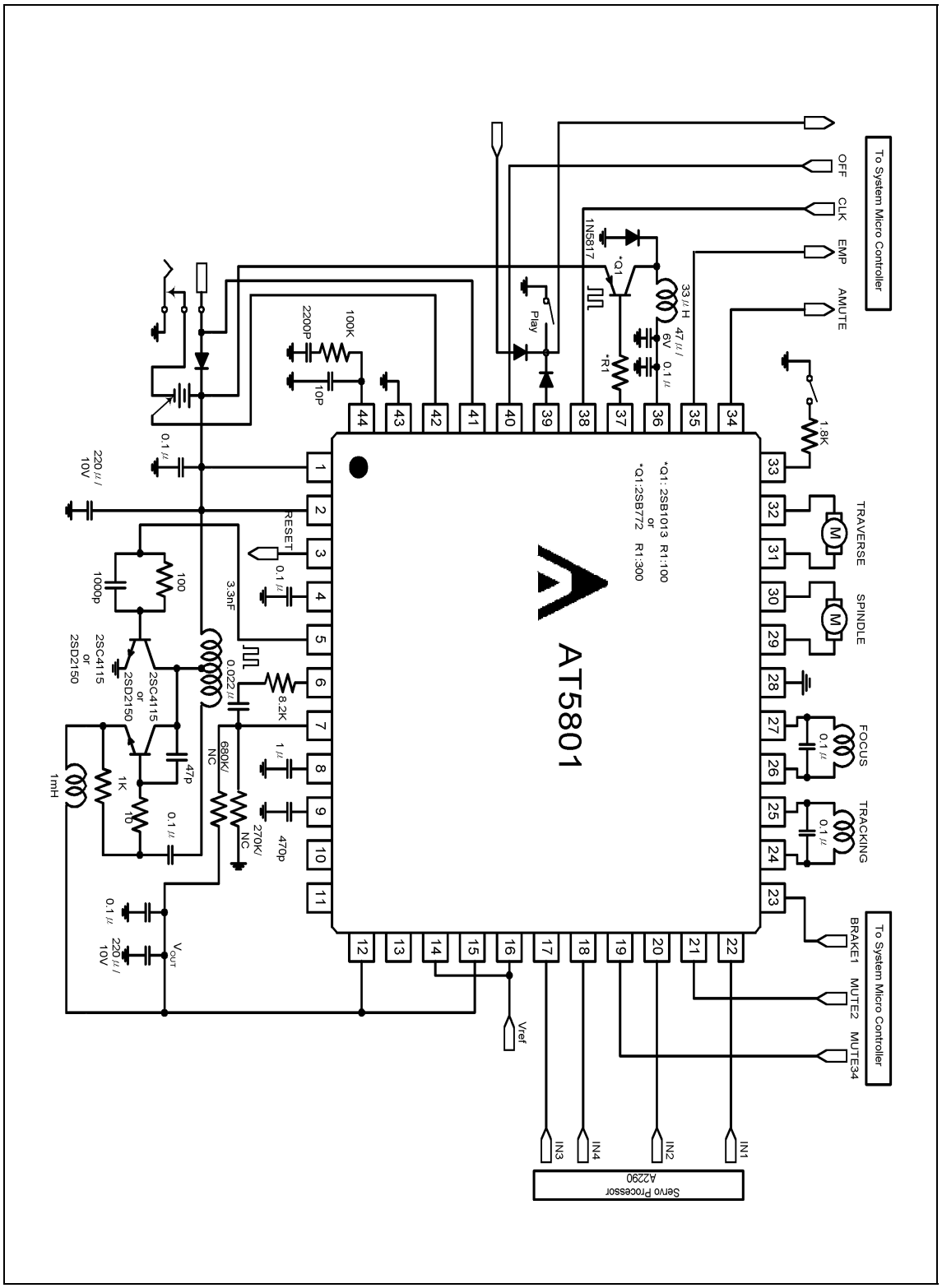
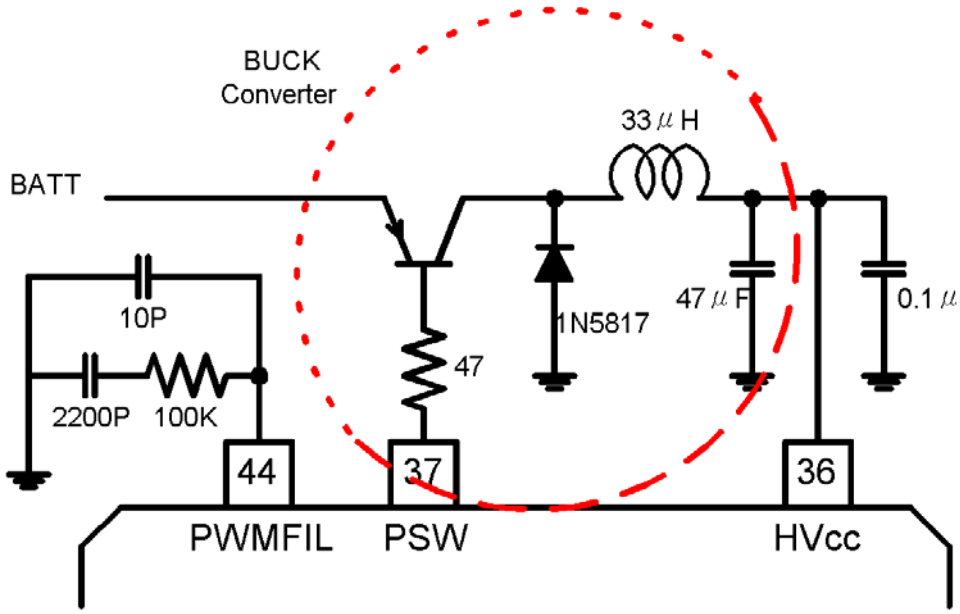


Function Description

1. PWM switching regulated power supply drive

This circuit detects the maximum output level of four channels drivers and then generates PWM signal accordingly. It uses a PNP transistor, a Schottky diode and a capacitor as external components.



2. Empty detector unit

SEL pin	Detect voltage	Return voltage
L	2.2V(typ.)	2.25V(typ.)
High-Z	1.8V(typ.)	1.85V(typ.)

3. Reset circuit

If the output voltage of the DC/DC converter is over than 90% of rating value, RESET terminal varies from “L” to “H”, AMUTE terminal changes from “H” to “L” and Hysteresis is typically 50mV.

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4. Charging circuit

The power supply for the charging unit is applied to the CHGVCC terminal. It is independent of any other circuits. Charging current is set by the resistance between RCHG terminal and GND. A constant charging current flows through SEL terminal.

5. Mute function

The BRAKE pin is low during normal operation (high to set CH1 mute on and enters a brake mode).

- The MUTE2 pin is low during normal operation (high to set CH2 mute on).
- The MUTE34 pin is high during normal operation (low to set CH3,4 mute on).

6. VREF drop mute

Normally when the voltage of VREF terminal is above 1.0V, the mute circuit is disabled and the output circuit is active.

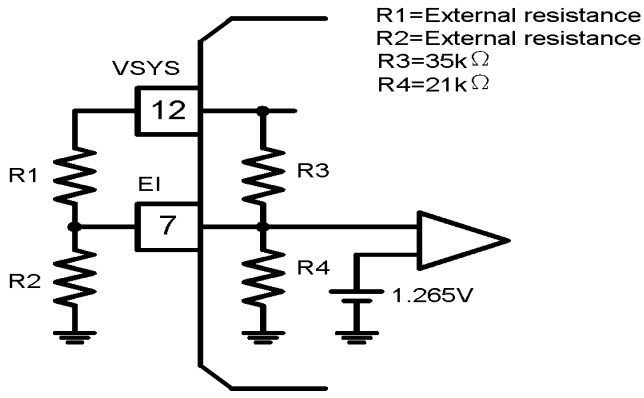
7. Thermal shutdown

If the chip temperature rises above 150℃, then the thermal shutdown (TSD) circuit will be activated and the output current will be mute.

8. Output voltage

The voltage booster circuit of (VSYS1) can be configured with external component as follows.

$$VSYS = 1.265 \times \frac{\frac{R1 \cdot R3}{R1 + R3} + \frac{R2 \cdot R4}{R2 + R4}}{\frac{R2 \cdot R4}{R2 + R4}} \quad (V)$$



9. Driver gain

Driver input resistance is 10KΩ for CH1, CH3, CH4 and input resistance of CH2 is 7.5KΩ. Driver gain can be set by using an external resistor and applying the following equations.

$$\text{CH1,3,4} \quad Gv = 20\log\left|\frac{55k}{11k+R}\right|$$

$$\text{CH2} \quad Gv = 20\log\left|\frac{110k}{7.5k+R}\right|$$

R is External resistance

10. Short-circuit protection function

When the output of error amplifier is "H", if the voltage of SPRT terminal has reached 1.265V upon charging the terminal, switching of SW terminal will be disabled. Switching off time depends on the value of the capacitor at SCP:

$$t = CSPRT \times \frac{VTH}{ISPRT}(\text{sec})$$
$$(VTH = 1.265V, ISPRT = 5\mu A)$$

11. Soft-start function and maximum duty

Maximum duty can be changed by attaching a resistor to pin 4.

$$t = CDEAD \times R(\text{sec})$$
$$(R = 65K\Omega)$$

12. Power-off operation

SPRT terminal is charged by setting OFF terminal to "L".Typically, the switching of SW terminal will be terminated when the voltage at the SPRT terminal reaches 1.265V.

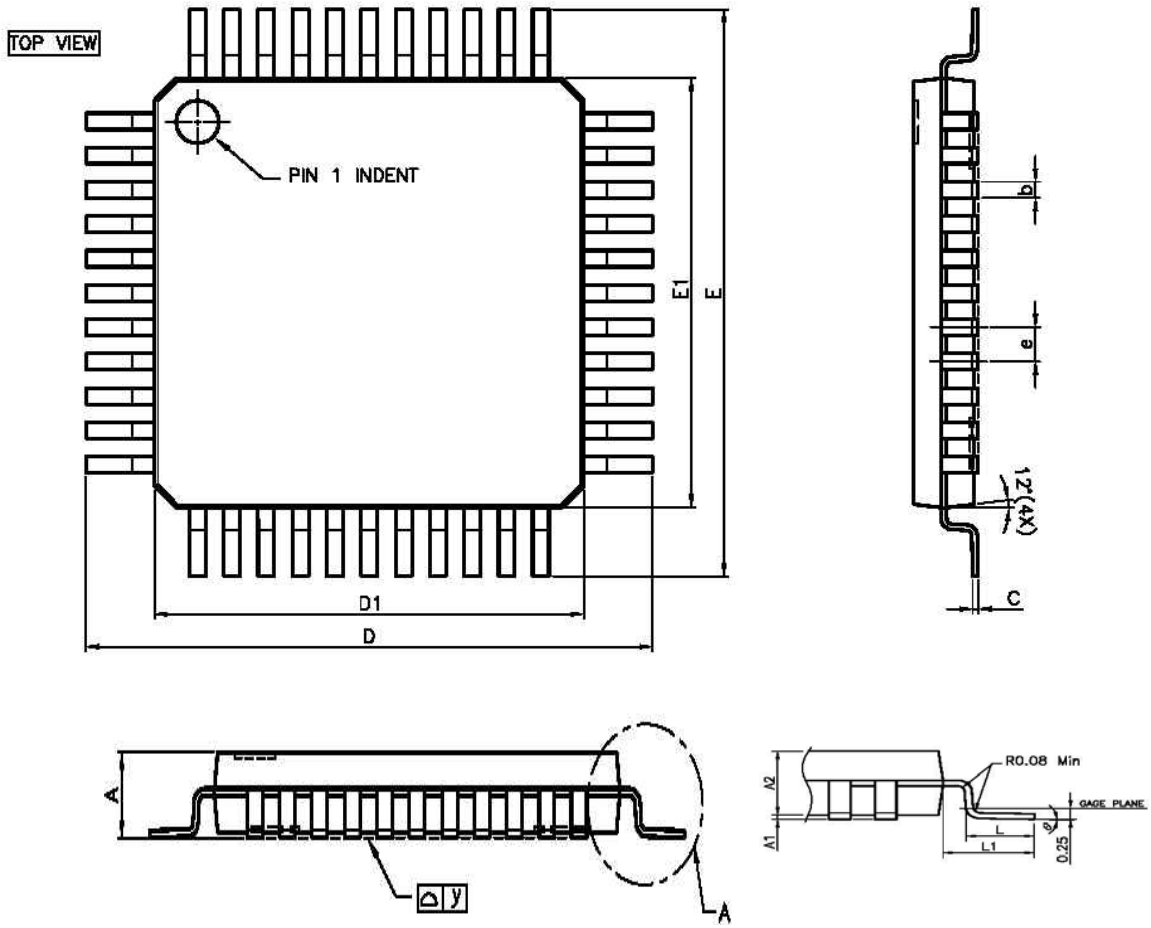
$$t = CSPRT \times \frac{VTH}{IOFF}(\text{sec})$$
$$(VTH = 1.265V, IOFF = 20\mu A)$$

13. Over-voltage protection operation

When the voltage at BSEN terminal has risen above 8.4V, the SPRT terminal will be charged. But the switching of SW terminal will be terminated when the voltage at the SPRT terminal has reached 1.265V.

$$t = CSPRT \times \frac{VTH}{IHV}(\text{sec})$$
$$(VTH = 1.265V, IHV = 20\mu A)$$

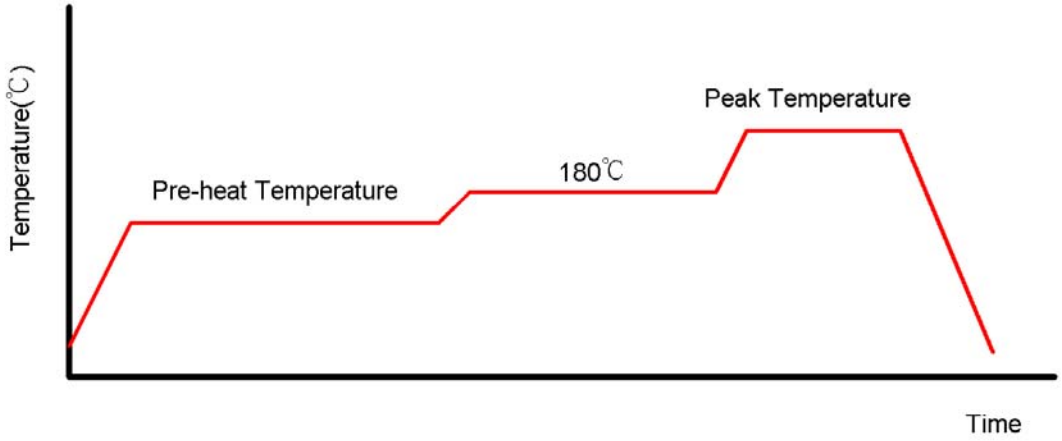
Package Outlines (units:mm): QFP-44



SYMBOL	MILLIMETERS		
	MIN.	TYP.	MAX.
A	-	-	1.70
A1	0.10	-	0.25
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
C	0.09	-	0.20
E	13.00	13.20	13.40
E1	9.90	10.00	10.10
D	13.00	13.20	13.40
D1	9.90	10.00	10.10
e	-	0.80	-
L	1.05	1.20	1.35
L1	-	1.60	-
θ	0°	3.5°	7°
y	0.0	-	0.08

Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A



Classification Reflow Profiles

	Convection or IR/Convction	VPR
Average Heating Rate(180℃ to peak)	5°C/second max.	10°C/second max.
Preheat Temperature(125±20℃)	120 seconds max.	
Temperature maintained above 180℃	10~150 seconds	
Time within 5℃ of actual Peak Temperature	10~20 seconds	60 seconds
Peak Temperature Range(Note 1)	219~225°C or 235~240°C	219~225°C or 235~240°C
Cooling Rate	6°C /second max.	10°C/second max.
Time 25℃ to Peak Temperature	6 minutes max.	

*1 The maximum peak temperatures for IR and VP reflow are depending on package dimensions.

Package Reflow Conditions

Pkg. Thickness ≥2.5mm and all bags	Pkg. Thickness <2.5mm and Pkg. Volume ≥350 mm^3	Pkg. Thickness <2.5mm and Pkg. Volume <350 mm^3
Convection 219~225℃		Convection 235~240℃
VPR 219~225℃		VPR 235~240℃
IR/Convection 219~225℃		IR/Convection 235~240℃