AT3210

16 Gray scales 160X160 STN LCD Controller

REV 1.11

February 2002

Aimtron reserves the right without notice to change this circuitry and specifications.

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Revision History

Revision 1.11 (February 1,2002)

. Modify FIRSTL register address from 2DH to 1DH

. Modify some description of the frame rate and mod rate

Revision 1.1 (January 29,2002)

. Change pin numbers

. Modify current consumption spec.

Revision 1.0 (January 22,2002)

. Add revision information

. Modify the sequence the D1,D0 of the DFORMT register

. Changes of the Aimtron address information

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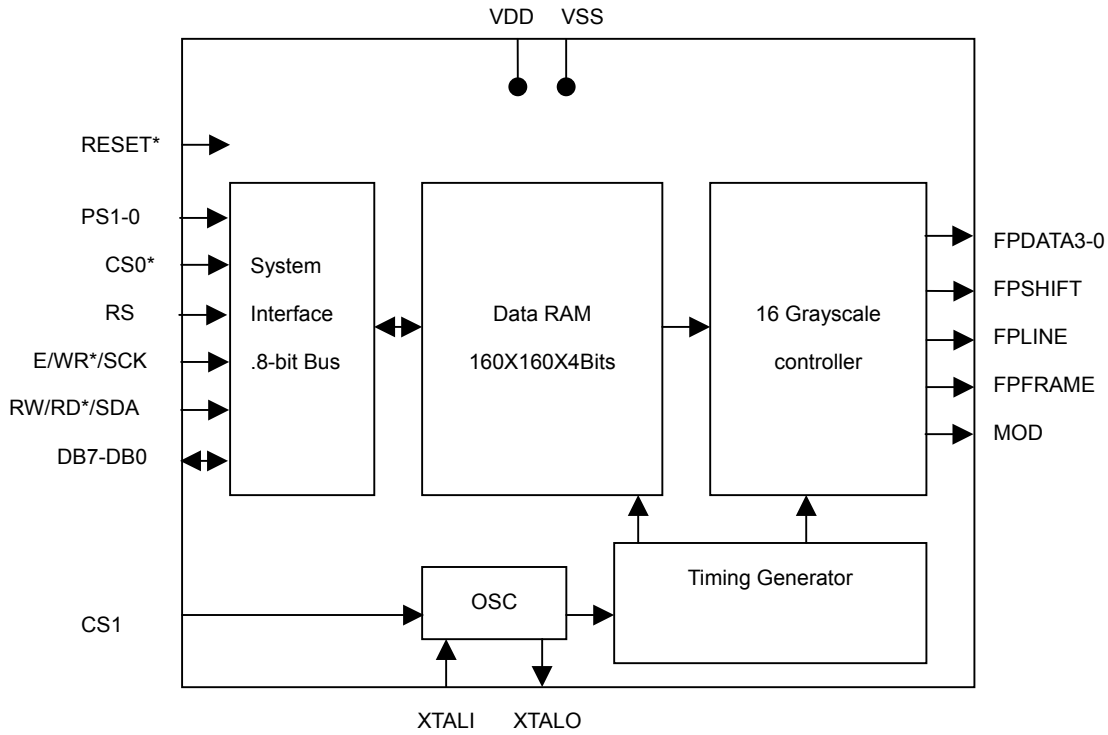
General Description

The AT3210 is a dot matrix graphics STN LCD controller LSI that can be connected directly to the microprocessor. It can support up to 160X160/16 grayscales for B/W and color STN module with drivers. The AT3210 displays the data directly from the internal 160X160X4 graphic RAM. The microprocessor interface is 6800/8080-series compatible 8-bit interface or 4-wire serial interface.

Features

. Supports up to 160X160 / 16 grayscales graphic display
. Directly interface to 4-bit interface LCD driver
. Hardware pin selectable for 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, or 4-wire Serial Peripheral Interface
. Programmable gamma table
. Auto increasement of the RAM address inside the display window
. Single supply operation VDD=3.3V
. 28 Pin SSOP package

Functional Block Diagram



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System Block Diagram

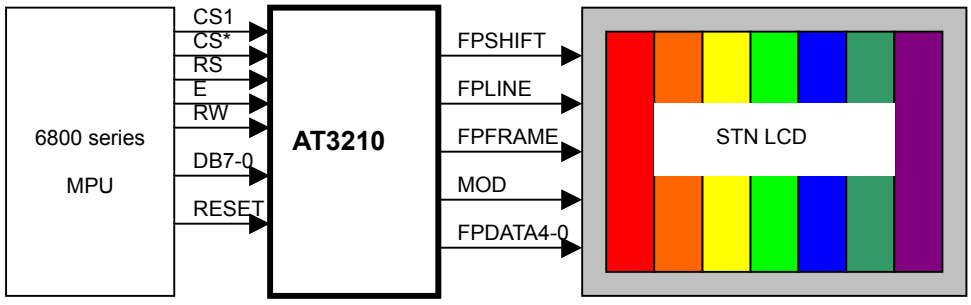

Fig 1. 6800 series MPU interface application

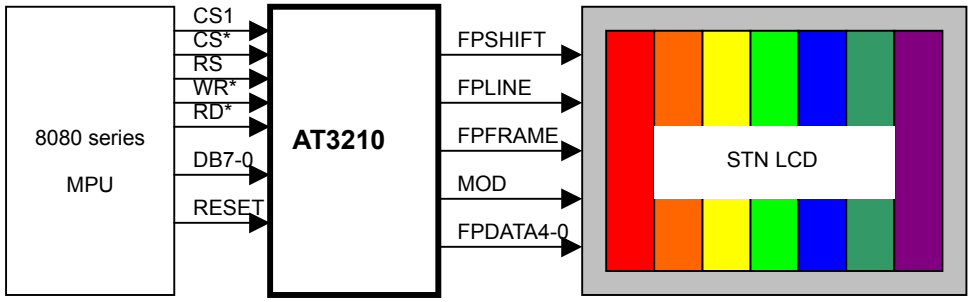

Fig 2. 8080 series MPU interface application

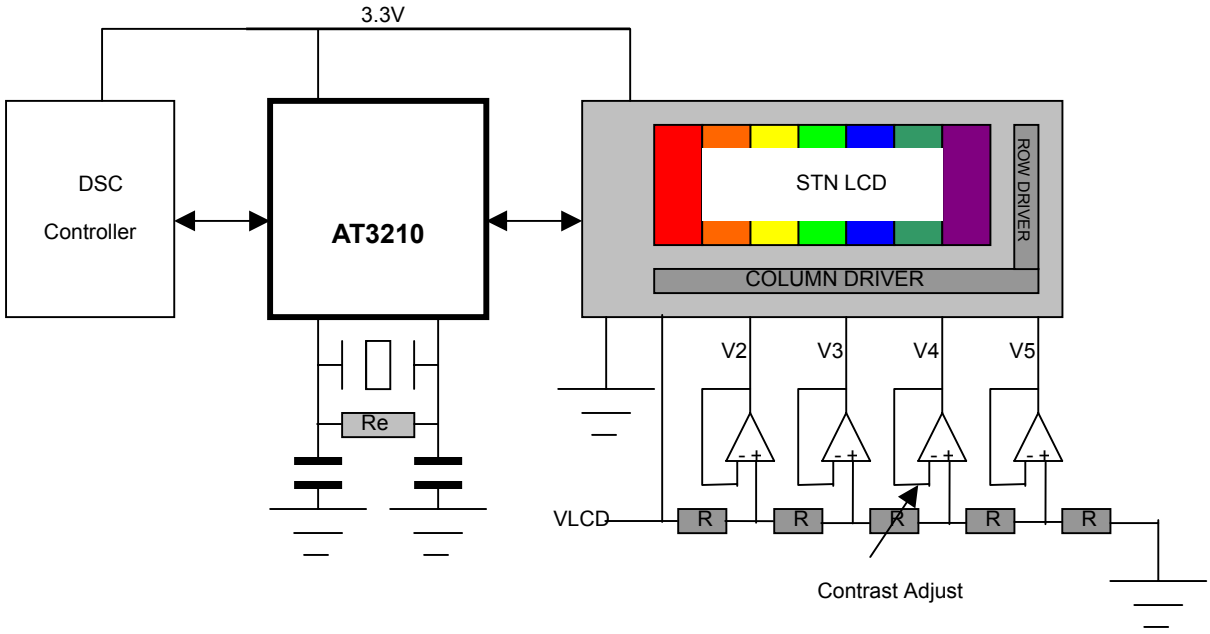

Fig 3. DSC system reference design

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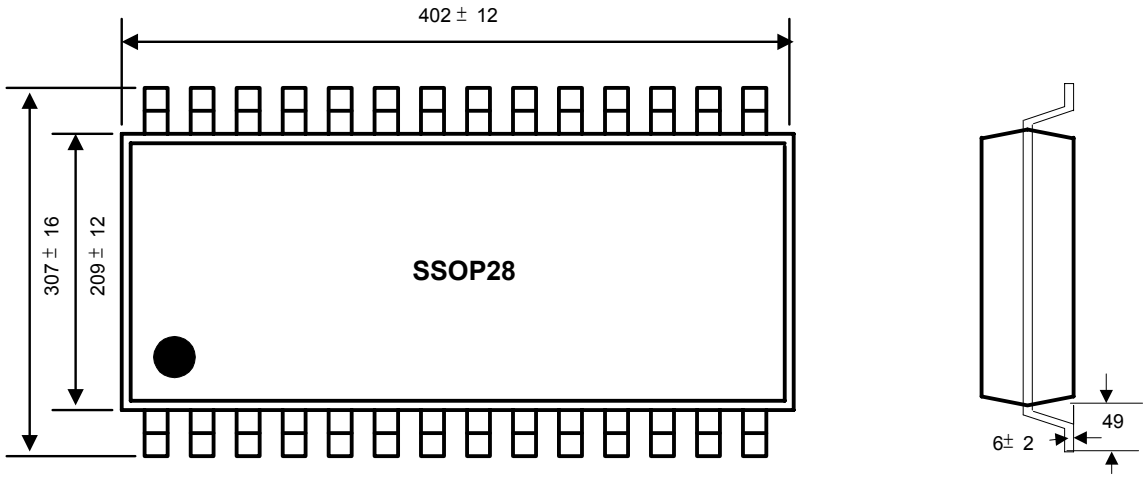
Pin Description

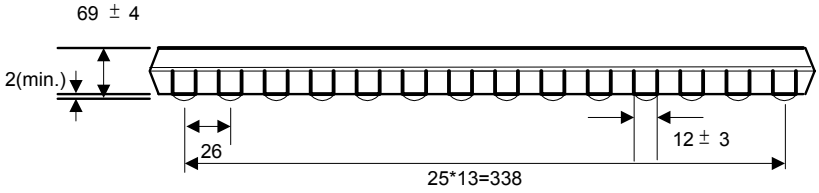
Pin Name	Pin Number	I/O	Pin Description
RESET*	19	Input	Reset: logical '0'.
CS1	18	Input	Chip select. logical '0' disable the crystal oscillator. logical '1' enable the crystal oscillator.
PS1,PS0	20, 21	Input	Select MPU interface. PS1 PS0 Mode '00' : Reserved '01' : 4-wire serial interface '10' : 8080 8-bit mode '11' : 6800 8-bit mode
CS0*	22	Input	Chipselect : logical '0' enable the MPU interface.
RS	23	Input	Select register. Logical '0': control index & data. Logical '1': image data.
E/WR*/SCK	24	Input	For a 68-system bus interface, serves as an enable signal to activate data read/write operation. For an 80-system bus interface, serves as a write strobe signal and writes data at the low level For the serial interface,serves as a clock signal
RW/RD*/SDA	25	Input	For a 68-system bus interface, serves as a signal to select data read/write operation. Low: Write High: Read. For an 80-system bus interface, serves as a read strobe signal and reads data at the low level. For the serial interface,serves as a data signal.
DB7-DB0	26,27,28,29, 1,2,3,4,5	Bidirection	Serves as a 8-bit bidirectional data bus. Fix unused DB7-DB0 to the VDD or VSS level.
FPDATA3-FPDATA0	9,8,7,6	Output	LCD 4-bit data.
FPSHIFT	10	Output	LCD horizontal shift clock.
FPLINE	12	Output	LCD line pulse.
FPFRAME	13	Output	LCD frame pulse.
MOD	11	Output	LCD AC input.
XTALI	16	Input	Oscillator input/clock input.
XTALO	17	Output	Oscillator Output.
VDD	14	Power	3.3V Power supply.
VSS	15	Ground	Ground pin.

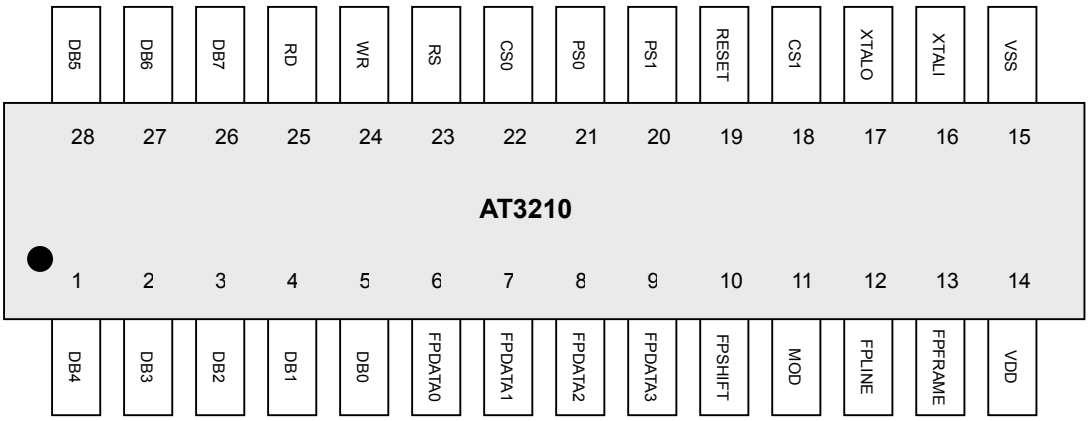
* All unused input pins must be tied to VDD or VSS

Package



Dimension in MIL





Functional Description

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MPU interface

The chip identifies the data bus signals by a combination of RS, RD(E), WR(RW) signals. The Interpretation and execution of command depends on the external clock.

In the 8080 MPU interface, commands are launched by inputting a low pulse to the RD terminal for reading, and inputting a low pulse to the WR terminal for writing. In the 6800 series MPU interface, the interface is placed in a read mode when an 'H' signal is input to the RW terminal and placed in a write mode when a 'L' signal is input to the R/W terminal and then the command is launched by inputting a high pulse to the E terminal. (See the timming diagram regarding the timing.) When the serial interface is selected, the data is input in sequence starting with D7.

The MPU data bus is used as the display data input when the RS pin is '1'. The interpretation of the data format depends on the DFORMAT command. If DFORMAT=0, the high nibble is the first pixel and the low nibble is the second pixel. If DFORMAT=1, the high nibble is the second pixel and the low nibble is the first pixel. If DFORMAT=2, the high nibble is the current pixel data and the low nibble is don't care. If DFORMAT=3, the low nibble is the current pixel data and the high nibble is don't care. Each MPU write cycle latches 2 pixel data when DFORMAT=0 or 1and 1 pixel data when DFORMAT=2 or 3. See Fig.6 and Fig. 7. The internal RAM will write these data only after 32 bits data is latched

The write pulses of the MPU must be the multiples of 4 or 8 which depends on the DFORMAT. The read pulses of the MPU must be the multiples of 4 which is independant of the DFORMAT. If you want to read data from memory, one dummy read cycle must be asserted before the wanted data output. The first read/write data is determined by the internal row and column counter. See Fig. 8.

The input/output direction of the MPU data bus is determined by the read/write operation. The data bus is at input state when the AT3210 detects a write operation. The data bus is at output state when the AT3210 detects a read operation. See Fig. 14. Note that the output state after a read operation will hold until the next write operation is detected.

Gamma look-up table

Each pixel data is represented by 4-bit and the maximum gray scales can be shown at the same time is 16. The AT3210 has a 4-bit to 5-bit look-up table. User can select the desired 16 gray scales from the available 32 gray scales when the GAMMA32 command is set to '1'. If the GAMMA32 command is set to 0, there are only 16 gray scales can be selected. See Fig. 4.

Each display data is modulated by 32 frames when GAMMA32=1. If GAMMA32=0, there is only 16 frames per picture.

Fig.4 Gamma look-up table

Panel size and window size

Fig.5 is the illustration of the panel size and the display window. The maximum width and height of the panel size are both limited to 160. The display window is also adjustable by setting the (XWS,YWS) and ending (XWE,YWE). The column number indicated by the XWS or the XWE is (XWS*8) or (XWE*8). The panel size indicated by the XP is (XP*8). The XWS and XWE must be smaller than the XP and the YWS and YWE must be smaller than YP. The internal column counter will automatically increase between the XWS and XWE. The internal row counter will automatically increase between the YWS and YWE. Any write operation outside the window will not be displayed and overlaid by the background color.

Address counter

There are two address counters, row and column counter. The column and row counter will automatically increase according to the window setting during successive read/wrire of display memory (RS pin='1') if the ACINC command is set to '1'. User can directly write to the counters by the COLADR and ROWADR command. *These counters will be update when the value of the COLADR or ROWADR is different from the internal value.*

The width of the data bus of the internal data ram is 32 bits. The display data will be written

into the memory after the 32 bits data is full. After the 32 bit data is written, the column counter is automatically increased by 1 if the ACINC is set to '1'. If DFORMAT is set as 0 or 1, the memory write operation will be executed after four successive MPU write cycles. If the DFORMAT is set as 2 or 3, the memory write operation will be executed after eight successive MPU write cycles. See Figure 6 and Figure 7..

Display mode

There are two display modes : reverse and off. The display data will be reversed when DISPREV=1. The display data will be set to (15-BKCOLOR) when DISPOFF=1 and DISPREV=0. The display data will be set to BKCOLOR when DISPOFF=1 and DISPREV=1.

Frame rate and MOD rate

Each display data is modulated by 32 frames when GAMMA32=1. If GAMMA32=0, there is only 16 frames per picture. Frame rate can be adjusted by setting CLINE0—CLINE2. Lower frame rate consumes lower power. The display is likely to flick at low frame rate. Setting MODRATE register changes the MOD rate. The MODRATE is ideally the same value as the YP.

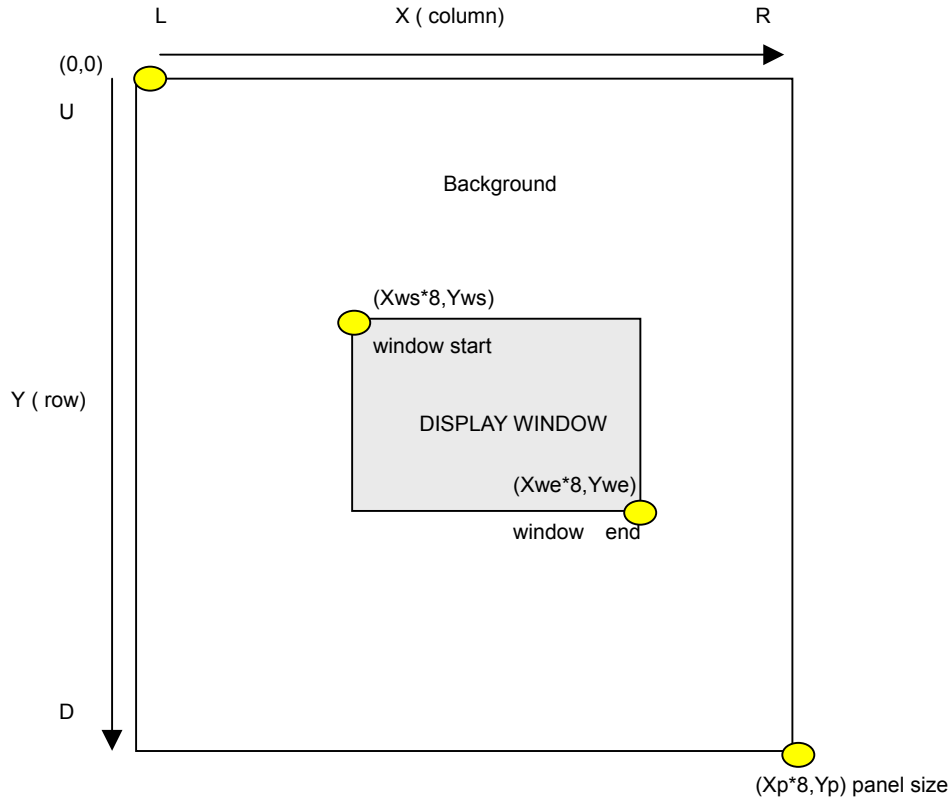

Fig. 5 Panel size and display window

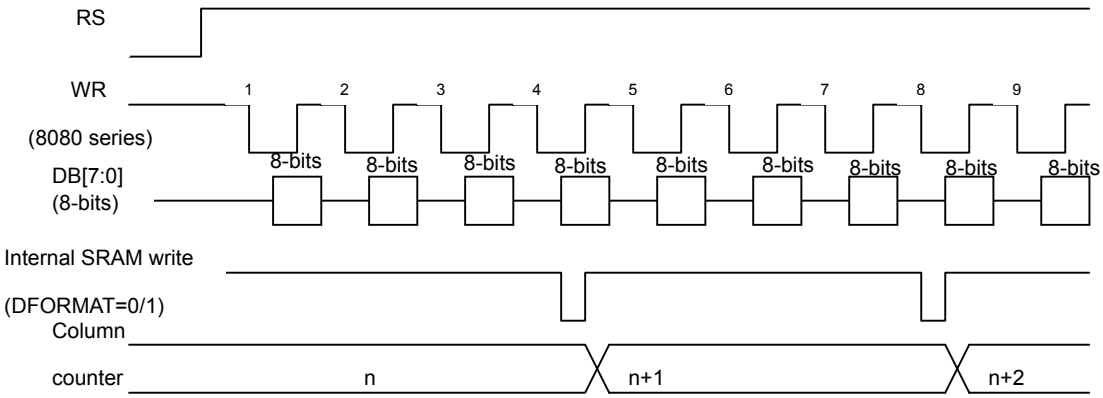

Fig. 6 Illustration of the MPU and internal SRAM write cycle (DFORMAT=0/1)

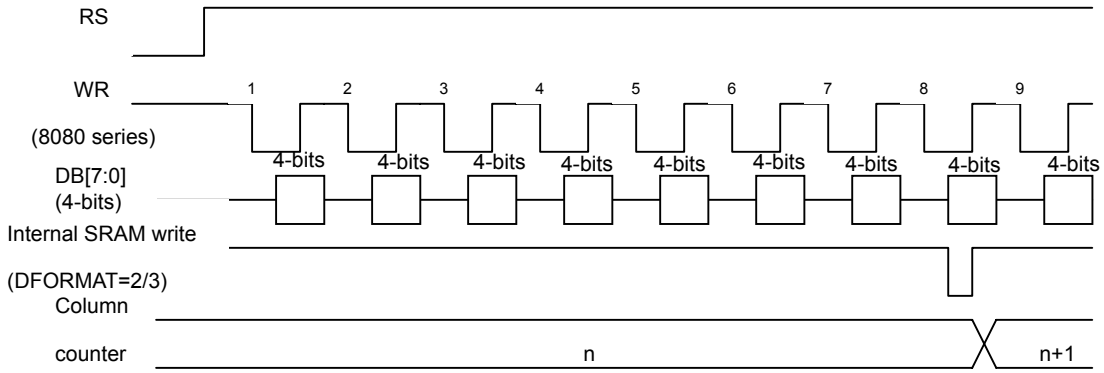

Fig. 7 Illustration of the MPU and internal SRAM write cycle (DFORMAT=2/3)

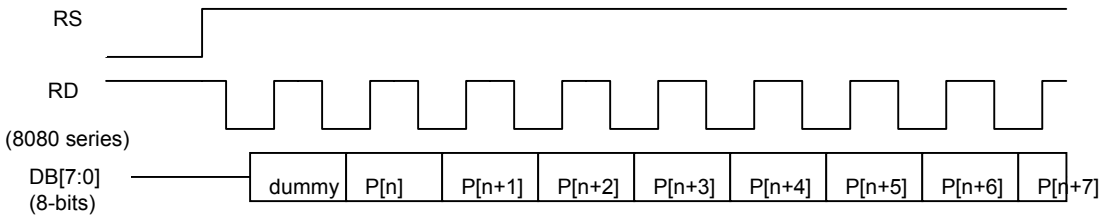

Fig. 8 Illustration of the dummy read cycle during read internal SRAM

(Note: n is determined by the internal column counter and row counter)

Command Descriptions

Double Byte Command (8080-series interface)

***First byte command is the index of command register. Second byte command is the value of command register**

Command	Command code (See Note 3)									Function
	RS	RD	WR	D7	D6	D5	D4	D3	D2	D1 D0
Display data write	1	1	0	d7	d6	d5	d4	d3	d2	d1 d0	Write display data into SRAM (One byte command). The write pulse of the MPU must be the multiples of 4 or 8 is dependant on the DFORMAT. (See Note 5)
Display data read	1	0	1	d7	d6	d5	d4	d3	d2	d1 d0	Read display data from SRAM (One byte command). The read pulse of the MPU must be the multiples is independant on the DFORMAT. (See Note 5)
LUT	0 0	1 1	0 0	0 0	0 0	0 0	0 d4	a3 d3	a2 d2	a1 a0 d1 d0	Set gamma table. Address(a3—a0) is from 0 to 15. Data(d4—d0) is from 0 to 31. (See Note 2)
XWS	0 0	1 1	0 0	0 0	0 0	0 0	1 d4	0 d3	0 d2	0 d1 d0	Window start column address = XWS * 8.
YWS	0 0	1 1	0 0	0 d7	0 d6	0 d5	1 d4	0 d3	0 d2	1 d1 d0	Window start row address. Range is from 0 to 159.
XWE	0 0	1 1	0 0	0 0	0 0	0 0	1 d4	0 d3	0 d2	1 d1 d0	Window end column address = XWE*8.
YWE	0 0	1 1	0 0	0 d7	0 d6	0 d5	1 d4	0 d3	0 d2	1 d1 d0	Window end row address. Range is from 0 to 159.
XP	0 0	1 1	0 0	0 0	0 0	0 0	1 d4	0 d3	1 d2	0 d1 d0	Panel column size= XP *8. The minmum value of the XP is 3.
YP	0 0	1 1	0 0	0 d7	0 d6	0 d5	1 d4	0 d3	1 d2	0 d1 d0	Panel row size.
ADC	0 0	1 1	0 0	0 0	0 0	0 0	1 0	1 0	1 0	1 1/0	Segment direction. (See Note 5) 0: L→R 1: R→L
DISPREV	0 0	1 1	0 0	0 0	0 0	0 0	1 0	1 0	0 0	0 1/0	Display mode. 0:normal 1:reverse
DISPOFF	0 0	1 1	0 0	0 0	0 0	0 0	1 0	1 0	0 0	1 1/0	Display mode. 0:normal 1: off
SRESET	0 0	1 1	0 0	0 0	0 0	0 0	1 0	1 0	0 0	0 1/0	Set 0 then reset. (Note 1) After reset, all registers return to their default value.
COMDIR	0 0	1 1	0 0	0 0	0 0	0 0	1 0	1 0	1 0	1 1/0	Row direction. 0: U→D 1: D→U
TEST	0 0	1 1	0 0	0 0	0 0	0 0	1 0	1 0	0 d1	0 d0	Test mode. Set to 0 for normal operation.
FIRSTL	0	1	0	0 d7	0 d6	0 d5	1 d4	1 d3	1 d2	0 d1	1 d0	First line address.
CLINE0	0 0	1 1	0 0	0 d7	0 d6	0 d5	1 d4	1 d3	1 d2	1 d1	1 d0	Frame rate=Fosc / (CLINE * (YP+1)) Cline must be greater than 4*XP+12. (Note 4)
CLINE1	0 0	1 1	0 0	0 d15	0 d14	1 d13	0 d12	0 d11	0 d10	0 d9	0 d8	
CLINE2	0 0	1 1	0 0	0 0	0 0	1 0	0 0	0 0	0 0	1 d16	
BKCOLOR	0 0	1 1	0 0	0 0	0 0	1 0	0 d3	0 d2	1 d1	0 d0	Background color.

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DFORMAT	0 1 0 0 1 0	0 0 1 0 0 0 1 1 0 0 0 0 0 0 d1 d0	The pixel sequence of the 8-bit MPU data bus. (See Note 5) D1 D0 DB7--DB4 DB3--DB0 0 0 P0 P1 0 1 P1 P0 1 0 P0 X 1 1 x P0
FPDIR	0 1 0 0 1 0	0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 1/0	FPDATA direction. (See Note 5) MSB LSB '0' : D3 D2 D1 D0 '1' : D0 D1 D2 D3
GAMMA32	0 1 0	0 0 1 0 0 1 0 1 0 0 0 0 0 0 0 1/0	The maxinum gray scales that LCD can be shown. '0: 16 gray scales. The gamma value written to the gamma table will be from 0 to 15. '1': 32 gray scales. The gamma value written to the gamma table will be from 0 to 31.
ACINC	0 1 0	0 0 1 0 0 1 1 0 0 0 0 0 0 0 0 1/0	'0'→ internal address counter is fixed when seccessive read/write data memory '1'→ internal address counter automatically increases when seccessive read/write data memory
COLADR	0 1 0	0 0 1 0 0 1 1 1 0 0 0 d4 d3 d2 d1 d0	Column address counter This value is written into the internal column counter when the COLADR or ROWADR is different from their old value.
ROWADR	0 1 0	0 0 1 0 1 0 0 0 d7 d6 d5 d4 d3 d2 d1 d0	Row address counter This value is written into the internal row counter when the COLADR or ROWADR is different from their old value.
MODRATE	0 1 0 0 1 0	0 0 1 0 1 0 1 0 d7 d6 d5 d4 d3 d2 d1 d0	(MODRATE + 1) is the number of FPLINEs between toggles of the MOD output signal.

Note:

1. When software/hardware reset command is set,the register values return to their default value, but the contents of the SRAM do not change.

2. Default value of gamma LUT

GAMA[0]	0	GAMA[8]	8	GAMA[4]	12	GAMA[12]	19
GAMA[1]	2	GAMA[9]	9	GAMA[5]	13	GAMA[13]	23
GAMA[2]	4	GAMA[10]	10	GAMA[6]	14	GAMA[14]	27
GAMA[3]	6	GAMA[11]	11	GAMA[7]	15	GAMA[15]	31

3. Register default values(after software and hardware reset)

XWS	0	DISPREV	0	CLINE1	1	ACINC	1
YWS	0	DISPOFF	0	CLINE2	0	COLADR	0
XWE	19	SRESET	1	CLINE2	0	ROWADR	0
YWE	159	COMDIR	0	BKCOLOR	0	MODRATE	159
XP	19	TEST	0	DFORMAT	1		
YP	159	FIRSTL	0	GAMMA32	1		
ADC	0	CLINE0	95	FPDIR	0		

4. The defaul LCD frame rate=27000000(Hz)/(159+1)(351) ~= 480 . Each picture needs 32 LCD frames(GAMMA32) for 16 grey levels display. The refresh rate of the image is 480/32=15 images/per second.

5. The order of the pixels displayed on the LCD depends on the setting of the ADC and FPDIR . See the following Table. The order of the input data from the MPU data bus follows the setting of the DFORMAT. If DFORMAT=0/1, two pixels is launched at each MPU write operation. If DFORMAT=2/3, only one pixel is launched at each MPU write operation.

		COLUMN No.								
ADC	FPDIR	0	1	2	3	.....	156	157	158	159
0	0	P0	P1	P2	P3	.....	P156	P157	P158	P159
0	1	P3	P2	P1	P0	.....	P159	P158	P157	P156
1	0	P159	P158	P157	P156	.....	P3	P2	P1	P0
1	1	P156	P157	P158	P159	.....	P0	P1	P2	P3

Timing Diagram

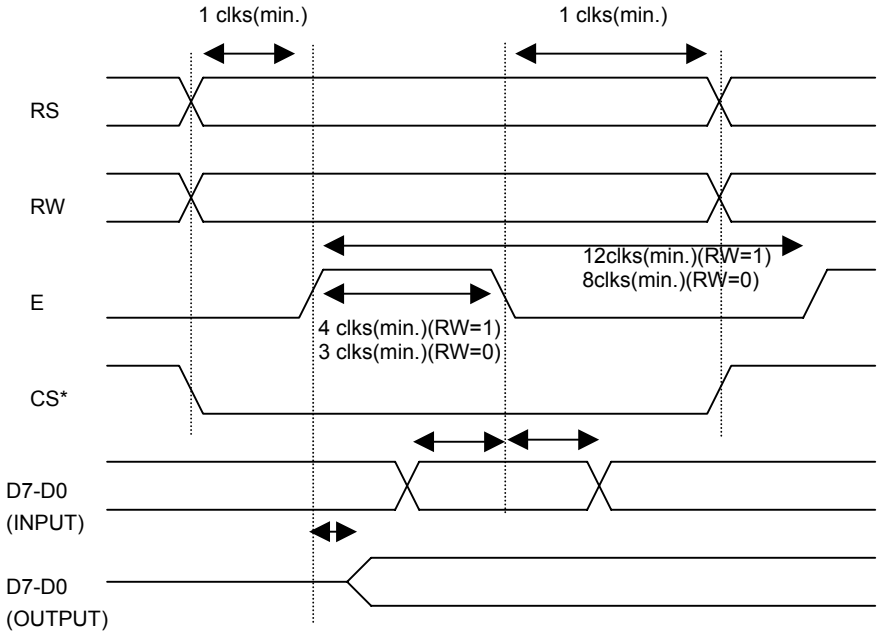

Fig.9 **Parallel 6800 series interface timing diagram**

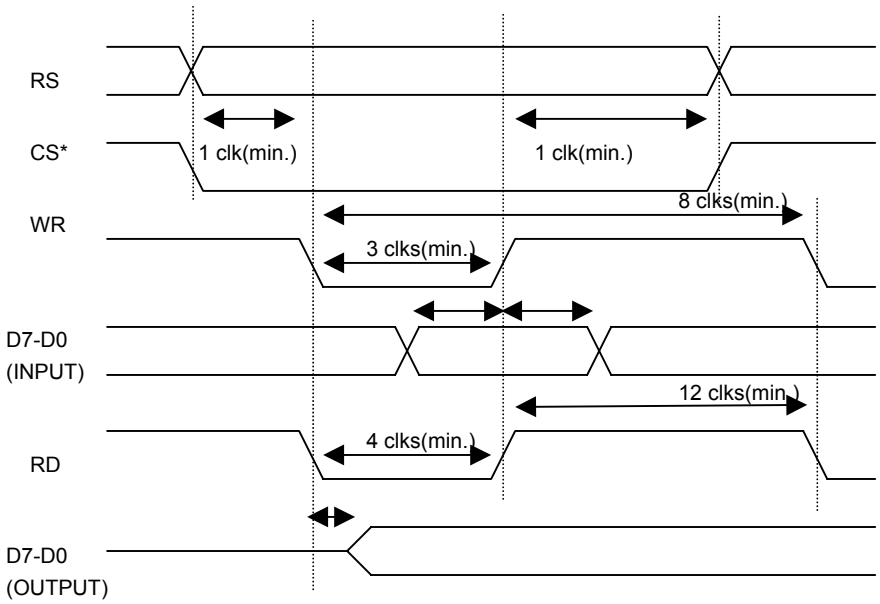

Fig.10_1 Parallel 8080 series interface timing diagram

(RS=0/ RS=1,DFORMAT=0,1)

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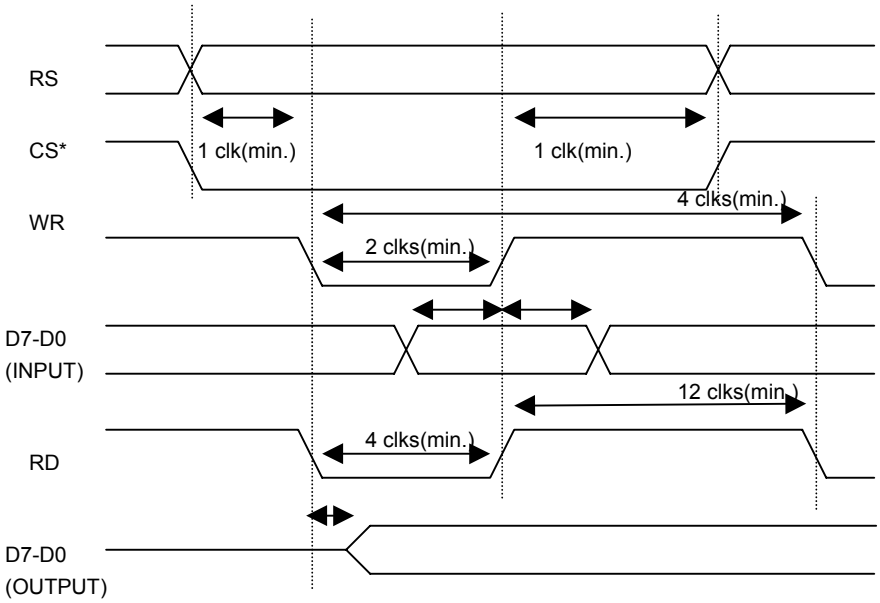


Fig.10_2 Parallel 8080 series interface timing diagram

(RS=1,DFORMAT=2,3)

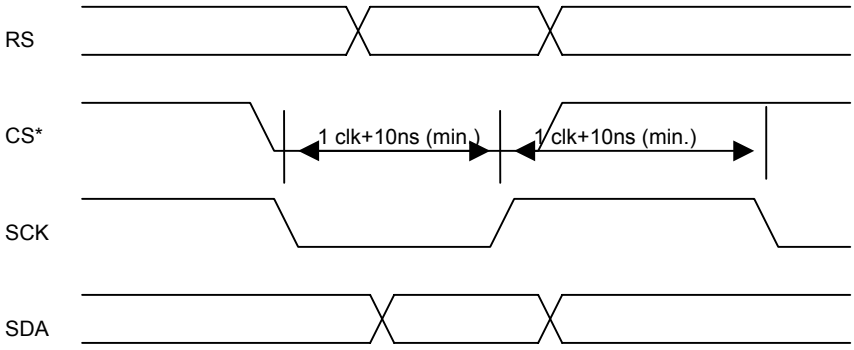


Fig.11 Serial 4-wire interface timing diagram

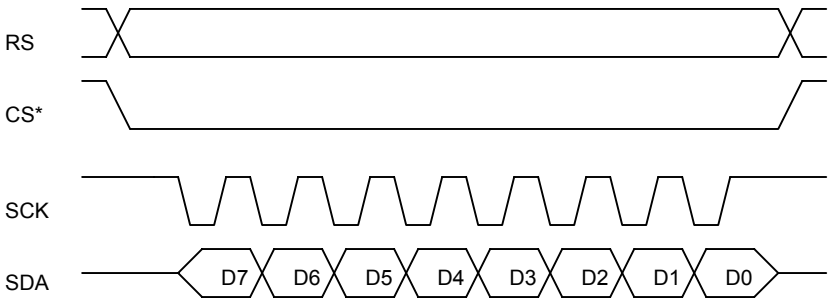
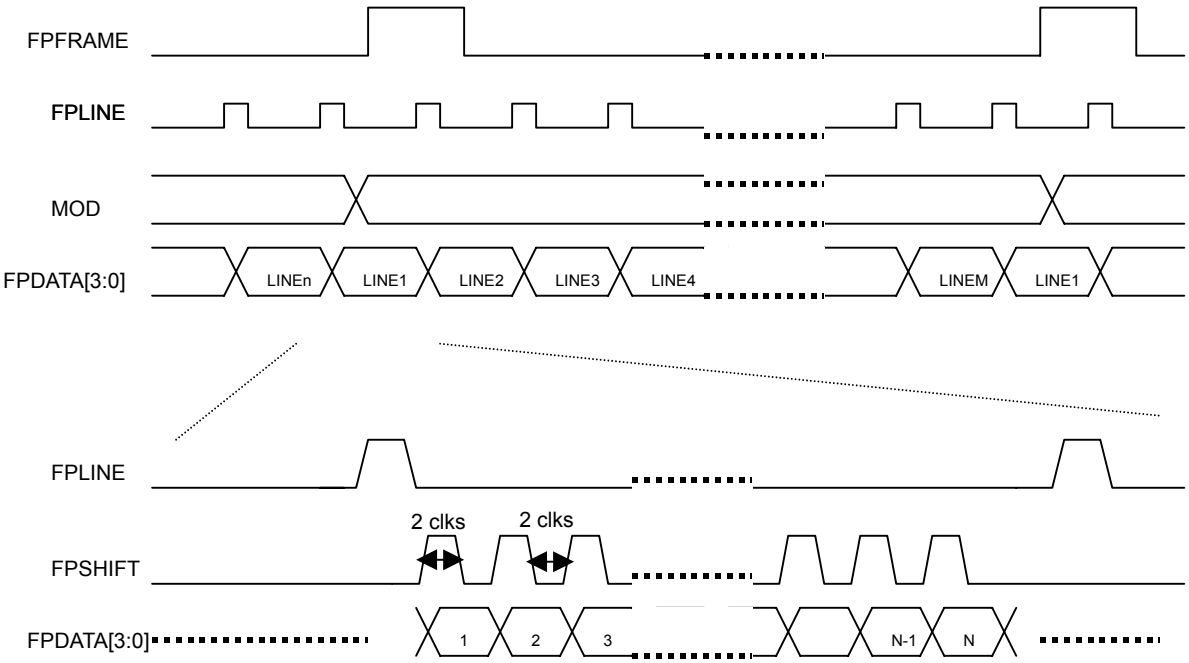


Fig.12 Serial 4-wire data format



**N=40 when horizontal resolution is 160 pixels

N=30 when horizontal resolution is 120 pixels

** M=160 when vertical resolution is 160 lines

M=120 when vertical resolution is 120 lines

Fig.13 LCD Timing Diagram

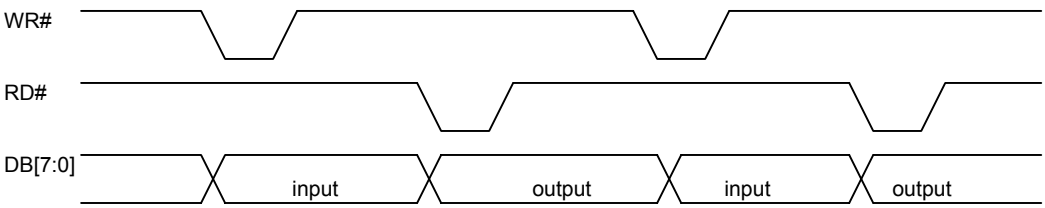


Fig.14 The I/O direction of the MPU data bus (8080 interface)

Absolute Maximum Ratings

Parameter	Symbol	Condictions	Min	Max	Units
Power Supply Voltage	Vdd		0	4	V
Input Voltage	Vt		0	Vdd	V
Operating Temperature	Topr		-20	70	℃

DC Characteristics

Parameter	Symbol	Condictions	Min	Typ	Max	Units
Power Supply Voltage	Vdd		3.0	3.3	3.6	V
Current Consumption	Icp	VDD=3.3V Clock=27MHz		10	11	mA
Digital Outputs						
Output Currents(High)	IoH	VDD=3.3V		-1.1		MA
Output Currents(Low)	IoL	VDD=3.3V		2		MA
Output Voltage(high)	VoH	VDD=3.3V			3.3	V
Output Voltage(high)	VoL	VDD=3.3V	0		0.8	V
Output Capacitance	Co	VDD=3.3V			3	pF
Digital Inputs						
Input Voltage(High)	ViH	VDD=3.3V	2		3.3	V
Input Voltage(Low)	ViL	VDD=3.3V	0		1	
Input Cuttent(High)	IiH	VDD=3.3V			5	uA
Input Voltage(Low)	IiL	VDD=3.3V			5	uA
Input capacitance	Ci	VDD=3.3V			4	PF

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