

Features

- Low start-up power supply voltage :1.4V(CH6)
- Wide supply voltage range from 2.5V to 7V (CH1~6)
- High speed operation is possible: Maximum 1 MHz
- Supports for up, flyback and up/down SEPIC conversion (CH3,4,5,6)
- Synchronized rectification on CH1,CH2
- Totem-pole type output for MOSFET
- Built-in On/Off function
- Built-in Soft-Start function
- Built-in Short-Circuit Protection.

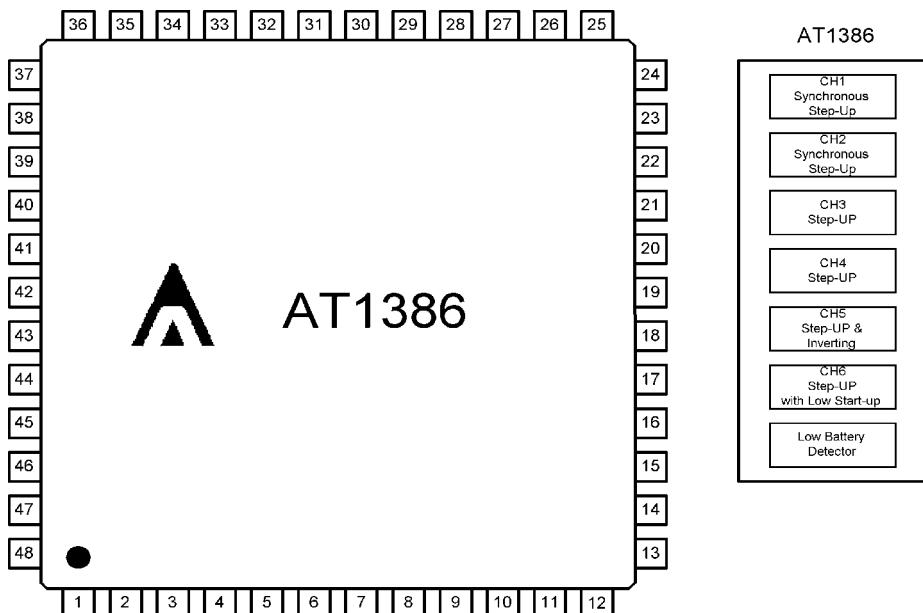
Applications

- Digital Cameras
- CCD Imaging Devices
- Camcorders

General Description

The AT1386 is a 6-channel PWM DC/DC control IC for low voltage applications with a soft start function and short circuit detection function. This IC is ideal for up conversion, down conversion, and up/down conversion (using a step-up/step-down SEPIC system with free input and output settings). 6 channels can be built in the LQFP48 package, each channel be controlled, and soft-start.

The AT1386 include one comparator to generate low-battery warning outputs. It also contains two high efficiency topology by using synchronous rectification PWM(It can be disable by floating OUT1_2,OUT2_2.)

Pin Assignment**Ordering Information**

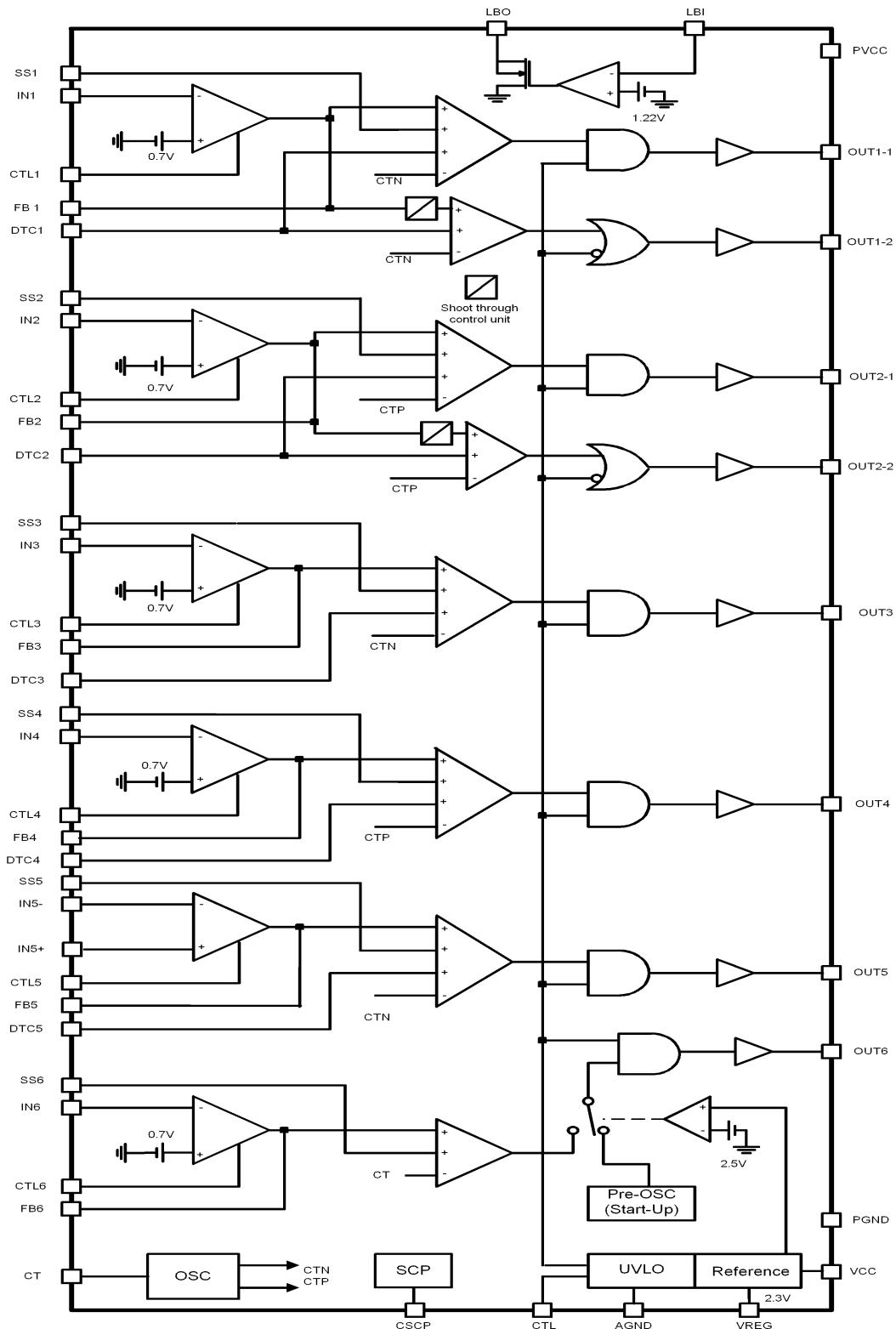
Part number	Package	Marking
AT1386	LQFP48	AT1386F

Aimtron reserves the right without notice to change this circuitry and specifications.

Pin Description

Pin No.	Pin name	I/O	Function
1	SS6	I	CH6 Soft Start Setting Capacitor
2	FB6	I	CH6 Error Amplifier Output
3	IN6	I	CH6 Error Amplifier Inverted Input
4	DTC5	I	CH5 Dead Time Control
5	SS5	I	CH5 Soft Start Setting Capacitor
6	FB5	I	CH5 Error Amplifier Output
7	IN5N	I	CH5 Error Amplifier Negative Input
8	IN5P	I	CH5 Error Amplifier Positive Input
9	DTC4	I	CH4 Dead Time Control
10	SS4	I	CH4 Soft Start Setting Capacitor
11	FB4	I	CH4 Error Amplifier Output
12	IN4	I	CH4 Error Amplifier Inverted Input
13	DTC3	I	CH3 Dead Time Control
14	SS3	I	CH3 Soft Start Setting Capacitor
15	FB3	I	CH3 Error Amplifier Output
16	IN3	I	CH3 Error Amplifier Inverted Input
17	CTL6	I	CH6 ON/OFF Control Input
18	CTL5	I	CH5 ON/OFF Control Input
19	VREG	O	2.3V Regulator Output
20	AGND	P	Power Ground
21	VCC	P	Power Supply
22	CTL4	I	CH4 ON/OFF Control Input
23	CT	-	Oscillation Frequency Setting Capacitor
24	CTL	I	Power Control Input
25	CSCP	-	Timer Latch Short-Circuit Detection Capacitor Input
26	CTL3	I	CH3 ON/OFF Control Input
27	CTL2	I	CH2 ON/OFF Control Input
28	CTL1	I	CH1 ON/OFF Control Input
29	IN2	I	CH2 Error Amplifier Inverted Input
30	FB2	I	CH2 Error Amplifier Output
31	SS2	I	CH2 Soft Start Setting Capacitor
32	DTC2	I	CH2 Dead Time Control
33	IN1	I	CH1 Error Amplifier Inverted Input
34	FB1	I	CH1 Error Amplifier Output
35	SS1	I	CH1 Soft Start Setting Capacitor
36	DTC1	I	CH1 Dead Time Control
37	LBI	I	Low Battery Detector Input
38	LBO	O	Low Battery Indicator
39	OUT1_1	O	CH1 Main Side Output
40	OUT1_2	O	CH1 Synchronous Rectifier Side Output
41	OUT2_1	O	CH2 Main Side Output
42	OUT2_2	O	CH2 Synchronous Rectifier Side Output
43	PVCC	P	Drive Output Block Power Supply
44	PGND	P	Drive Output Block Ground
45	OUT3	O	CH3 Output
46	OUT4	O	CH4 Output
47	OUT5	O	CH5 Output
48	OUT6	O	CH6 Output

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V _{CC}	--	--	7	V
Output current	I _O	Output pin	--	30	mA
Output peak current	I _O	Output pin, Duty $\leq 5\%$	--	200	mA
Power dissipation	P _D	T _A $\leq 25^{\circ}\text{C}$ (LQFP-48P)	--	860	mW
Operation temperature	T _{OPR}	--	-30	85	°C
Storage temperature	T _{STG}	--	-55	125	°C

*Semiconductor devices can be permanently damaged by application of stress in excess of absolute ratings. Do not exceed these ratings.

Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit	
			Min	Typ	Max		
Startup power supply voltage	V _{CC}	CH6	1.4	--	6.5	V	
Power supply voltage	V _{CC}	CH1 to CH6	2.5	5.0	6.5	V	
Regulator voltage output current	I _{OR}	VREG pin	-10	--	0	mA	
Input voltage	V _{IN}	IN1 to IN6 pins	0	--	V _{CC} -1.8	V	
Control input voltage	V _{CTL}	CTL pin	0	--	6.5	V	
Output current	I _O	OUT pin (CH1 to CH5)	--	2	15	mA	
		OUT pin (CH6)	1	2	15	mA	
Oscillator	f _{OSC}	--	100	500	1000	kHz	
Timing capacitor	C _T	--	47	82	560	pF	
Soft start capacitor	C _S	CH1 to CH5	--	0.1	1.0	μF	
	C _{SS6}	CH6	--	0.1	1.0	μF	
Short detection capacitor	C _{CSCP}	--	--	0.1	1.0	μF	
VREG pin capacitor	C _{VREG}	--	0.082	0.1	--	μF	
Operating ambient temperature	T _A	--	-30	25	85	°C	

Electrical Characteristics

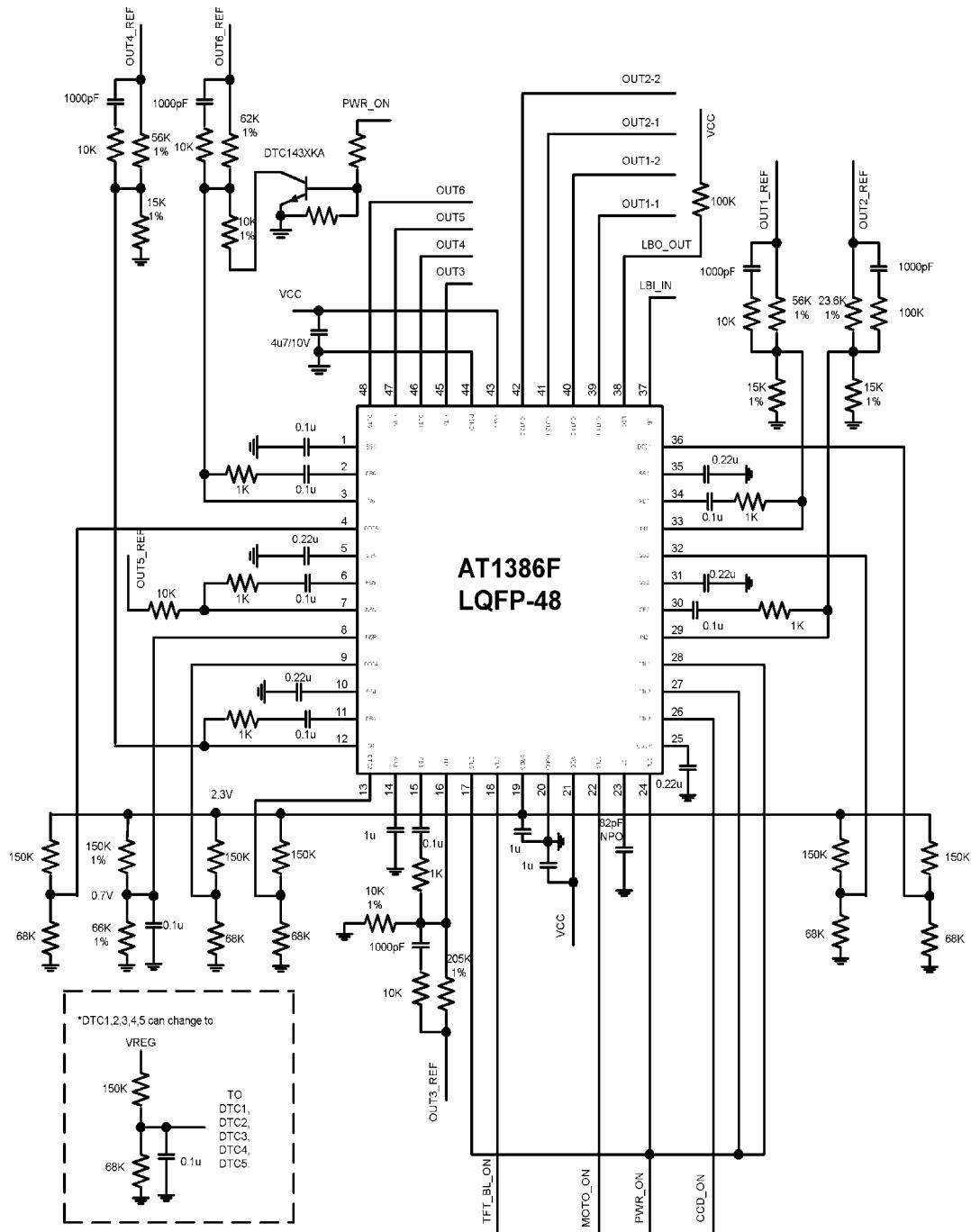
($T_A=25^\circ\text{C}$, VCC=PVCC=5V)

Parameter	Symbol	Condition	Measure result			Unit
			Min.	Typ.	Max.	
Reference voltage block [REF]						
Regulator voltage	V_{REG}		2.25	2.30	2.35	V
Output voltage temperature stability	$\Delta V_{\text{REF}} / V_{\text{REF}}$	$T_A = -30^\circ\text{C} \text{ to } 85^\circ\text{C}$	-	0.5	-	%
Input stability	Line	VCC=2.5V to 6.5V	-80	-	80	mV
Load stability	Load	$V_{\text{REG}}=0\text{mA}$ to -10mA	-20	-	20	mV
Under voltage lockout block [U.V.L.O]						
Threshold voltage(CH1~CH5)	V_{TH}		2.0	2.2	2.3	V
Hysteresis width(CH1~CH5)	$V_{\text{H1_5}}$		0.05	0.1	0.3	V
CH6 Pre-OSC change to Main-OSC threshold	V_{TH6}		2.2	2.3	2.5	V
Hysteresis width(CH6 Pre-OSC change to Main-OSC threshold)	V_{H6}		0.05	0.1	0.3	V
Pre-OSC frequency	$f_{\text{PRE-OSC}}$		320	400	480	KHz
Soft start block [CS]						
Charge current	I_{CS}		-1.5	-1.0	-0.8	μA
Invalid Threshold voltage			-	0.3	-	V
Short circuit detection block [SCP]						
Threshold voltage	V_{TH}		0.80	0.90	1.00	V
Input source current	I_{CSCP}		-1.5	-1.0	-0.6	μA
Short detect comparator [SCP Comp]						
Threshold voltage	V_{TH}	CH1 to CH6	0.65	0.7	0.75	V
Input bias current	I_{B}	IN=0V	-320	-80	-	nA
Triangular wave oscillator block [OSC]						
Oscillator frequency	f_{osc}	$CT=82\text{pF}$	400	500	600	KHz
Frequency stability for voltage	$\Delta f / f_{\text{dv}}$	$VCC=2.5\text{V}$ to 6.5V	-	1	10	%
Frequency stability for temperature	$\Delta f / f_{\text{dt}}$	$T_A=-30^\circ\text{C} \text{ to } 85^\circ\text{C}$	-	1	10	%

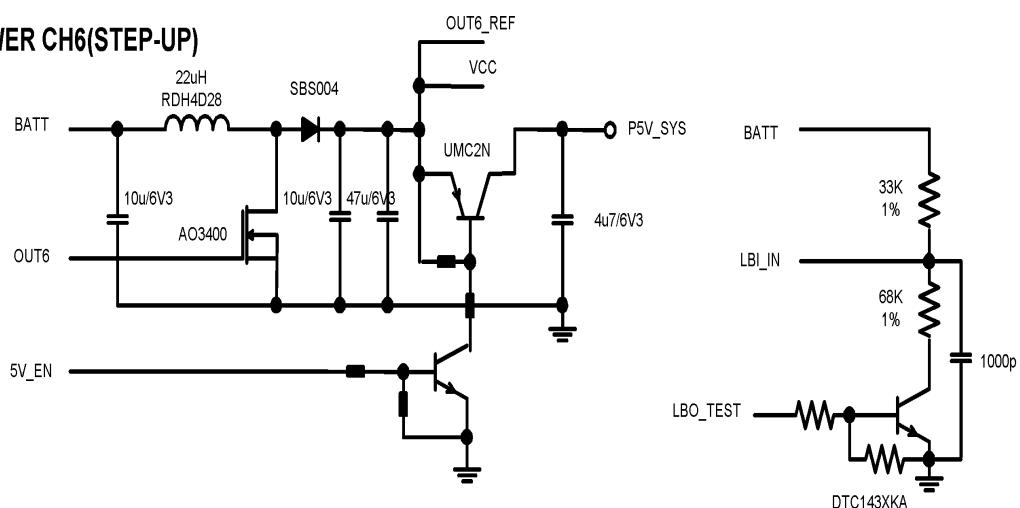
Error amplifier block [Error Amp](CH1~CH6)						
Threshold voltage	V_{TH}	FB=IN	0.682	0.70	0.717	V
V_{TH} temperature stability	$\Delta V_T/V_T$	$T_A = -30^\circ C$ to $85^\circ C$	-	0.5	-	%
Input bias current	I_B	IN=0.7V	-	80	320	nA
Voltage gain	A_V	DC	-	100	-	dB
Frequency bandwidth	BW	$A_v=0dB$	-	10	-	MHz
Output voltage	V_{OH}		0.9	1.0	1.2	V
	V_{OL}		-	50	200	mV
Output source current	I_{SOURCE}	FB=0.5V	-	-4.0	-1.0	mA
Output sink current	I_{SINK}	FB=0.5V	70	140	-	μA
PWM Comp. [PWM Comp]						
Threshold voltage(CH1~6)	V_{T0}	Duty = 0 %	0.25	0.3	-	V
	V_{Tmax}	Duty = 100 %	-	0.80	0.85	V
Input current	I_{DTC}	DTC=0.5V	-1.0	-0.3	-	μA
Output block (CH1 to CH5) [Pin 39,41,45,46,47]						
Output source current	I_{SOURCE}	OUT=1/2VCC	-	-130	-80	mA
Output sink current	I_{SINK}	OUT=1/2VCC	65	100	-	mA
Output ON resistor	R_{OH}	OUT = -15mA	-	10	25	Ω
	R_{OL}	OUT = 15mA	-	10	25	Ω
Output block (CH1,2) [Pin 40,42]						
Output source current	I_{SOURCE}	OUT=1/2VCC	-	-130	-80	mA
Output sink current	I_{SINK}	OUT=1/2VCC	65	100	-	mA
Output ON resistor	R_{OH}	OUT = -15mA	-	10	25	Ω
	R_{OL}	OUT = 15mA	-	10	25	Ω
Output block (CH6) [Pin 48]						
Output source current	I_{SOURCE}	OUT=1/2VCC	-	-260	-160	mA
Output sink current	I_{SINK}	OUT=1/2VCC	130	200	-	mA
Output ON resistor	R_{OH}	OUT = -15mA	-	10	25	Ω
	R_{OL}	OUT = 15mA	-	10	25	Ω
Control block [CTL]						
CTL input voltage	V_{IH}	Active mode	1.3	-	7	V
	V_{IL}	Standby mode	0	-	0.7	V
CTL1 to CTL6 input voltage	V_{IH}	Active mode	1.3	-	7	V

	V _{IL}	Standby mode	0	-	0.7	V
Input current	I _{CTL}	CTL = 5V	-	5	20	μA
Low battery detect block [LBI, LBO]						
LBI detect threshold			1.20	1.22	1.24	V
Detect Hysteresis			-50		+50	mV
LBO output voltage low		I _{sink} =1mA	-	-	0.4	V
LBO output high leakage		V _{LBO} =5V	-	0.01	1	μA
General(Output no Load)						
Standby current	I _{css}	CTL=CTL1=CTL2=CTL3=CTL4=CTL5=CTL6=0V	-	1	10	μA
	I _{css(o)}	CTL=0V, CTL1=CTL2=CTL3=CTL4=CTL5=CTL6="H"	-	200	250	μA
Power supply current	I _{cc1}	CTL=CTL1=CTL2=CTL3=CTL4=CTL5=CTL6="H"	-	5	7	mA
Power supply current	I _{cc2}	CTL="H" CTL1=CTL2=CTL3=CTL4=CTL5=CTL6="L"	-	2	2.5	mA

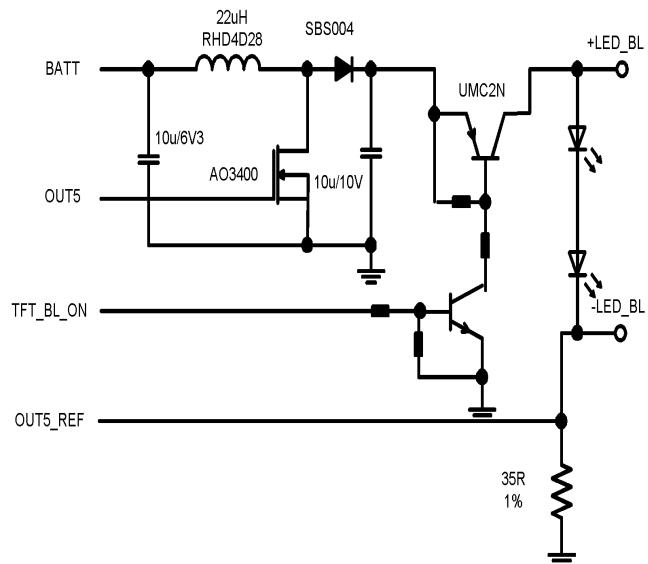
Application Circuit



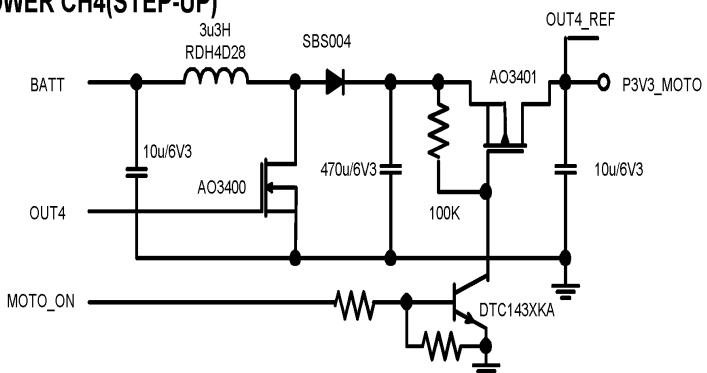
POWER CH6(STEP-UP)



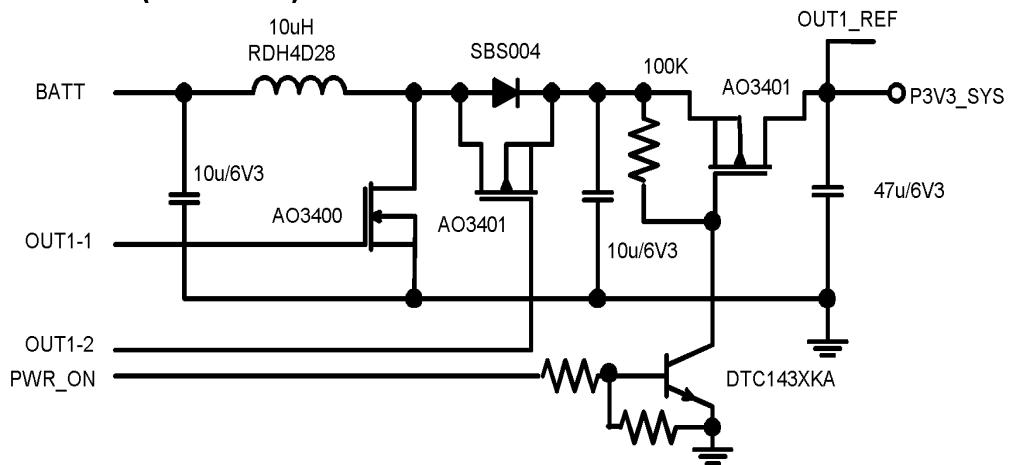
POWER CH5(STEP-UP)



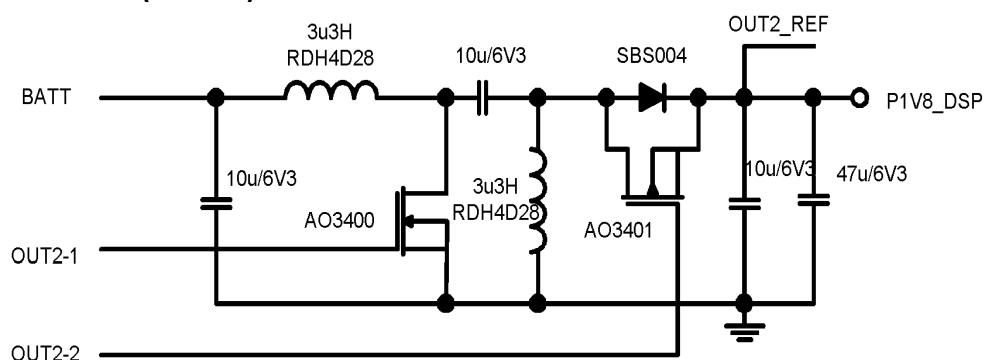
POWER CH4(STEP-UP)



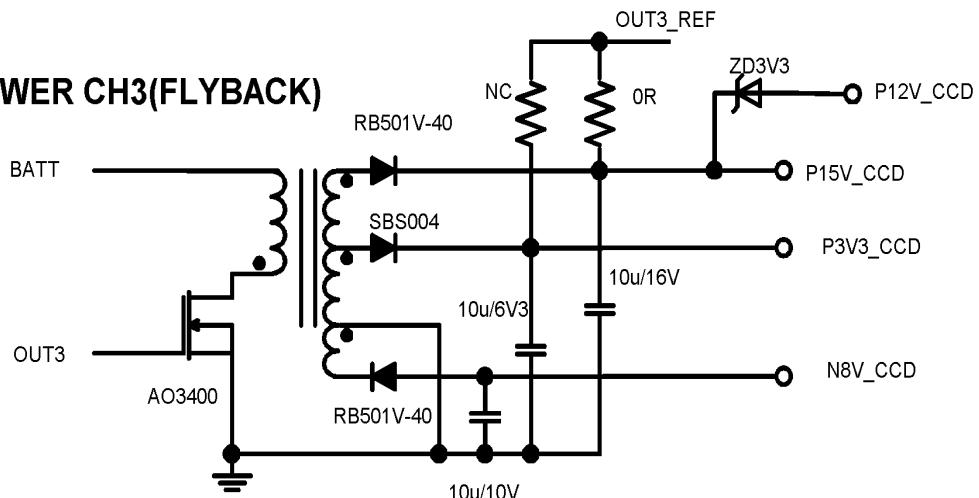
POWER CH1(STEP-UP)



POWER CH2(SEPIC)



POWER CH3(FLYBACK)



Function Description

1. Power Converter Functions

* Reference voltage block

The reference voltage circuit generates a temperature independence voltage (typical=2.3V) from the power source, which is used as reference voltage for the IC's internal circuitry and supply load current above 10mA to external device.

* Triangular oscillator block

The triangular wave oscillator is generated by timing capacitor(CT) to incorporate each other. The waveforms CT (amplitude of 0.3V to 0.8V), CTP (amplitude 0.3V to 0.8V in phase with CT) and CTN (amplitude 0.3V to 0.8V in inverse phase with CT) are input to the PWM comparator.

* Error amplifier block

The error amplifier outputs controlling error signal to PWM comparator from sensing DC/DC converter output voltage. In addition, an arbitrary loop gain can be set by connecting feedback resistor and capacitor from the output pin to inverted input pin of the error amplifier, in order to make a stable system.

* CH5 Inverting amplifier block

The inverting amplifier detects the DC/DC converter output voltage (negative) and outputs a control signal to the error amplifier.

* PWM comparator block

The PWM comparator is a voltage-to-pulse width converter for controlling the duty cycle of DC/DC converter.

Channels 1, 2 main sides, channel 3, 4, 5, and 6 : The comparator keeps the output transistor turn on while the error amplifier output voltage and DTC voltage still higher than the triangular wave voltage.

Channels 1, 2 synchronous rectification sides : The comparator keeps the output transistor turn on while the error amplifier output voltage still lower than the triangular wave voltage.

*Output block

The output block is the totem pole configuration, which could drive external MOSFET or transistor.

2. Channel Control Function

The channels are turned on and turned off depending on the voltage levels at the CTL, CTL12, CTL3, CTL4, CTL5, and CTL6. Described as follow.

CTL	L	H					
CTL1	X	H	Z	Z	Z	Z	Z
CTL2	X	Z	H	Z	Z	Z	Z
CTL3	X	Z	Z	H	Z	Z	Z
CTL4	X	Z	Z	Z	H	Z	Z
CTL5	X	Z	Z	Z	Z	H	Z
CTL6	X	Z	Z	Z	Z	Z	H
CH1	OFF	ON	OFF	OFF	OFF	OFF	OFF
CH2		OFF	ON	OFF	OFF	OFF	OFF
CH3		OFF	OFF	ON	OFF	OFF	OFF
CH4		OFF	OFF	OFF	ON	OFF	OFF
CH5		OFF	OFF	OFF	OFF	ON	OFF
CH6		OFF	OFF	OFF	OFF	OFF	ON

X : Don't care Z: Low or Floating

3. Protective Functions

* Short circuit protection and timer latch

The short circuit detection comparator in each channel detects the output voltage level of power converter. When the output voltage falls below the short detection level, there is a constant current bias charging the external capacitor C_{CSCP} which connected to the CSCP pin until the capacitor voltage level reaches about 0.7V then disable the IC. It could reset the actuated protection by restart the power source or pull CTL from low to high.

* Under-voltage lockout protection

The under-voltage lockout protection is to disable the IC while the supply voltage transient or momentary decrease, which may cause the IC to malfunction. To prevent such malfunctions, the under-voltage lockout protection circuit detects a

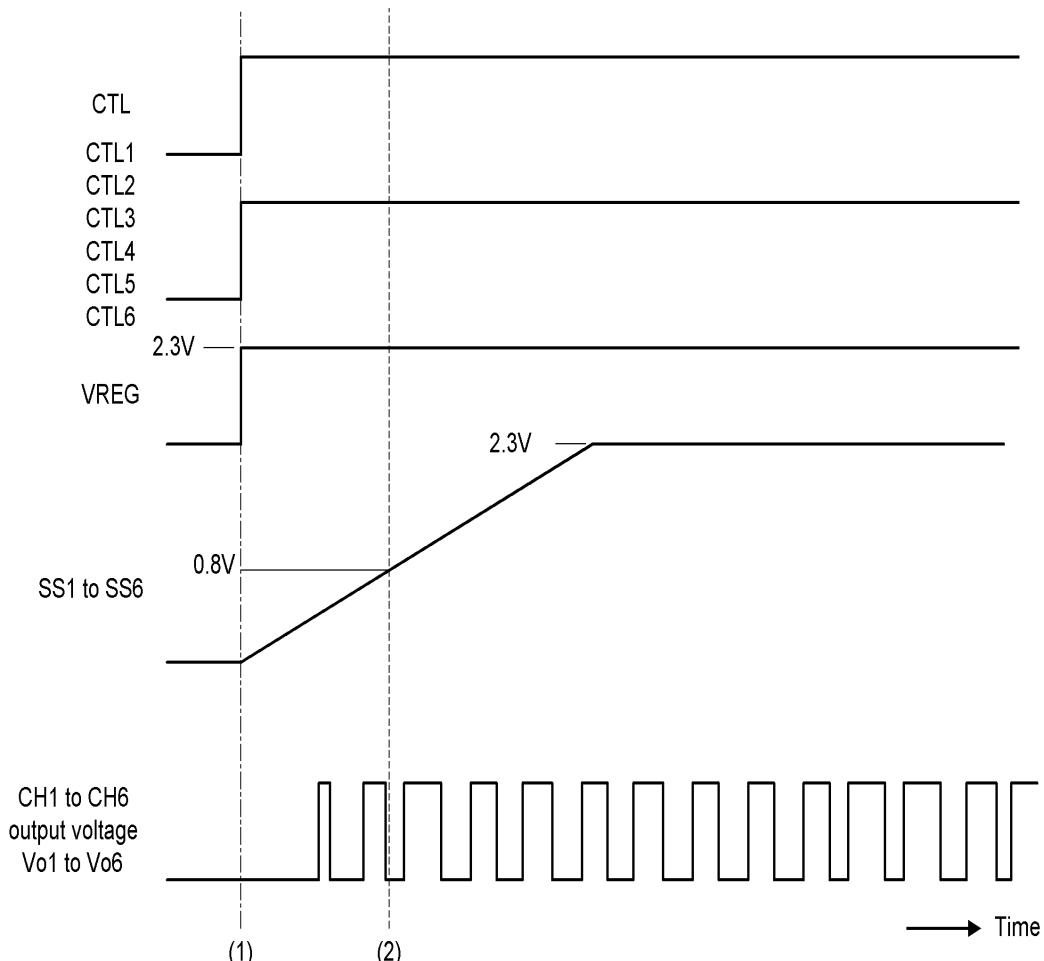
decrease in internal reference voltage with respect to the power supply voltage, turns off the output transistor, and holding the CSCP pin at the “L” level.

*Battery Low Detect Function

The Battery low comparator open-drain output LBO sinks up to 1mA if the LBI input is below its threshold voltage. Connect LBO to power source with a 100KΩ~1MΩ pull-up resistor.

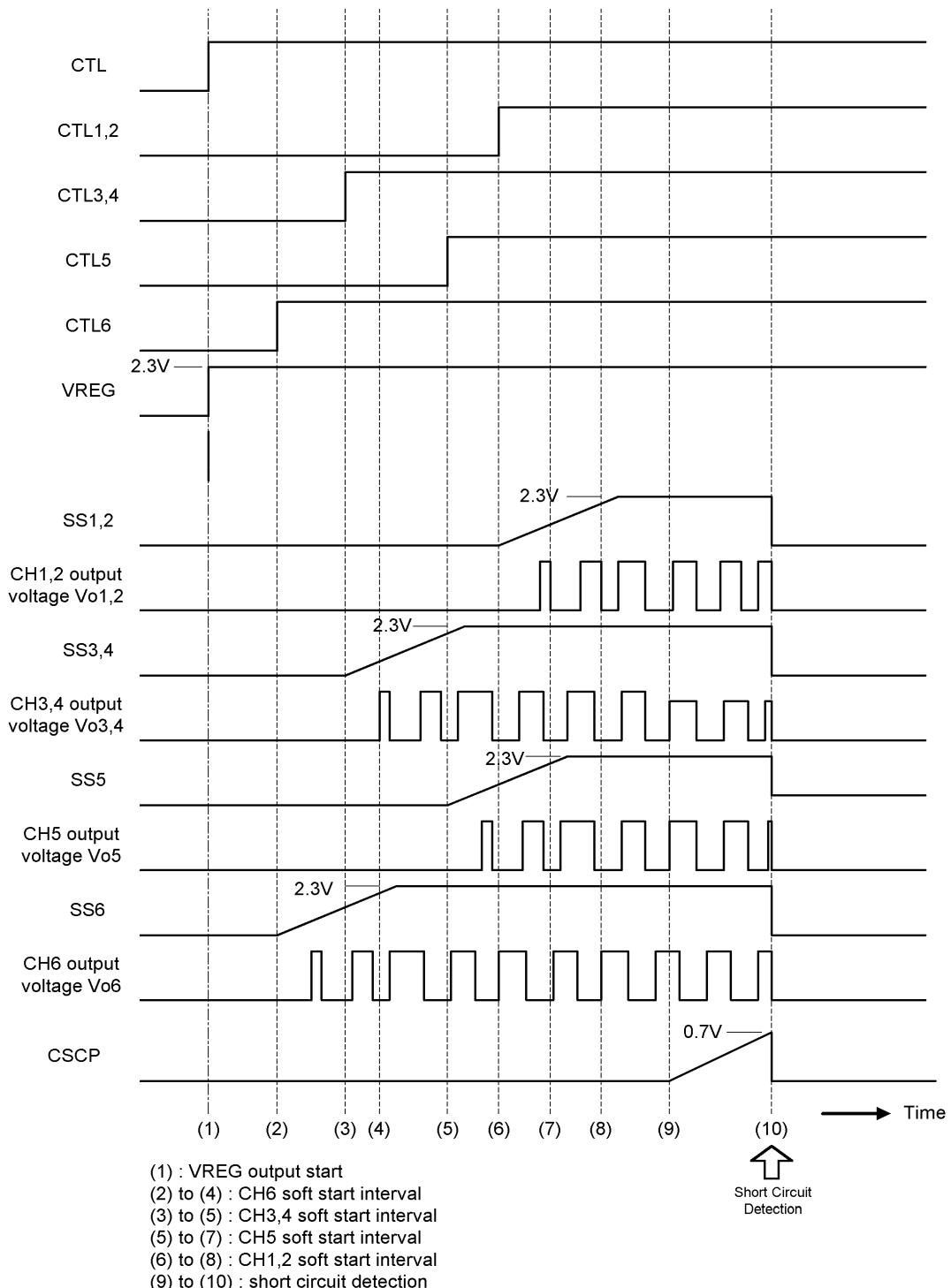
4. Soft Start Operation

* The CTL, CTL1,2, CTL3, CTL4, CTL5 and CTL6 terminals are driven high level at the same time. The driving scheme is described as follow diagram.



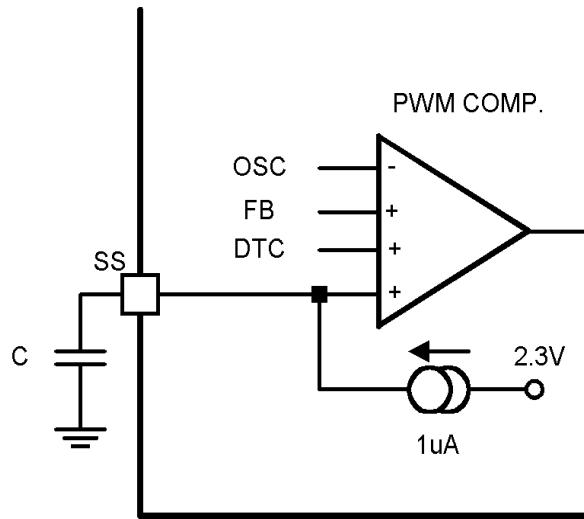
(1) to (2) : CH1 to CH6 soft start interval

* After CTL ON, driving the CTL1, CTL2, CTL3, CTL4, CTL5 and CTL6 to high level. The driving scheme is described as follow diagram.



* Soft start setting (CH1~6)

Consider the input voltage and load current to design the capacitor connected to the SS pin.



It can calculate the CH1~6 soft start time $T_s(s)$.

$$C \times \frac{\Delta V}{\Delta t} = I$$

$$T_s(s) = 0.5 \times C(\mu F)$$

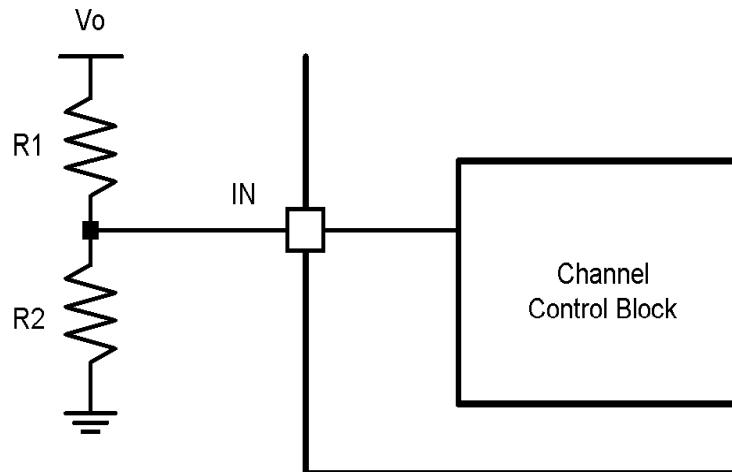
Note : It could be disabled soft start function by floating SS pin.

Determine the triangular Oscillator Frequency

The triangular oscillator frequency is determined by the timing capacitor (C_T). It is difficult to incorporate these non-linear characteristics into the equation. This difference is caused by characteristics, such as changes in the maximum voltage amplitude of the sawtooth waveform with the CT value and the circuit delay causing the maximum amplitude to become large in the case of a high oscillating frequency even for the same capacitor. In practical use, therefore, the user should read the CT values from the characteristic curve or should determine an approximate target value by using the equation.

Design the DC/DC Output Voltage

*CH1~6



$$V_o = 0.7 \times \frac{R_1 + R_2}{R_2}$$

Setting Time Period When Short Circuit Protection

The CSCP comparator detects each channel output voltage while the power converter work at normal condition. At the same time, the voltage level of CSCP pin is held at low level. If the output load of these converters rapidly malfunction or short, causing the output voltage to drop, the CSCP comparator detects that to enable short circuit protection. The time period when short circuit protection show as follow equation.

Short detection time ($T_{PE}(s)$)

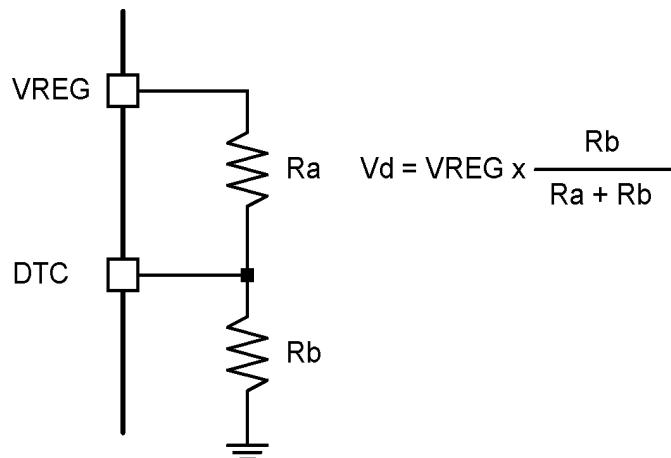
$$T_{PE}(s) = 0.7 * C_{CSCP} (\mu F)$$

Note : It could be disabled short circuit protection function by connecting CSCP pin into the ground.

Setting the Dead Time Control Level

When using Boost, SEPIC, Zeta or flyback DC/DC converter, it must prevent that output transistor works at full-ON state (ON duty = 100%). To prevent this situation, set the maximum duty of these channels. The dead time control circuit is implemented as below. When the voltage at the DTC pin is higher than the triangular wave voltage (CT, CTP, CTN), the output transistor is turned on. The maximum duty calculation formula assuming that triangular wave amplitude = 0.5V and triangular wave minimum voltage = 0.3V.

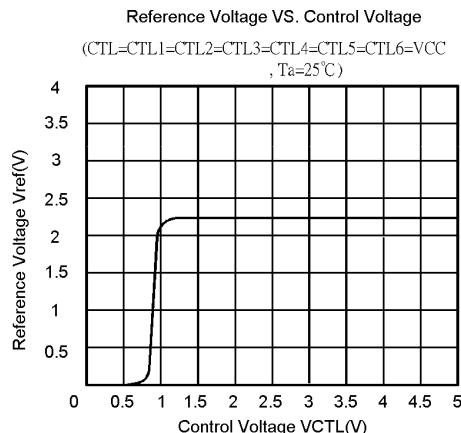
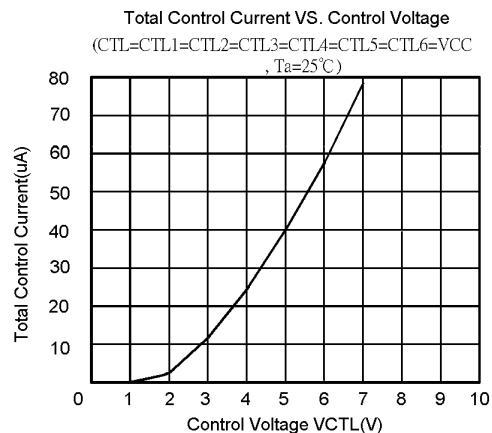
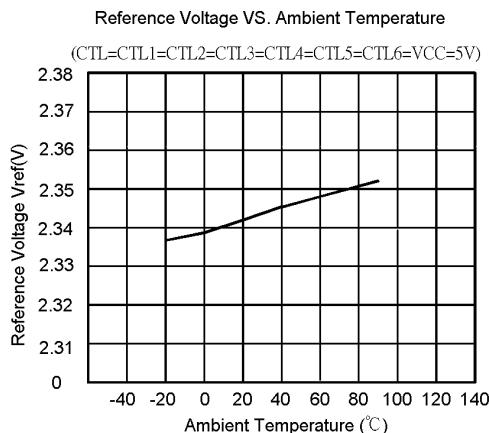
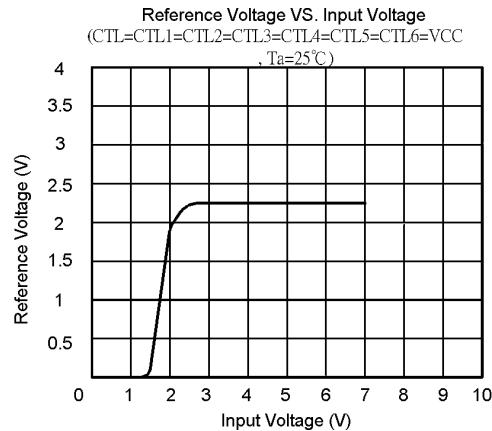
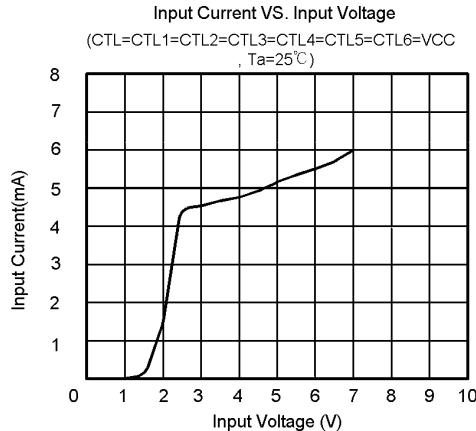
$$Duty_{MAX.} = \left(\frac{Vd - 0.3}{0.5} \right) \times 100\%$$

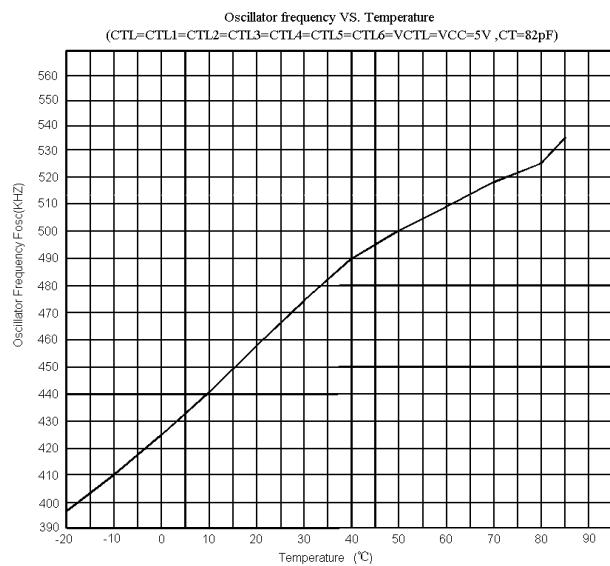
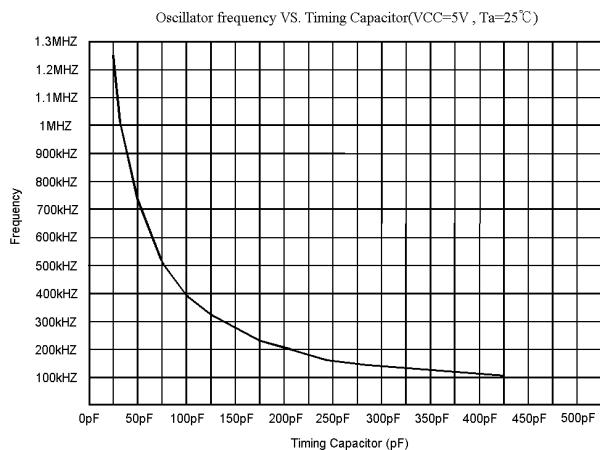
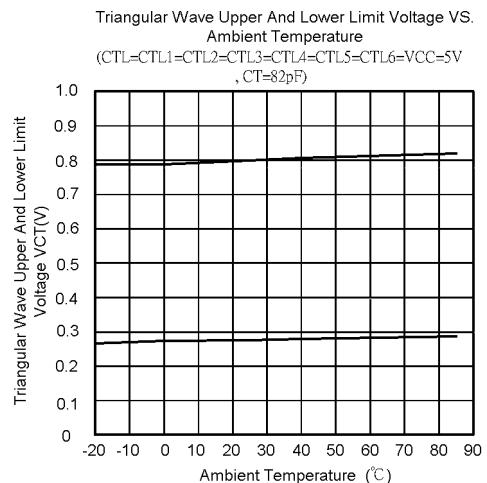
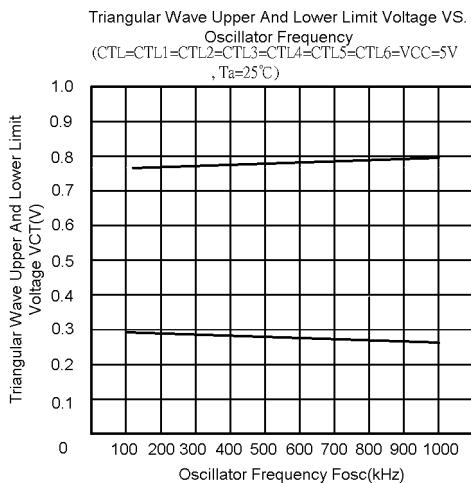


Note 1 : The circuit is suitable at CH1 to CH6.

Note 2 : Shorting DTC and VREG to disable dead time control function.

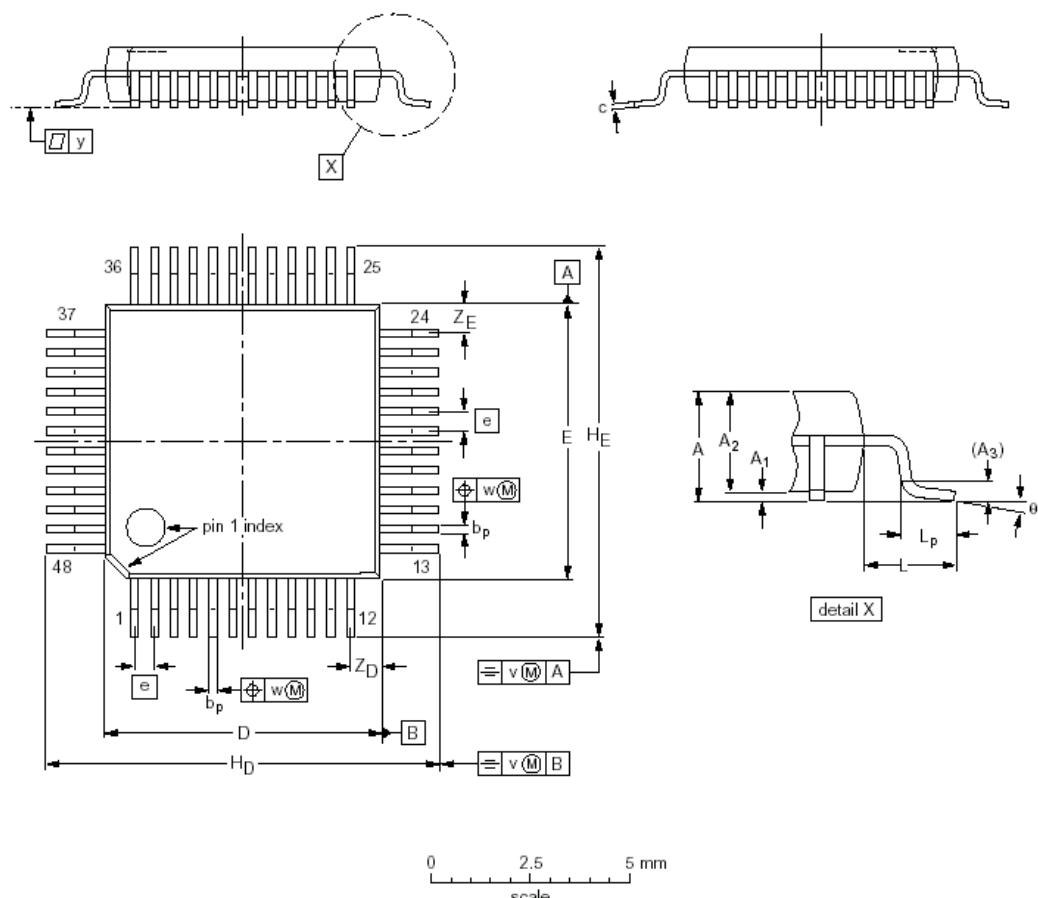
Typical Characteristics





Package Outline

LQFP48

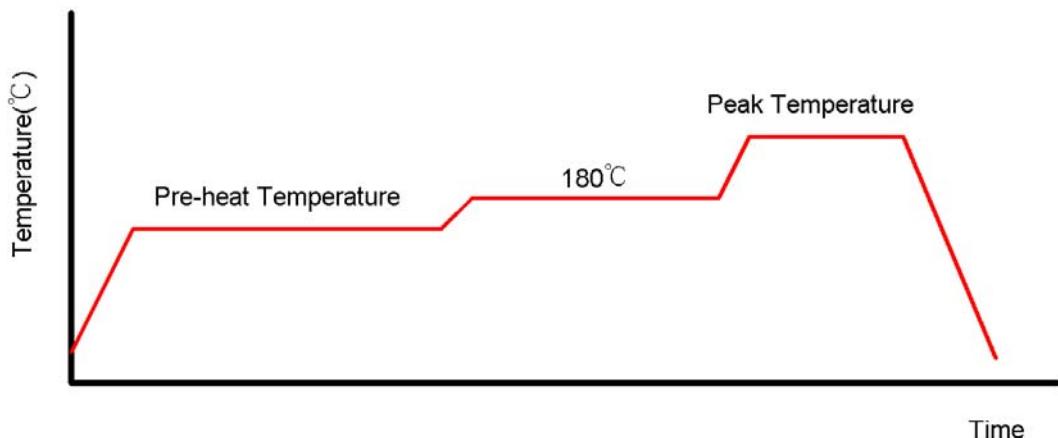


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	1.60 0.05	0.20 1.35	1.45 0.25	0.25 0.17	0.27 0.12	0.18 6.9	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A



Classification Reflow Profiles

	Convection or IR/Convction	VPR
Average Heating Rate(180°C to peak)	5°C/second max.	10°C/second max.
Preheat Temperature($125 \pm 20^\circ\text{C}$)	120 seconds max.	
Temperature maintained above 180°C	10~150 seconds	
Time within 5°C of actual Peak Temperature	10~20 seconds	60 seconds
Peak Temperature Range(Note 1)	219~225°C or 235~240°C	219~225°C or 235~240°C
Cooling Rate	6°C /second max.	10°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	

*1 The maximum peak temperatures for IR and VP reflow are depending on package dimensions.

Package Reflow Conditions

Pkg. Thickness $\geq 2.5\text{mm}$ and all bags	Pkg. Thickness $< 2.5\text{mm}$ and Pkg. Volume $\geq 350\text{ mm}^3$	Pkg. Thickness $< 2.5\text{mm}$ and Pkg. Volume $< 350\text{ mm}^3$
Convection 219~225°C		Convection 235~240°C
VPR 219~225°C		VPR 235~240°C
IR/Convection 219~225°C		IR/Convection 235~240°C