Aimtron
圓創科技股份有限公司

AT1382A

Preliminary Product Information

4-Channel DC-DC Converter for DSC

Features

- Low start-up power supply voltage :1.4V(CH4)
- Wide supply voltage range from 1.8V to 7V (CH1~4)
- High speed operation is possible: Maximum 1 MHz
- Supports for up, flyback and up/down SEPIC conversion (CH1~4)
- Totem-pole type output for MOSFET
- Built-in On/Off function
- Built-in Short-Circuit Protection.

Applications

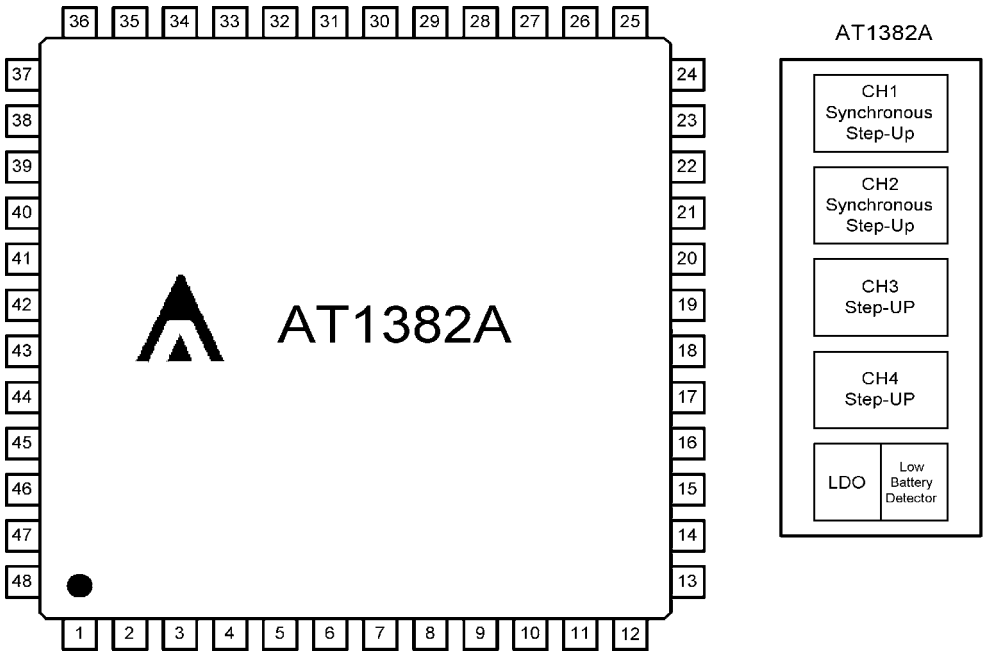
- Digital Cameras
- CCD Imaging Devices
- Camcorders

General Description

The AT1382A is a 4-channel PWM DC/DC control IC for low voltage applications with a soft start function and short circuit detection function. This IC is ideal for up conversion, down conversion, and up/down conversion (using a step-up/step-down SEPIC system with free input and output settings). Four channels can be built in the LQFP48 package, each channel be controlled, and soft-start.

The AT1382A include one comparator to generate low-battery warning outputs. It also contains a gain block that can be used with an external P-channel MOSFET to make a low-dropout linear regulator.

Pin Assignment



Ordering Information

Part number	Package	Marking
AT1382A	LQFP48	AT1382AF

Aimtron reserves the right without notice to change this circuitry and specifications.

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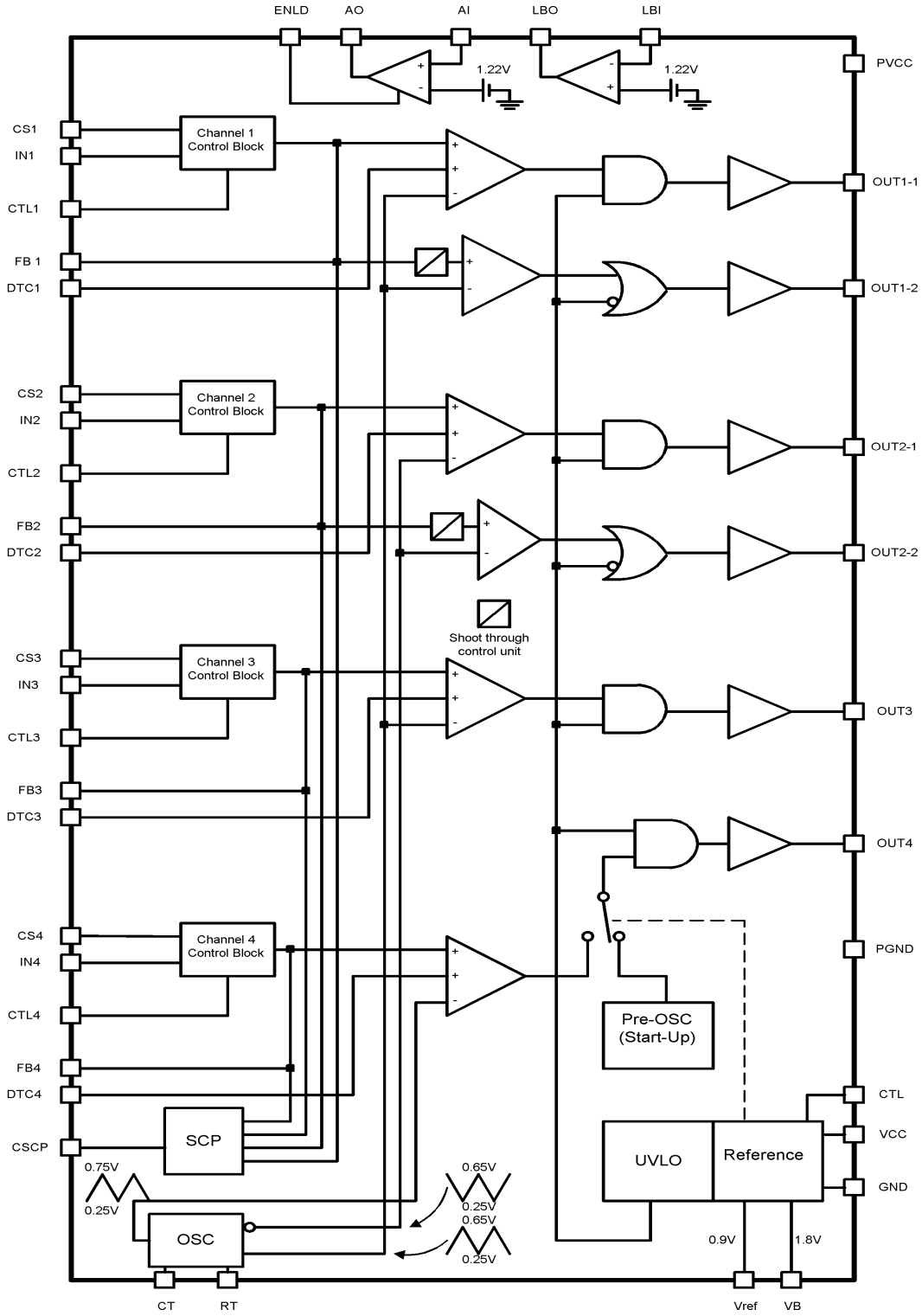
Pin Description

Pin No.	Pin name	I/O	Function
1	DTC4	I	CH4 Dead Time Control
2	FB4	O	CH4 Error Amplifier Output
3	IN4	I	CH4 Error Amplifier Inverted Input
4	CS4	-	CH4 Soft Start Setting Capacitor
5	CTL4	I	CH4 ON/OFF Control
6	DTC3	I	CH3 Dead Time Control
7	FB3	O	CH3 Error Amplifier Output
8	IN3	I	CH3 Error Amplifier Inverted Input
9	CS3	-	CH3 Soft Start Setting Capacitor
10	CTL3	I	CH3 ON/OFF Control
11	CSCP	-	Timer Latch Short-Circuit Detection Capacitor Input
12	VREF	O	Reference 0.9V Output
13	GND	P	Ground
14	GND	P	Ground
15	VBG	TEST	Reference Test Pin
16	VCC	P	Power Supply
17	VCC	P	Power Supply
18	POR	TEST	Pre-OSC Change to Main-OSC Indicator
19	RT	-	Oscillation Frequency Setting Resistor
20	CT	-	Oscillation Frequency Setting Capacitor
21	VB	O	Reference 1.8V Output
22	CTL	I	Power Supply Control
23	ENLD	I	Gain Block Enable Input
24	CT2	TEST	Triangular wave OSC Inverted output Test Pin
25	CTL2	I	CH2 ON/OFF Control
26	CS2	-	CH2 Soft Start Setting Capacitor
27	IN2	I	CH2 Error Amplifier Inverted Input
28	FB2	O	CH2 Error Amplifier Output
29	DTC2	I	CH2 Dead Time Control
30	CTL1	I	CH1 ON/OFF Control
31	CS1	-	CH1 Soft Start Setting Capacitor
32	IN1	I	CH1 Error Amplifier Inverted Input
33	FB1	O	CH1 Error Amplifier Output
34	DTC1	I	CH1 Dead Time Control
35	LBI	I	Low Battery Detected Input
36	LBO	O	Low Battery Indicator
37	AI	I	LDO Regulated Input
38	AO	O	LDO Drive Output
39	OUT1_1	O	CH1 Main Side Output
40	OUT1_2	O	CH1 Synchronous Rectifier Side Output
41	OUT2_1	O	CH2 Main Side Output
42	OUT2_2	O	CH2 Synchronous Rectifier Side Output
43	N.C.	-	
44	PVCC	P	Drive Output Block Power Supply
45	N.C.	-	
46	PGND	P	Drive Output Block Ground
47	OUT3	O	CH3 Output
48	OUT4	O	CH4 Output

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	Vcc	--	--	8	V
Output current	Io	Output pin	--	20	mA
Output peak current	Io	Output pin, Duty≦5%	--	200	mA
Power dissipation	P_D	Ta≦25℃ (LQFP-48P)	--	860	mW
Operation temperature	Topr	--	-30	85	℃
Storage temperature	Tstg	--	-55	125	℃

***Semiconductor devices can be permanently damaged by application of stress in excess of absolute ratings. Do not exceed these ratings.**

Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Startup power supply voltage	Vcc	CH4	1.4	--	7	V
Power supply voltage	Vcc	CH4	1.5	5.0	7	V
		CH1 to CH3	1.8	5.0	7	V
Reference voltage output current	I_{OR}	VREF pin	-1	--	0	mA
VB pin output current	I_B	VB pin	-0.5	--	0	mA
Input voltage	V_{IN}	IN1 to IN4 pins	0	--	Vcc-1.8	V
Control input voltage	V_{CTL}	CTL pin	0	--	7	V
Output current	Io	OUT pin (CH1 to CH3)	--	2	15	mA
		OUT pin (CH4)	1	2	15	mA
Oscillator	f_{OSC}	--	100	500	1000	kHz
Timing capacitor	C_T	--	47	100	560	pF
Timing resistor	R_T	--	8.2	18	100	kΩ
Soft start capacitor	Cs	CH1 to CH3	--	0.027	1.0	μF
	C_{CS4}	CH4	--	0.47	1.0	μF
Short detection capacitor	C_{SCP}	--	--	0.1	1.0	μF
VB pin capacitor	C_{VB}	--	0.082	0.1	--	μF
Operating ambient temperature	Ta	--	-30	25	85	℃

Electrical Characteristics

(Ta=25℃, VCC=PVCC=5V)

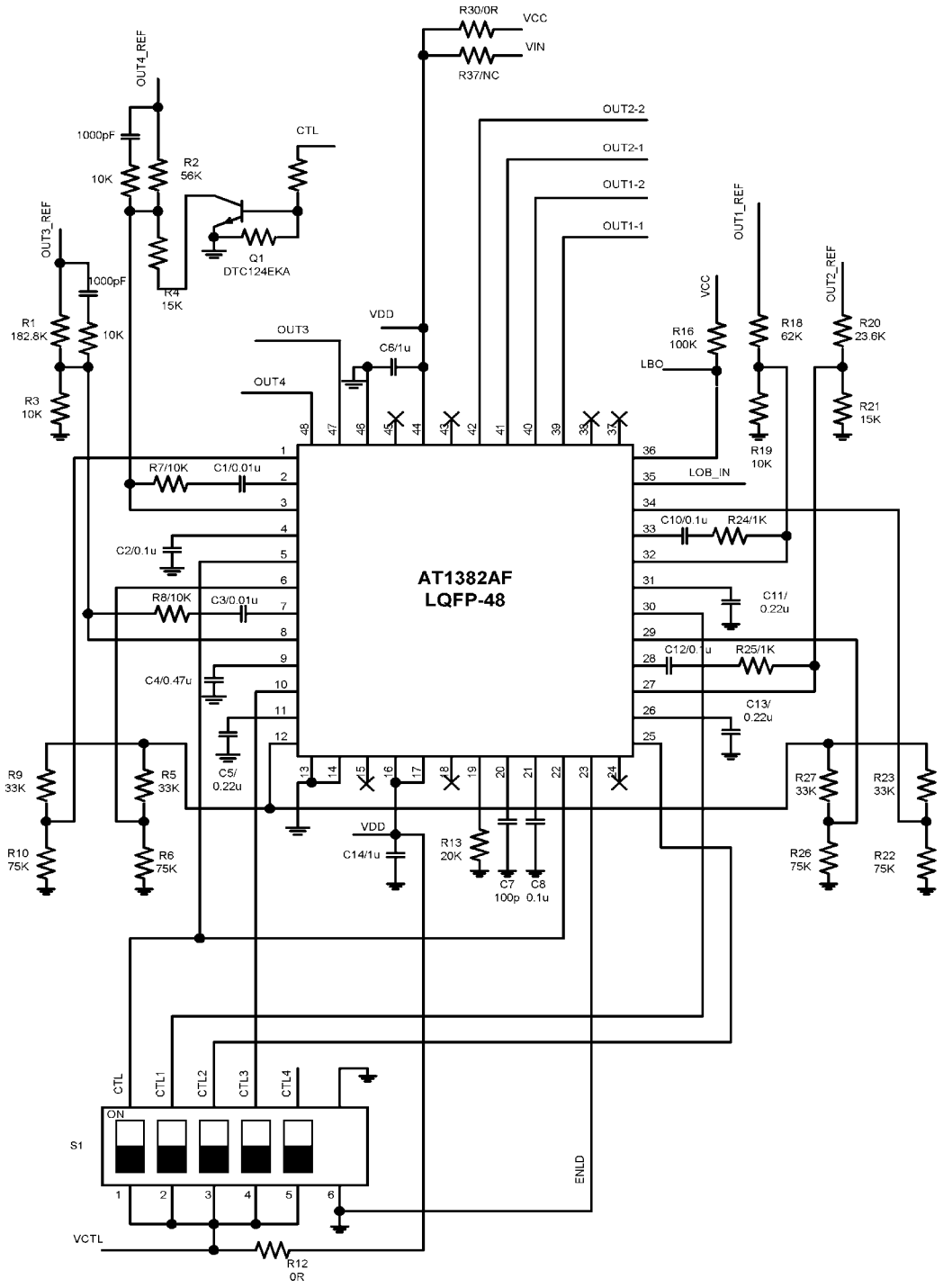
Parameter	Symbol	Condition	Measure result			Unit
			Min.	Typ.	Max.	
Reference voltage block [REF]						
Reference voltage	V_{REF}		0.88	0.90	0.92	V
Output voltage temperature stability	$\triangle V_{REF}$ /V_{REF}	Ta = -30℃ to 85℃	-	0.5	-	%
Input stability	Line	VCC=1.8V to 7V	-10	-	10	mV
Load stability	Load	VREF=0mA to –1mA	-10	-	10	mV
Shout circuit output current	I_{OSC}	VREF=0.7V	-20	-5	-1	mA
Under voltage lockout block [U.V.L.O]						
Threshold voltage(CH1~CH3)	V_{TH}		1.5	1.6	1.7	V
Hysteresis width(CH1~CH3)	V_H		-	0.2	-	V
Reset voltage(CH1~CH3)	V_{RST}		1.6	1.7	1.8	V
CH4 Pre-OSC change to Main-OSC threshold	V_{TH2}		-	1.7	-	V
Soft start block [CS]						
Charge current	I_{CS}		-6.0	-5.0	-4.0	μA
Short circuit detection block [SCP]						
Threshold voltage	V_{TH}		0.65	0.70	0.75	V
Input source current	I_{CSCP}		-1.5	-1.0	-0.7	μA
Triangular wave oscillator block [OSC]						
Oscillator frequency	f_{OSC}	CT=100pF, RT=20kΩ	400	500	600	kHz
Frequency stability for voltage	△f /fdv	VCC=1.8V to 7V	-	1	10	%
Frequency stability for temperature	△f /fdt	Ta=-30℃ to 85℃	-	1	-	%
Error amplifier block [Error Amp](CH1~CH4)						
Threshold voltage	V_{TH}	FB=0.9V	0.69	0.70	0.71	V
V_T temperature stability	$\triangle V_T/V_T$	Ta = -30℃ to 85℃	-	0.5	-	%
Input bias current	I_B	IN=0V	-320	-80	-	nA
Voltage gain	A_V	DC	-	100	-	dB

Frequency bandwidth	BW	A_V=0dB	-	10	-	MHz
Output voltage	V_{OH}		1.3	1.4	-	V
	V_{OL}		-	50	200	mV
Output source current	I_{SOURCE}	FB=0.5V	-	-4.0	-1.0	mA
Output sink current	I_{SINK}	FB=0.5V	70	140	-	μA
Short detect comparator [SCP Comp]						
Threshold voltage	V_{TH}	CH1 to CH4	0.8	0.9	1.0	V
Input bias current	I_B	IN=0V	-320	-80	-	nA
PWM Comp. [PWM Comp]						
Threshold voltage(CH4)	V_{T0}	Duty = 0 %	0.25	0.3	-	V
	V_{Tmax}	Duty = 100 %	-	0.75	0.80	V
Threshold voltage(CH1~3)	V_{T0}	Duty = 0 %	0.20	0.25	-	
	V_{Tmax}	Duty = 100 %	-	0.65	0.70	
Input current	I_{DTC}	DTC=0.4V	-1.0	-0.3	-	μA
Output block (CH1,2) [Pin 40,42]						
Output source current	I_{SOURCE}	Duty≧95%, OUT=0V	-	-130	-80	mA
Output sink current	I_{SINK}	Duty≦5%, OUT=5V	65	100	-	mA
Output ON resistor	R_{OH}	OUT = -15mA	-	18	30	Ω
	R_{OL}	OUT = 15mA	-	16	25	Ω
Output block (CH1 to CH3) [Pin 39,41,47]						
Output source current	I_{SOURCE}	Duty≧95%, OUT=0V	-	-130	-80	mA
Output sink current	I_{SINK}	Duty≦5%, OUT=5V	65	100	-	mA
Output ON resistor	R_{OH}	OUT = -15mA	-	18	30	Ω
	R_{OL}	OUT = 15mA	-	16	25	Ω
Output block (CH4) [Pin 48]						
Output source current	I_{SOURCE}	OUT=1/2PVCC	-	-260	-160	mA
Output sink current	I_{SINK}	OUT=1/2PVCV	150	260	-	mA
Output ON resistor	R_{OH}	OUT = -15mA	-	9	15	Ω
	R_{OL}	OUT = 15mA	-	9	15	Ω
Control block [CTL]						
CTL input voltage	V_{IH}	Active mode	1.3	-	7	V
	V_{IL}	Standby mode	0	-	0.8	V
CTL1 to CTL4 input voltage	V_{IH}	Active mode	1.3	-	7	V

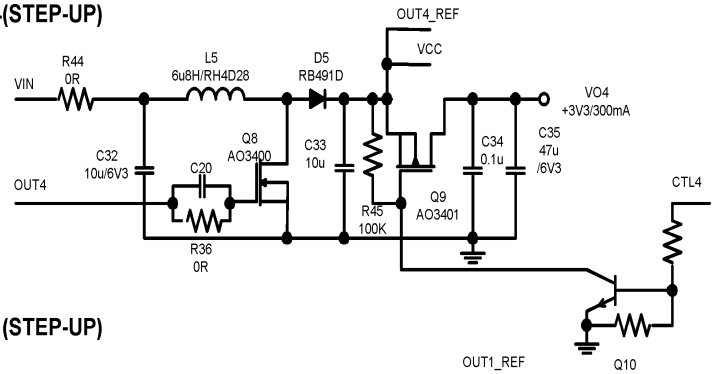
	V_{IL}	Standby mode	0	-	0.8	V
Input current	I_{CTL}	CTL = 5V	-	5	20	μA
Analog gain block [AO,AI]						
AI feedback regulation voltage		$V_{AO}=V_{OUT}$-1.22V	1.20	1.22	1.24	V
AI input common-mode range			-0.1	-	1.3	V
AI input current		V_{AI}=1.32V	-	-	100	nA
AI to AO voltage gain			70	100	140	V/V
AO output sink current		V_{AI}=1V, V_{AO}=2V	0.5	2.5	-	mA
AO output source current		V_{AI}=1.5V, V_{AO}=2V	0.5	2.5	-	mA
ENLD enable	V_{IH}	Active mode	1.2	-	7	V
ENLD disable	V_{IL}	Standby mode	0	-	0.8	V
Low battery detect block [LBI, LBO]						
LBI detect threshold			1.20	1.22	1.24	V
Detect Hysteresis			-50		+50	mV
LBO output voltage low		Isink=1mA	-	-	0.4	V
LBO output high leakage		V_{LBO}=5V	-	0.01	1	μA
General						
Standby current	Icss	CTL=0V	-	-	10	μA
	Icss(o)	CTL=0V CTL1=CTL2=CTL3=CTL4="H"	-	-	10	μA
Power supply current	Icc	CTL=CTL1=CTL2=CTL3=CTL4=ENLD="H"	-	3	6	mA

Typical Application

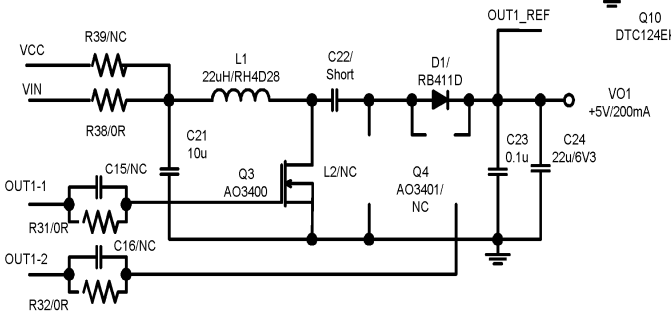
A.



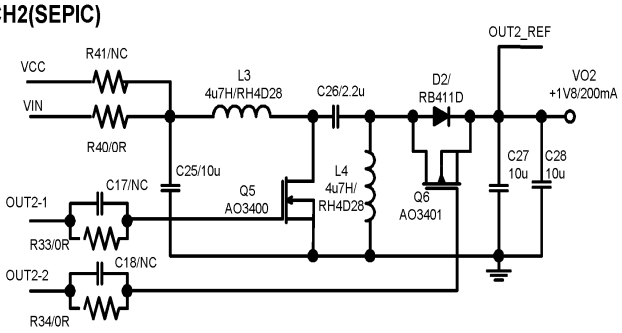
POWER CH4(STEP-UP)



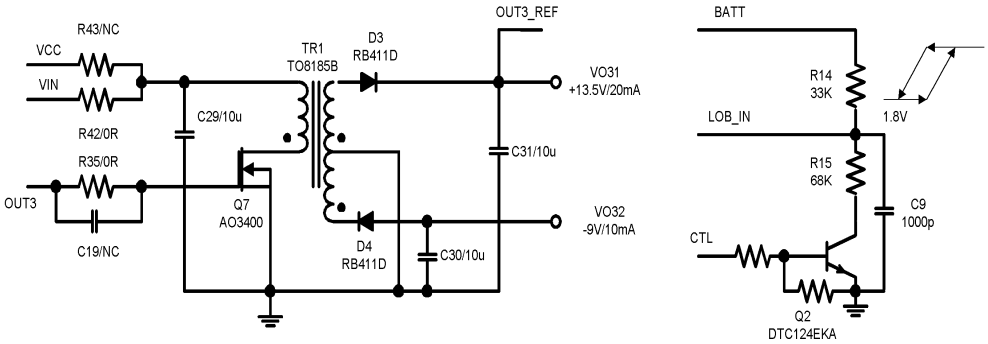
POWER CH1(STEP-UP)



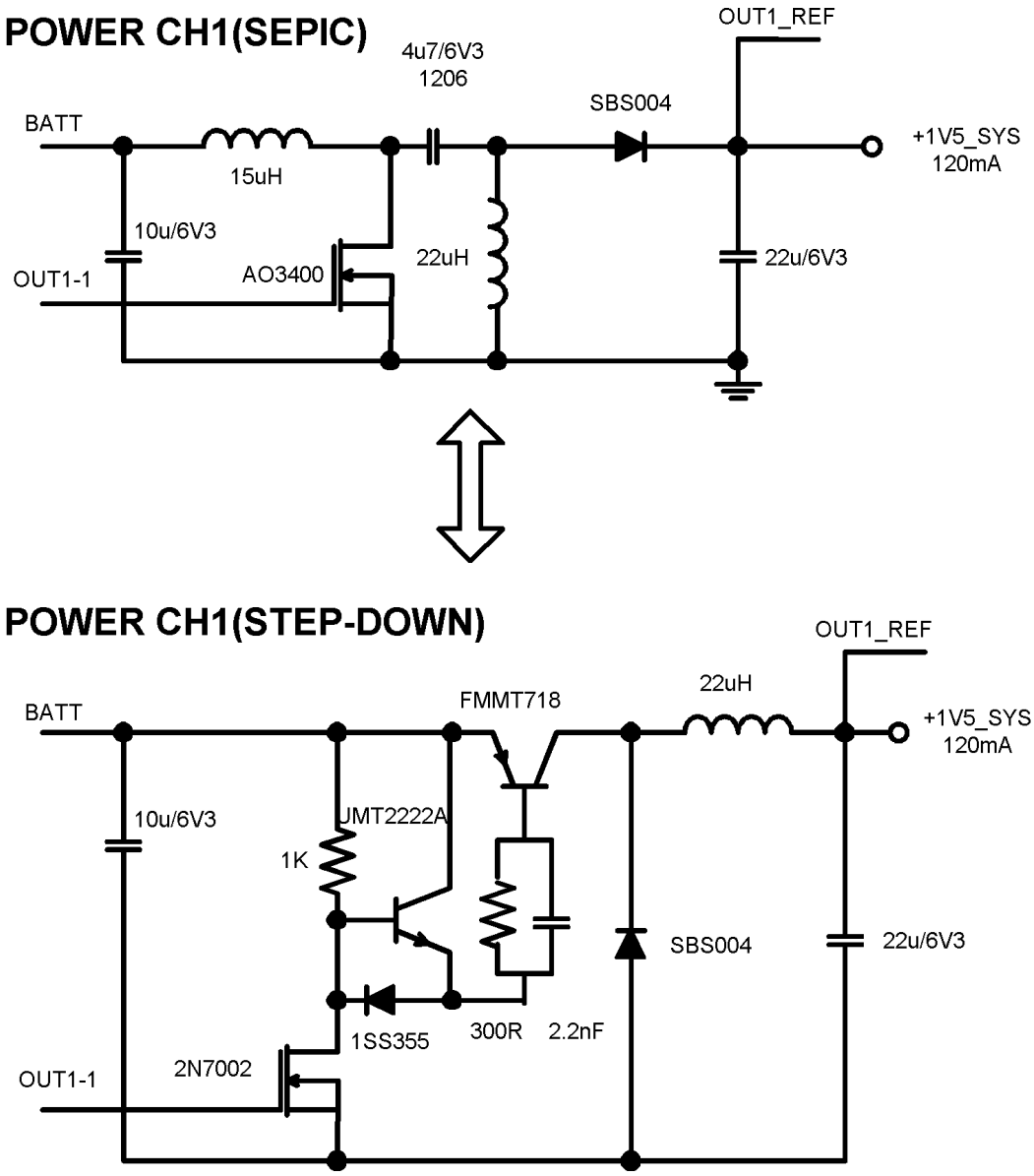
POWER CH2(SEPIC)



POWER CH3(FLYBACK)



B. Using AT1382A on Buck Cnverter



Function Description

1. Power Converter Functions

- **Reference voltage block**
  The reference voltage circuit generates a temperature independence voltage (typical = 0.9V) from the power source, which is used as reference voltage for the IC's internal circuitry and supply load current above 1mA to external device.

- **Triangular oscillator block**
  The triangular wave oscillator is generated by timing resistor (RT) and timing capacitor(CT) to incorporate each other. The waveforms CT (amplitude of 0.3V to 0.7V), CT1 (amplitude 0.25V to 0.65V in phase with CT) and CT2 (amplitude 0.25V to 0.65V in inverse phase with CT) are input to the PWM comparator.

- **Error amplifier block**
  The error amplifier outputs controlling error signal to PWM comparator from sensing DC/DC converter output voltage. In addition , an arbitrary loop gain can be set by connecting feedback resistor and capacitor from the output pin to inverted input pin of the error amplifier, in order to make a stable phase compensation to the system.

- **PWM comparator block**
  The PWM comparator is a voltage-to-pulse width converter for controlling the duty cycle of DC/DC converter.
  Channels 1and 2 main sides, channel 3 and 4 : The comparator keeps the output transistor turn on while the error amplifier output voltage and DTC voltage still higher than the triangular wave voltage.
  Channels 1 and 2 synchronous rectification sides : The comparator keeps the output transistor turn on while the error amplifier output voltage still lower than the triangular wave voltage.

- **Output block**
  The output block is the totem pole configuration , which could drive external MOSFET or transistor.

- **Battery low detect block**
  The AT1382A battery-low comparator open-drain output LBO sinks up to 1mA if the LBI input is below its threshold voltage. Connect LBO to power source with a 100K~1MΩ pullup resistor.

- **Analog gain block**
  The AT1382A analog gain block is a voltage amplifier with a gain of 100 and a push-pull output stage with 2mA drive capability. The analog gain block can be used with an external P-channel MOSFET pass transistor to build a low-dropout linear regulator. Connect ENLD to High to enable the gain block.

2. Channel control function

The channels are turned on and turned off depending on the voltage levels at the CTL, CTL1, CTL2, CTL3 and CTL4. Described as follow.

Voltage level at CTL pin					Channel on / off state			
CTL	CLT1	CLT2	CLT3	CLT4	CH1	CH2	CH3	CH4
L	X	X	X	X	OFF (Standby state)			
H	L	L	L	L	OFF	OFF	OFF	OFF
				H				ON
			H	L			ON	OFF
				H				ON
		H	L	L		ON	OFF	OFF
				H				ON
			H	L			ON	OFF
				H				ON
	H	L	L	L	ON	OFF	OFF	OFF
				H				ON
			H	L			ON	OFF
				H				ON
		H	L	L		ON	OFF	OFF
				H				ON
			H	L			ON	OFF
				H				ON

X：Undefined

3. Protective Functions

- **Short circuit protection and timer latch**

The short circuit detection comparator in each channel detects the output voltage level of power converter. When any channel output voltage falls below the short-circuit detection level, there is a constant current bias charging the external capacitor C_{SCP} which connected to the CSCP pin until the capacitor voltage level reaches about 0.7V then turn off the output transistor and disable the IC. It could reset the actuated protection by restart the power source.

- **Under-voltage lockout protection**

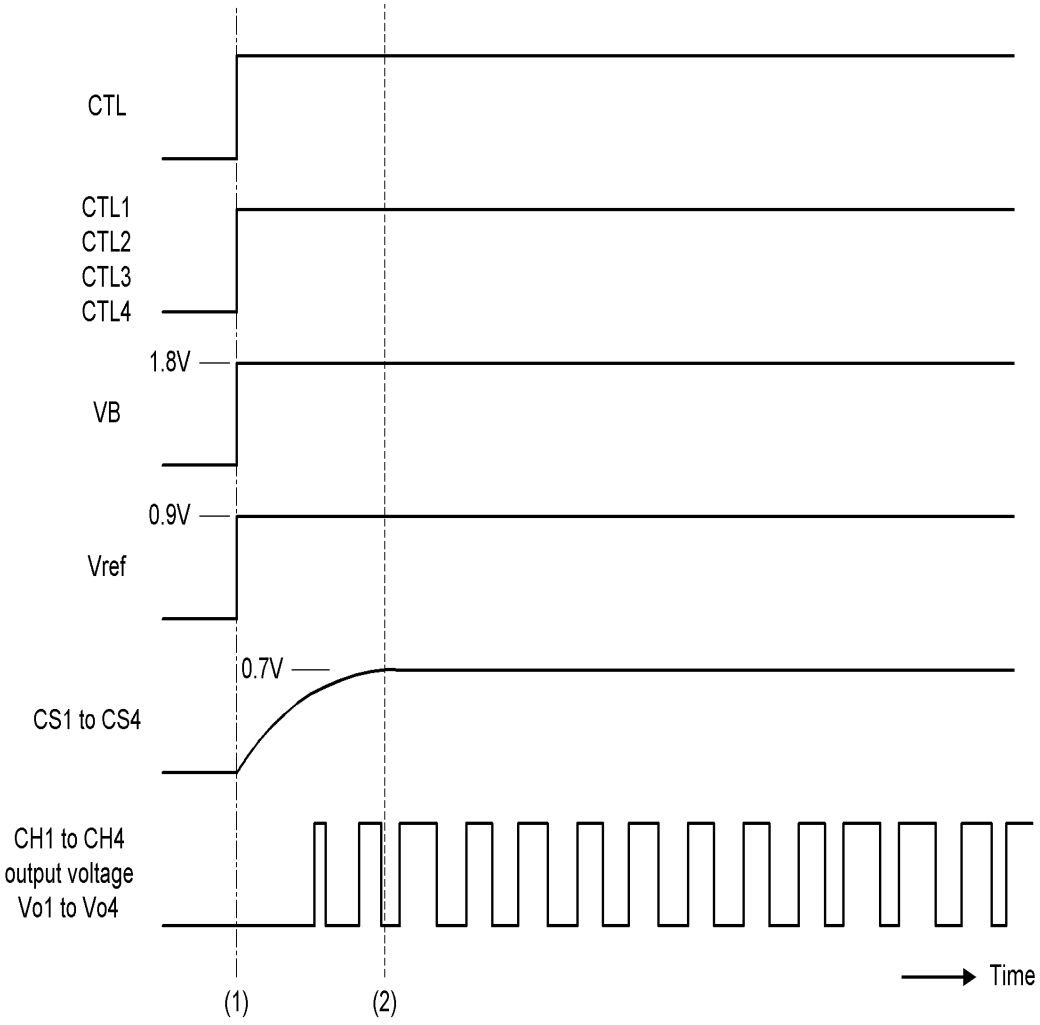
The under-voltage lockout protection is to disable the IC while the supply voltage transient state or momentary decrease, which may cause the IC to malfunction. To prevent such malfunctions, the under-voltage lockout protection circuit detects a decrease in internal reference voltage with respect to the power supply voltage, turns off the output transistor, and sets the dead time to 100% while holding the CSCP pin at the “L” level.

The circuit restores the output transistor to normal when the power source voltage reaches the threshold voltage of the under-voltage lockout protection circuit.

4. Soft Start Operation

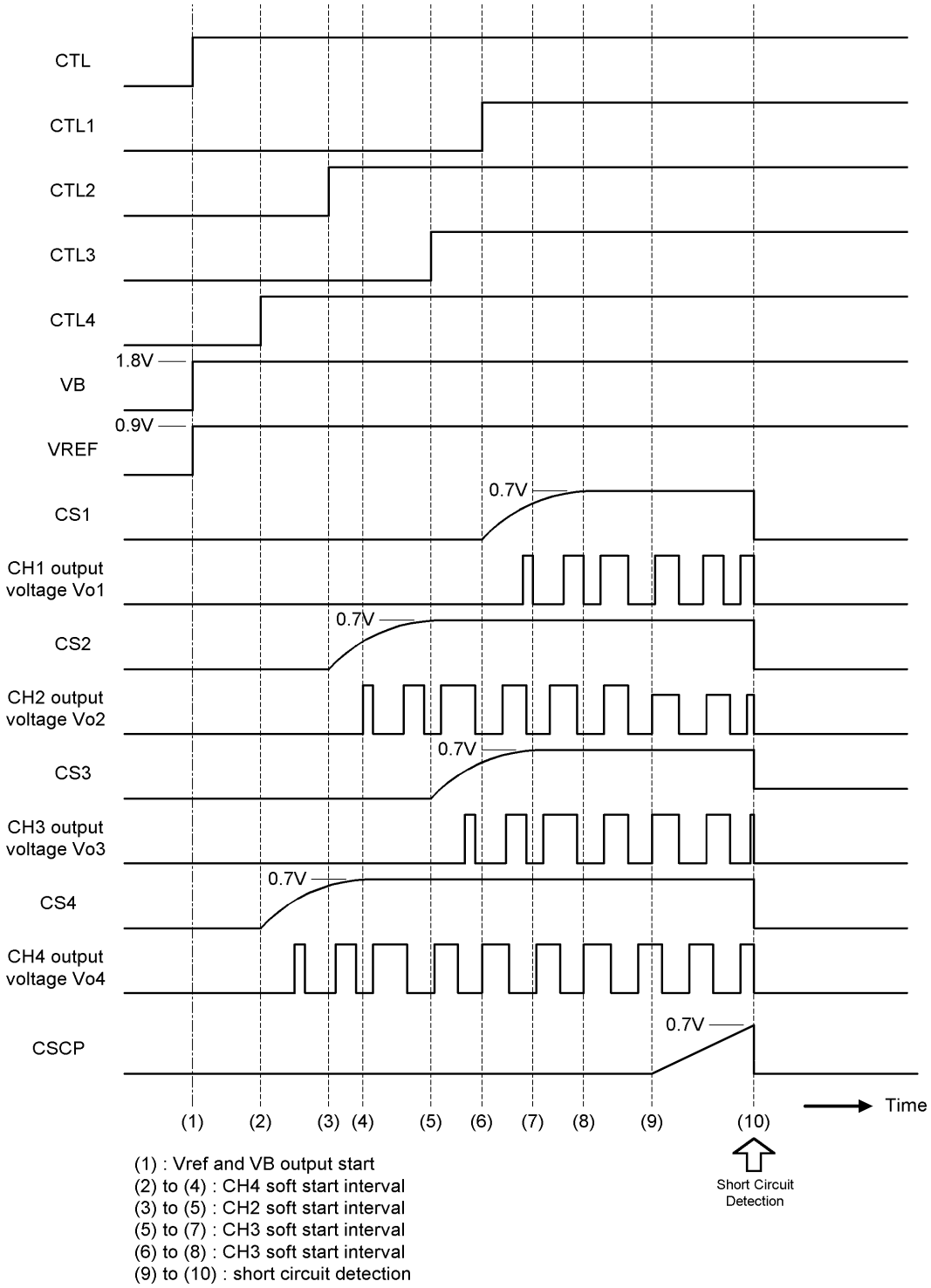
When the CTL , CTL1, CTL2, CTL3 and CTL4 terminals are driven high level at the same time. The driving scheme is described as follow diagram.

The capacitor connected to the CS1,CS2,CS3 and CS4 terminal starts charging and provides a soft start by comparing the CH1 to CH4 output voltage .



(1) to (2) : CH1 to CH4 soft start interval

• When the CTL terminal is switch on, then each of the terminals CTL1, CTL2, CTL3, and CTL4 can be switched on or off independently. Any of the CTL1, CTL2, CTL3 and CTL4 terminals are driven high level. The driving scheme is described as follow diagram.



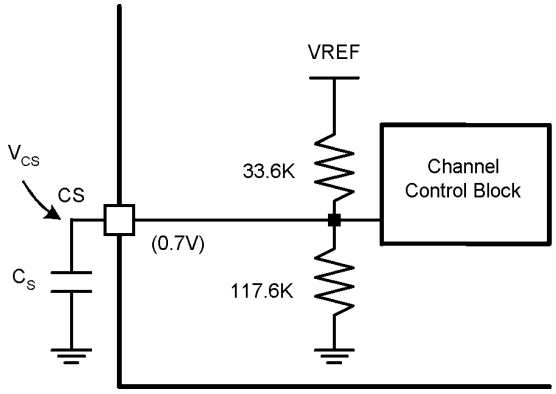
(1) : Vref and VB output start
(2) to (4) : CH4 soft start interval
(3) to (5) : CH2 soft start interval
(5) to (7) : CH3 soft start interval
(6) to (8) : CH3 soft start interval
(9) to (10) : short circuit detection

5. Soft start setting

The soft start operation is determined by the capacitor connected to the CS1~CS4 terminal. Consider the input voltage and load current to design the soft start time.

The soft start time until the DC/DC converter output voltage reaches 95%. It can calculate the soft start time Ts (s).

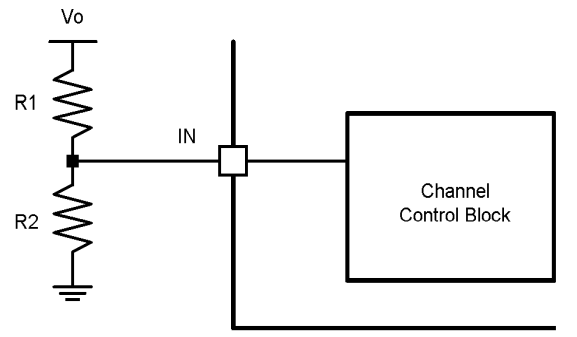
$$Ts\ (s) = 0.084 * C_S\ (\mu F)$$



$$V_{CS} = 0.7 \times (1 - e^{-(\frac{Ts}{R \times Cs})}) \qquad R = \frac{33.6 \times 117.6}{33.6 + 117.6} K\Omega$$

The soft start function of CH1 to CH4 are the same. It could be disabled soft start function by floating CS pin.

6. Setting the output voltage

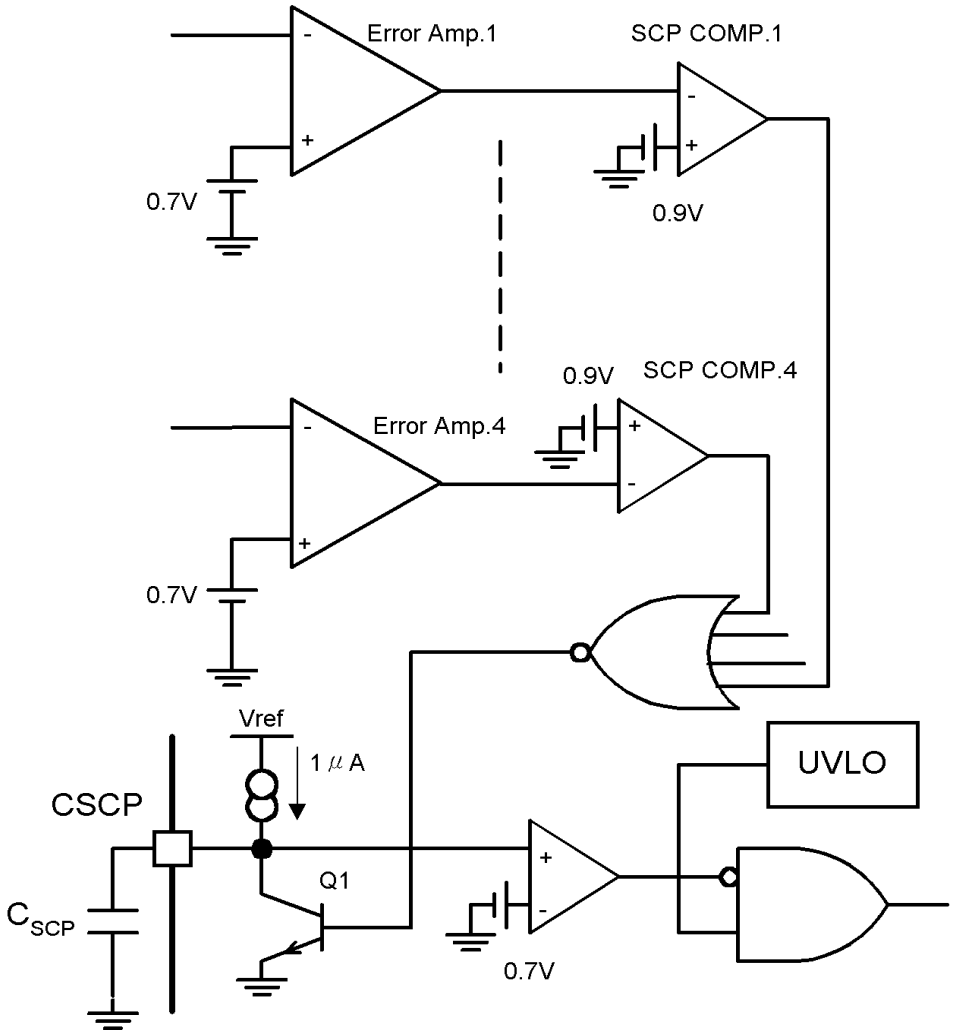


$$Vo = 0.7 \times \frac{R1 + R2}{R2}$$

7. Setting time constant for Time-latch Short-circuit protection

The SCP comparator detects each channel output voltage while the power converter work at normal condition. Q1 is turn on, and the voltage level of CSCP pin is held at low level. If the load of one channel rapidly due to a short of the load, causing the output voltage to drop, the SCP comparator output on that channel goes to "H" level. The transistor Q1 to be turned off and the external capacitor C_{SCP} to be charged at 1.0 μA. The time period of short circuit protection as show below equation.

t_{PE}(s): Short detection time



$$t_{PE}\,(s) = 0.7 * C_{SCP}\,(\mu F)$$

When the C_{SCP} is charged to the 0.7V, the timer-latch is set and output is turn off (dead time is set to 100 %). At this point, the timer-latch is closed and the CSCP terminal is held at "L" level. It could be disabled short circuit protection function by connecting CSCP pin into the ground.

8. Setting the triangular oscillator frequency

The triangular oscillator frequency is determined by the timing capacitor (C_T) connected to the CT terminal, and the timing resistor (R_T) connected to the RT terminal.

$$f_{OSC}(kHz) = \frac{1000000}{C_T(PF) \times R_T(k\Omega)}$$

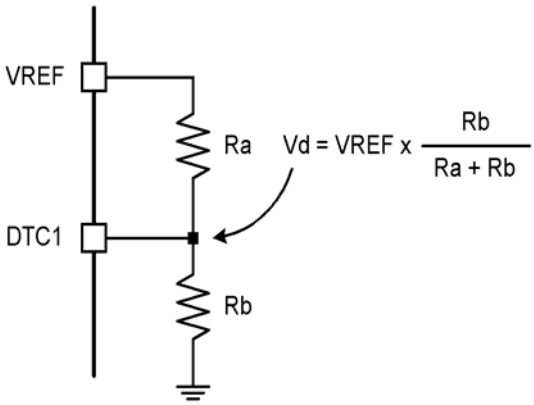
9. Setting the DEAD time

When using step up or SEPIC or flyback DC/DC converter, it must prevent that output transistor works at full-ON state (ON duty = 100%). To prevent this situation, set the maximum duty of these channels. To set it, set the voltage at the DTC terminal by applying a resistive voltage divider to the VREF as shown below.

When the voltage at the DTC pin is higher than the triangular wave voltage (CT), the output transistor is turned on. The maximum duty calculation formula assuming that triangular wave amplitude = ΔV1(CH4=0.45,CH1~3=0.4) and triangular wave minimum voltage = Vx (CH4=0.3,CH1~3=0.25).

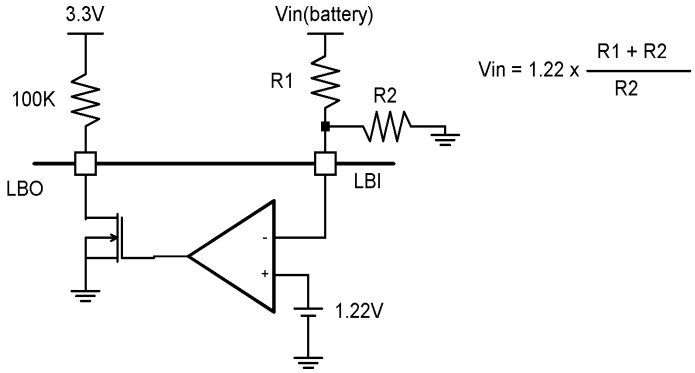
$$DUTY(ON)\max = \frac{Vd - Vx}{\Delta V1} \times 100\%$$

If don't setting maximum duty, connect DTC terminal directly to the VREF terminal.

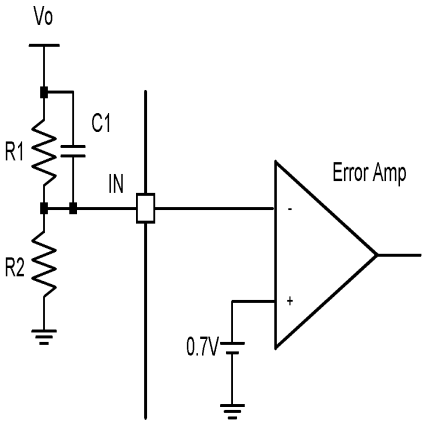


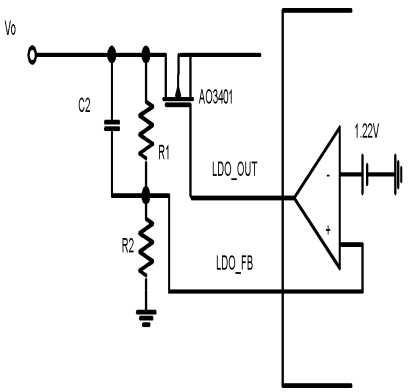
10. Setting low battery detector threshold voltage

The low battery detected threshold voltage is determined by the external resistor connected to the LBI terminal. If Vin (battery voltage) under setting threshold voltage, low battery detect output terminal (LBO) is hold at "L" level. The driving scheme is described as follow diagram.

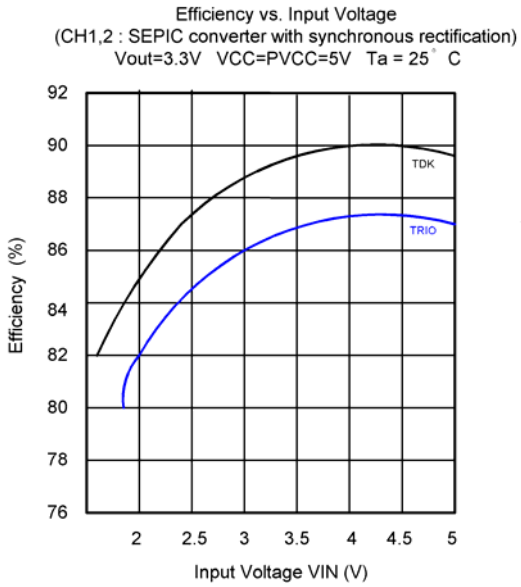


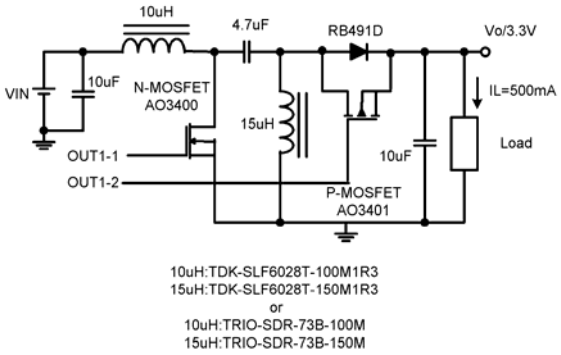
11. Decrease the Output Overshoot

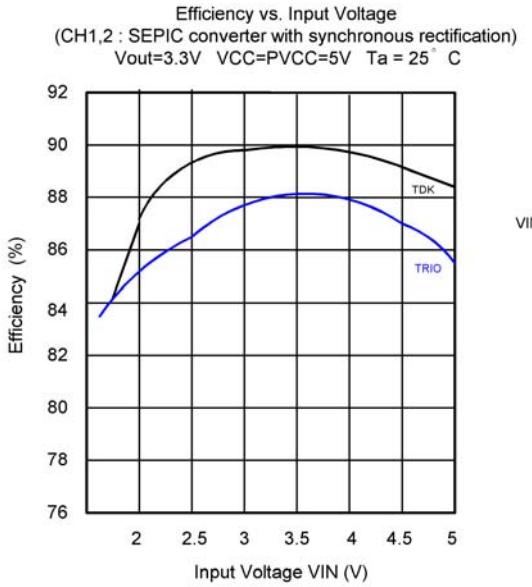


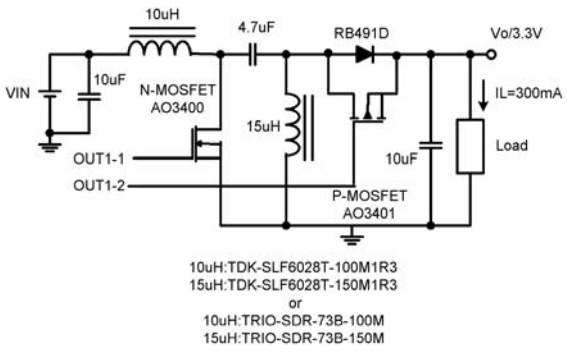


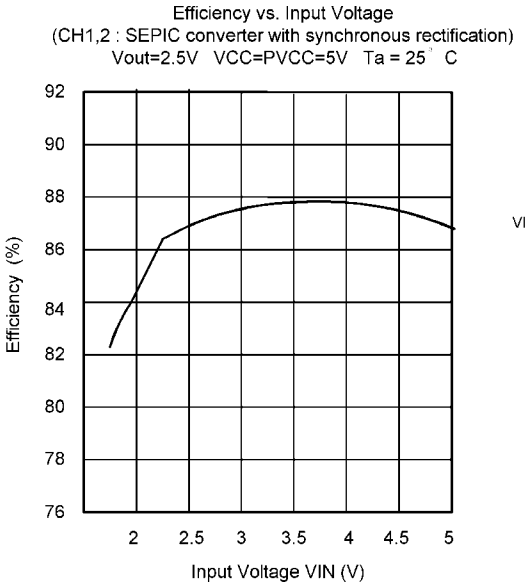
Synchronous Rectification Reference Data

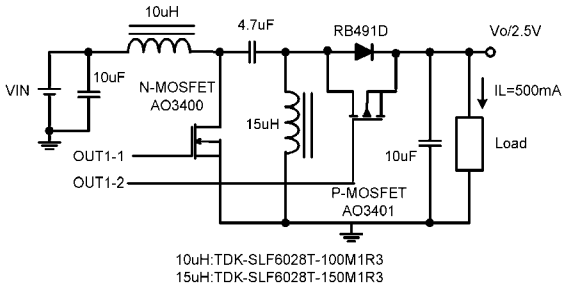


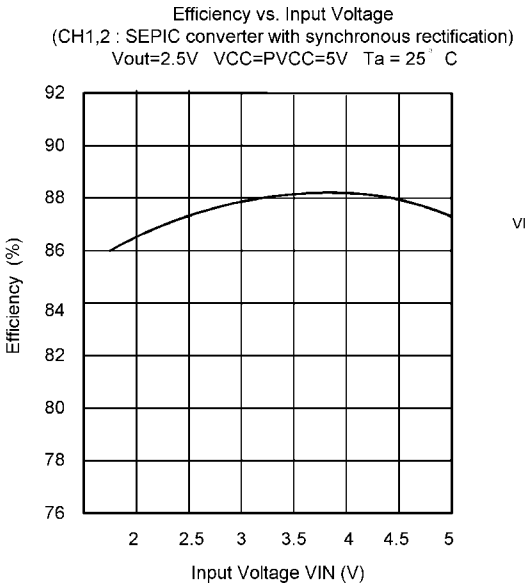







Efficiency vs. Input Voltage
(CH1,2 : SEPIC converter with synchronous rectification)
Vout=2.5V VCC=PVCC=5V Ta = 25° C
Efficiency (%)
92
90
88
86
84
82
80
78
76
2
2.5
3
3.5
4
4.5
5
Input Voltage VIN (V)


10uH
4.7uF
RB491D
Vo/2.5V
VIN
10uF
N-MOSFET
AO3400
15uH
IL=500mA
Load
OUT1-1
OUT1-2
10uF
P-MOSFET
AO3401
10uH:TDK-SLF6028T-100M1R3
15uH:TDK-SLF6028T-150M1R3


Efficiency vs. Input Voltage
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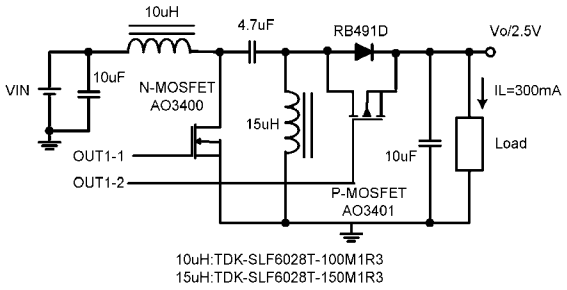
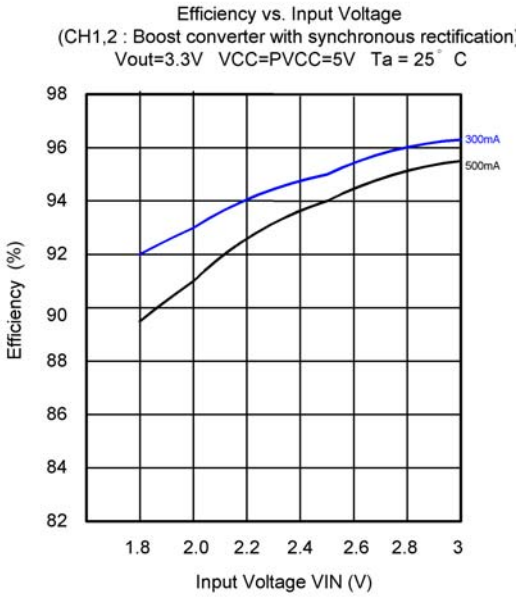
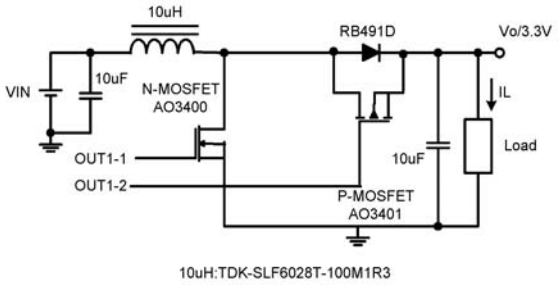
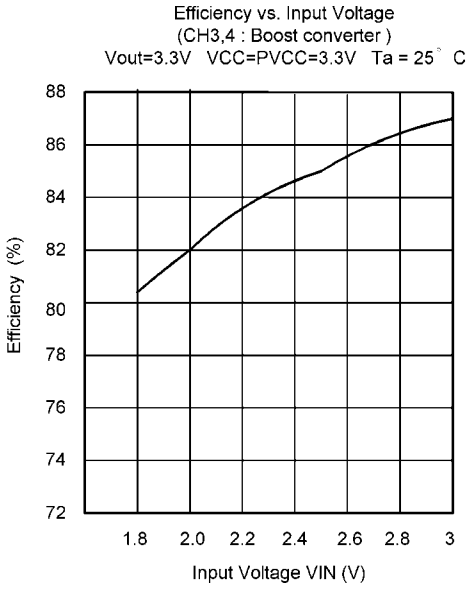
Input Voltage VIN (V)

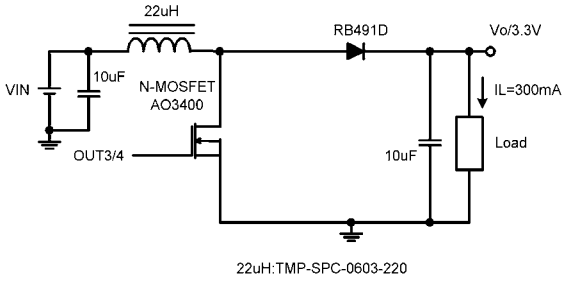

10uH
4.7uF
RB491D
Vo/2.5V
VIN
10uF
N-MOSFET
AO3400
15uH
IL=300mA
Load
OUT1-1
OUT1-2
10uF
P-MOSFET
AO3401
10uH:TDK-SLF6028T-100M1R3
15uH:TDK-SLF6028T-150M1R3





10uH:TDK-SLF6028T-100M1R3



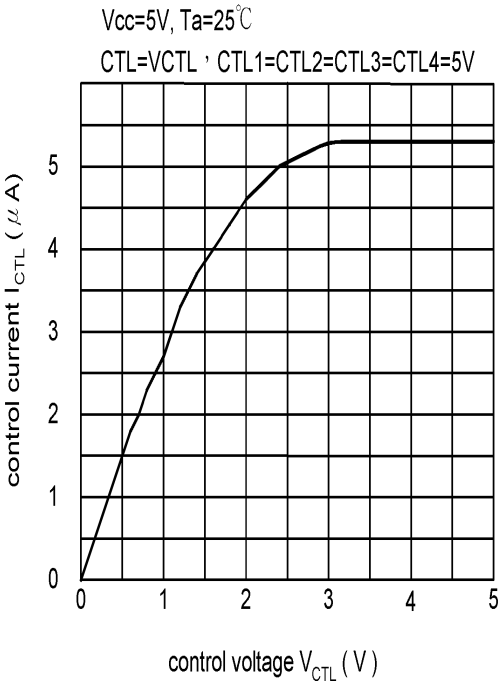


22uH:TMP-SPC-0603-220

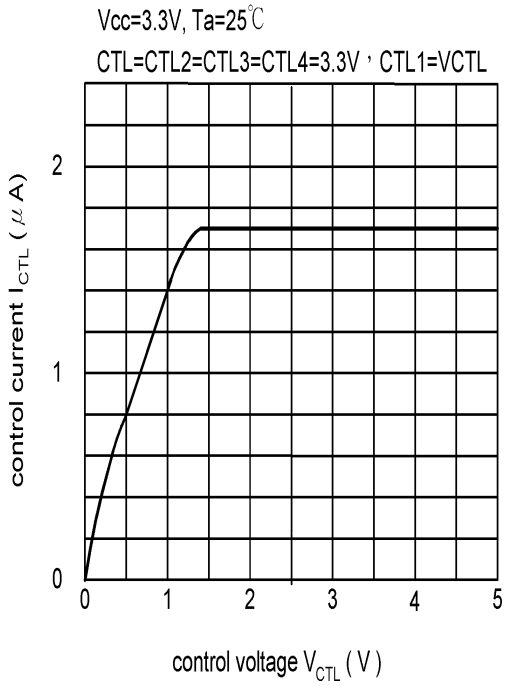
***if VCC=PVCC=3.3V, the efficiency will decrease about 0.2~05 % because of the N-MOSFET AO3400 Rds(on) increase.**

Typical Characteristics

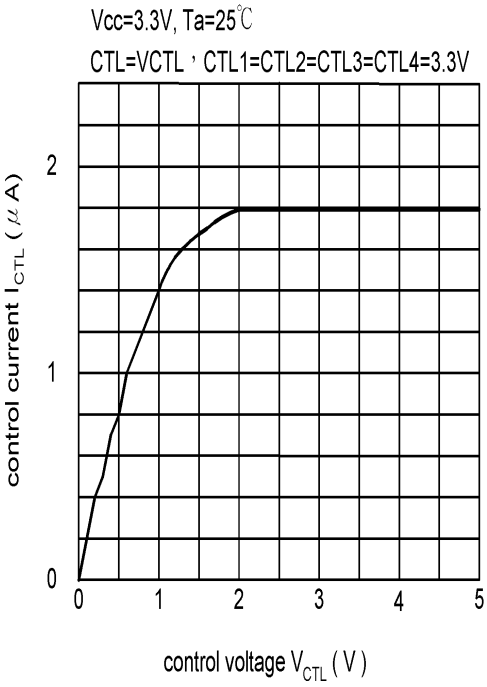
control voltage vs. control current (CTL)



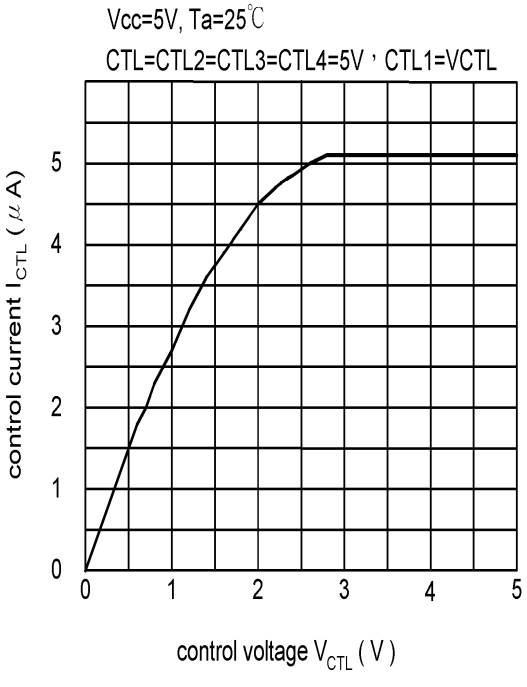
control voltage vs. control current (CTL1-CTL4)



control voltage vs. control current (CTL)

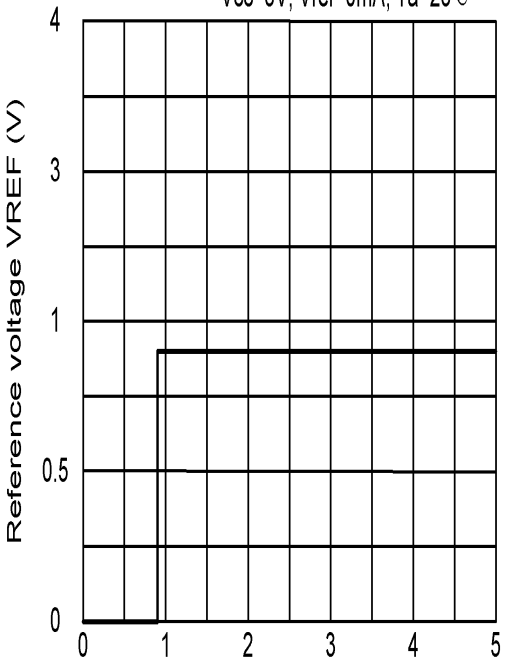


control voltage vs. control current (CTL1-CTL4)



Reference voltage vs. control voltage

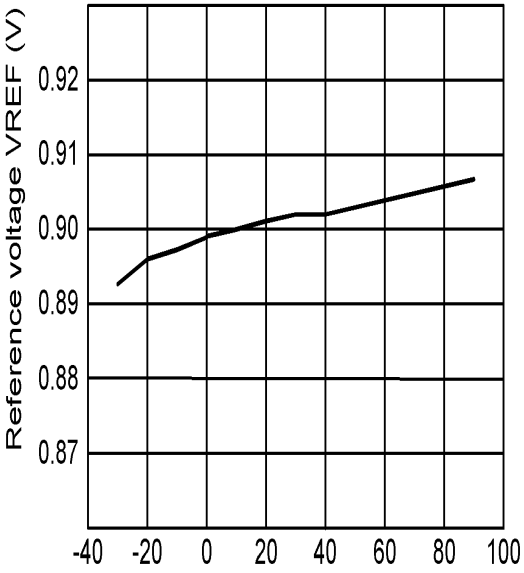
Vcc=5V, Vref=0mA, Ta=25℃



Reference voltage vs. Ambient temperature

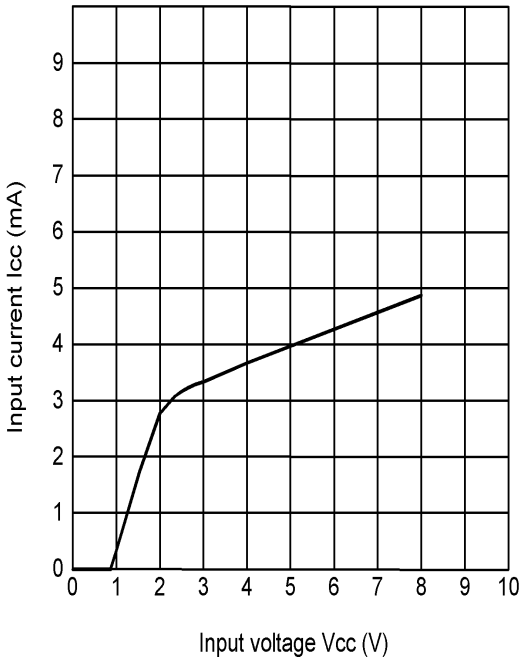
Vcc=5V, Vref=0mA

CTL=5V, CTL1=CTL2=CTL3=CTL4=0V



Input current vs. Input voltage

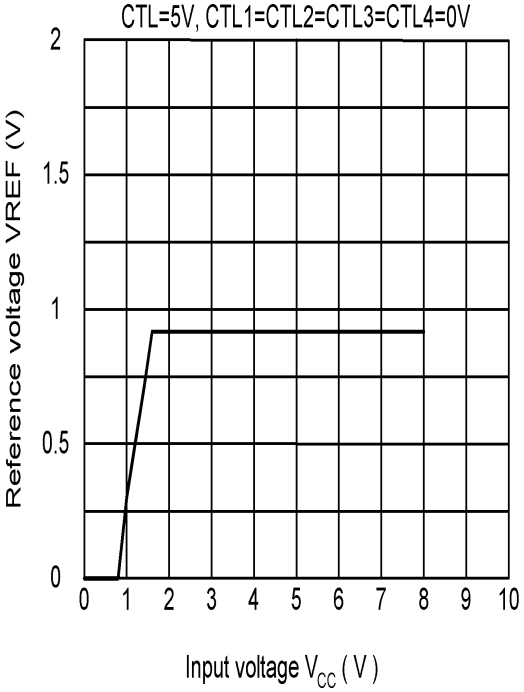
(CTL=5V, CTL1=CTL2=CTL3=CTL4=0V Ta = 25 ° C)



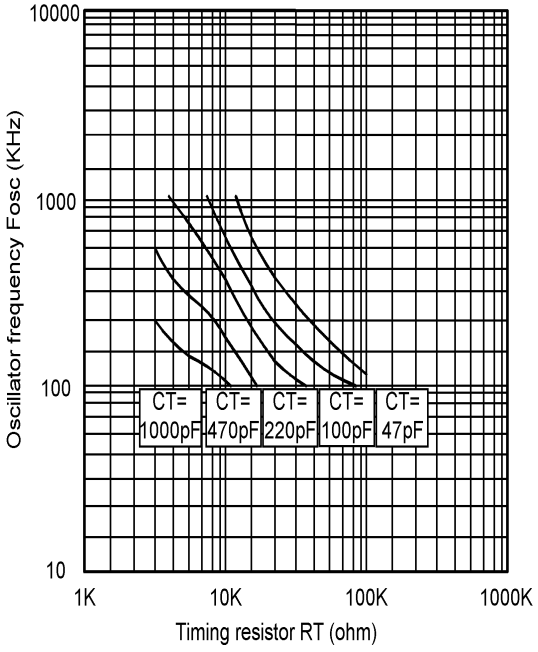
Reference voltage vs. Input voltage

Ta=25℃, Vref=0mA

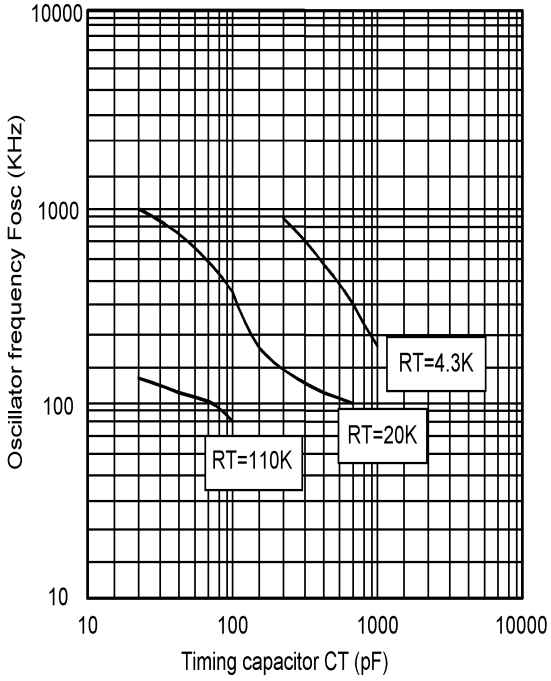
CTL=5V, CTL1=CTL2=CTL3=CTL4=0V



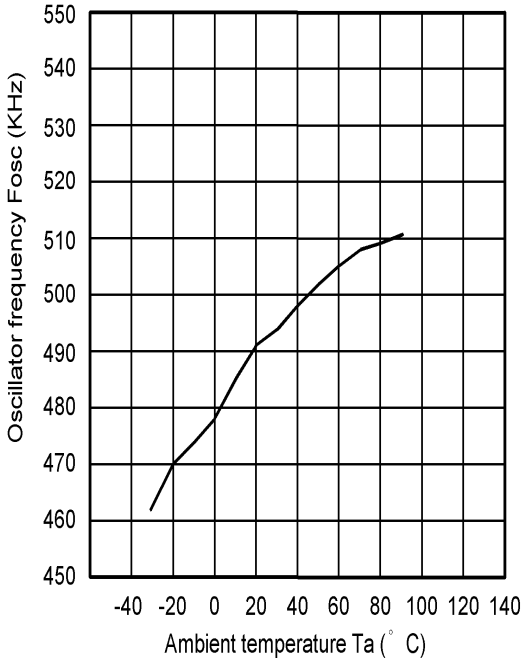
Oscillatro frequency vs. Timing capacitor
(VCC=5V Ta=25° C)



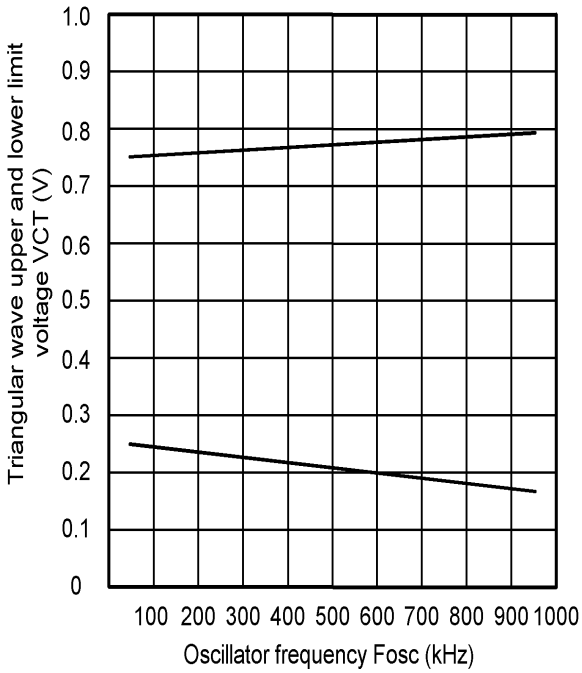
Oscillatro frequency vs. Timing capacitor
(VCC=5V Ta=25° C)



Oscillatro frequency vs. Ambient temperature
(VCC=5V RT=20k ohm CT=100pF
CTL=5V, CTL1=CTL2=CTL3=CTL4=0V)



Triangular wave upper and lower limit voltage vs.
Oscillator frequency
(VCC=5V RT=20k ohm Ta=25° C)



2F, No.10, Prosperity RD. II, Science-Based Industrial Park, Hsinchu 300,Taiwan, R.O.C.
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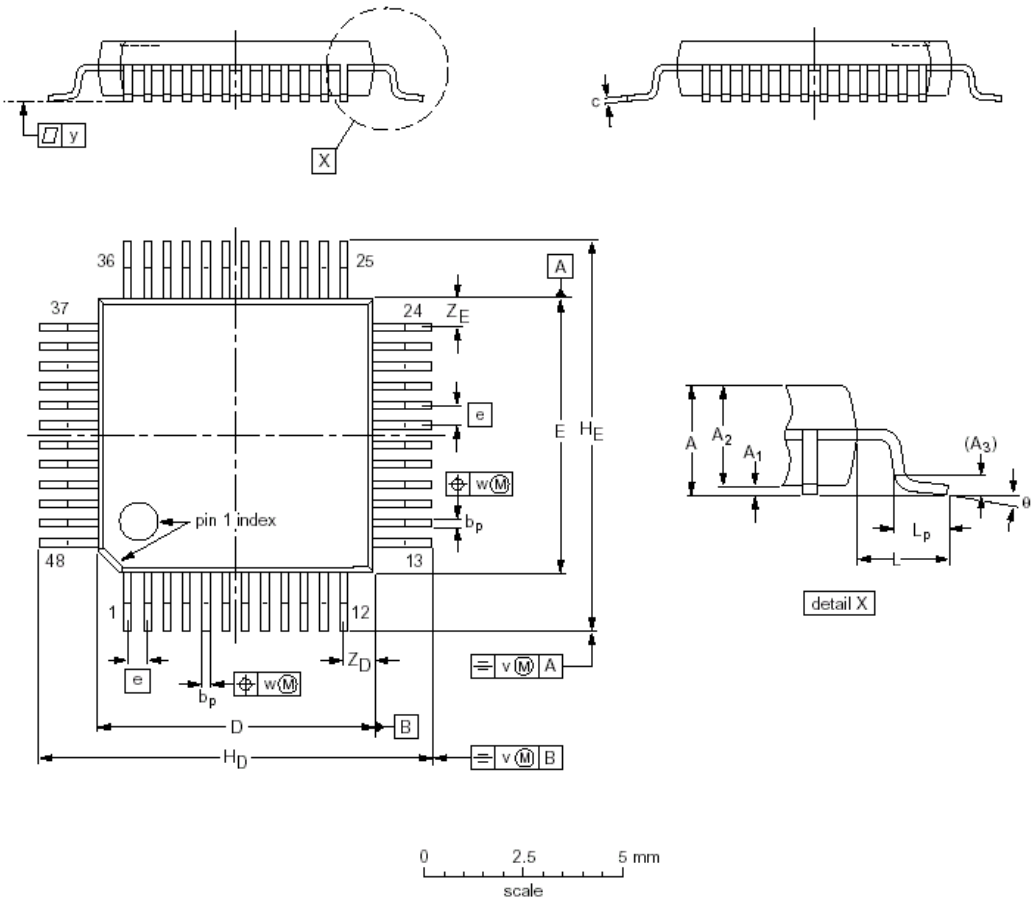
WWW: http://www.aimtron.com.tw
Email: service@aimtron.com.tw

Package Outline: LQFP48

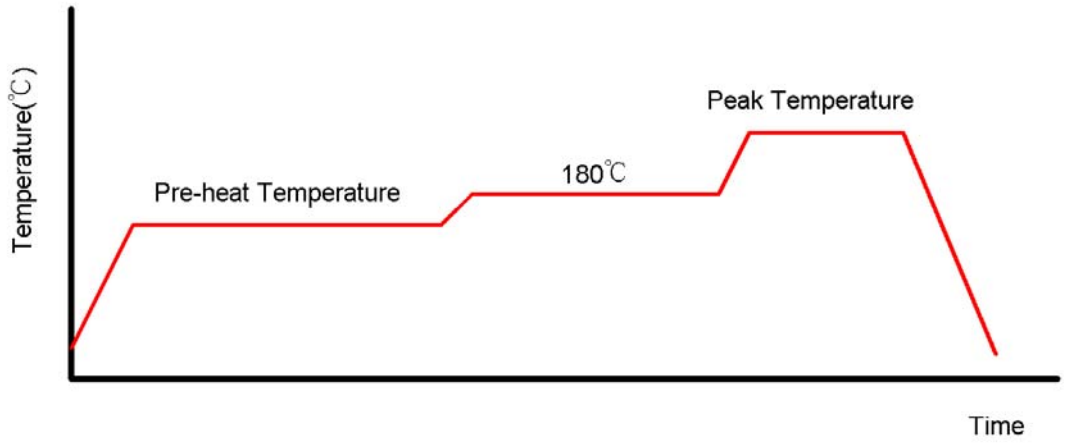


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A



Classification Reflow Profiles

	Convection or IR/Convction	VPR
Average Heating Rate(180°C to peak)	5°C/second max.	10°C/second max.
Preheat Temperature(125±20°C)	120 seconds max.	
Temperature maintained above 180°C	10~150 seconds	
Time within 5°C of actual Peak Temperature	10~20 seconds	60 seconds
Peak Temperature Range(Note 1)	219~225°C or 235~240°C	219~225°C or 235~240°C
Cooling Rate	6°C /second max.	10°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	

*1 The maximum peak temperatures for IR and VP reflow are depending on package dimensions.

Package Reflow Conditions

Pkg. Thickness ≥2.5mm and all bags	Pkg. Thickness <2.5mm and Pkg. Volume ≥350 mm^3	Pkg. Thickness <2.5mm and Pkg. Volume <350 mm^3
Convection 219~225°C		Convection 235~240°C
VPR 219~225°C		VPR 235~240°C
IR/Convection 219~225°C		IR/Convection 235~240°C