MicroConverter™, Multi-Channel 12 bit ADC with Embedded MCU

Preliminary Technical Data — ADuC812

FEATURES

ANALOG I/O
- 8 Channel, true 12 bit ADC
- Self Calibrating
- High Speed 200 kSPS
- On-chip DMA Controller for auto-capture
- Dual 12-bit Voltage DAC's
- On-chip temperature sensor function

MEMORY
- 8K Bytes On-Chip Program Flash EEPROM
- 640 Bytes On-Chip Data Flash EEPROM
- 256 Bytes On-Chip Data RAM
- 16M Bytes Ext. Data Address Space
- 64K Bytes Ext. Program Address Space

8051 BASED CORE
- 8051 Compatible Instruction Set
- 12 MHz Nominal Operation
- Three 16 bit Timer/Counters
- 24 Programmable I/O lines
- 8 Programmable Input lines
- Nine interrupt sources, two priority levels

POWER
- Specified for 3V and 5V operation
- Normal, Sleep and Powerdown Modes

On-Chip PERIPHERALS
- UART Serial I/O
- 2 Wire(I2C® Compatible) and SPI® Serial I/O
- Watchdog Timer and Power Supply Monitor

GENERAL DESCRIPTION

The ADuC812 is a fully integrated 12 bit data acquisition system incorporating a high performance self calibrating multi-channel ADC, dual DACs and programmable 8 bit MCU (8051 instruction set compatible) on a single chip.

8K bytes FLASH program memory with memory security lock features, 640 bytes FLASH user memory and 256 bytes RAM are also incorporated On-Chip.

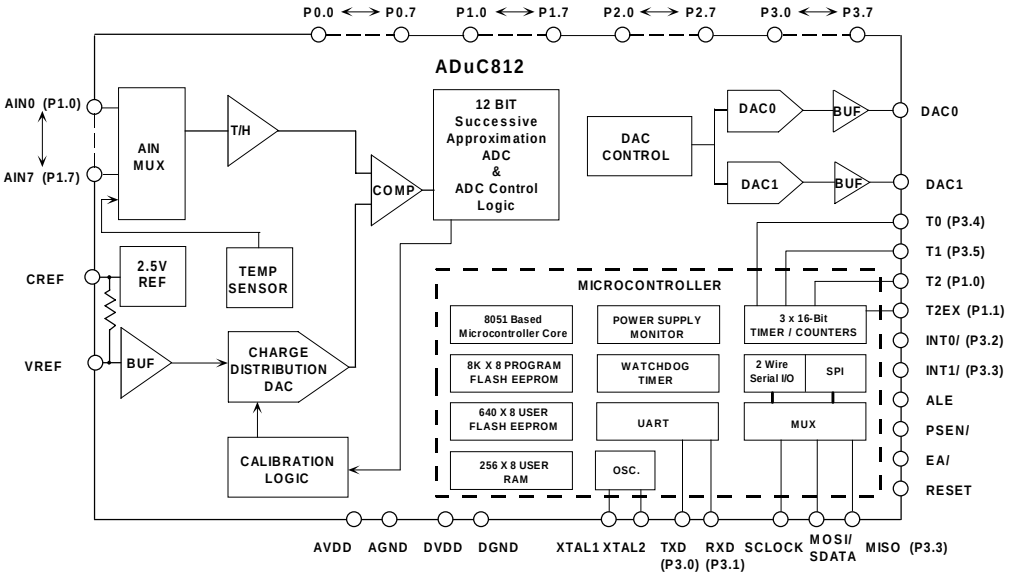
Additional MCU support functions include Watchdog Timer, Power Supply Monitor and ADC DMA functions. 24 Programmable I/O lines, 8 input only lines, I2C compatible, SPI and Standard UART Serial Port I/O are provided for multi-processor interfaces and I/O expansion.

Static CPU operation, sleep and powerdown modes for the converters allow power management for low power applications. The part is available in 52 pin, plastic quad flatpack package (PQFP).

APPLICATIONS

Intelligent Sensor calibration and conditioning
Battery Powered Systems (Portable PCs, Instruments, Monitors)
Transient Capture Systems
DAS and Communications Systems

FUNCTIONAL BLOCK DIAGRAM



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® SPI is a Registered Trademark of Motorola Inc.
® I2C is a Registered Trademark of Philips Semiconductors Inc.

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ADuC812 ARCHITECTURE, MAIN FEATURES

The ADuC812 is a highly integrated true 12-bit data acquisition system. At its core, the ADuC812 incorporates a high performance 8 bit MCU (8051 Instruction Set Compatible) with on-chip reprogrammable non-volatile Flash program memory controlling a multi-channel (8 input channels on 52PQFP), true 12-bit ADC.

The chip incorporates all secondary functions to fully support the programmable data acquisition core. These secondary functions include User data Flash memory, Watchdog Timer (WDT), Power Supply Monitor (PSM) and various industry standard parallel and serial interfaces.

ADuC812 MEMORY ORGANIZATION

As with all 8051 related devices, the ADuC812 has separate address spaces for Program and Data memory as shown in Figure 1. As shown in Figure 1, an additional 640 Bytes of Flash EEPROM are also available to the user and are accessed indirectly via a group of control registers mapped in the Special Function Register (SFR) area in the Data Memory Space.

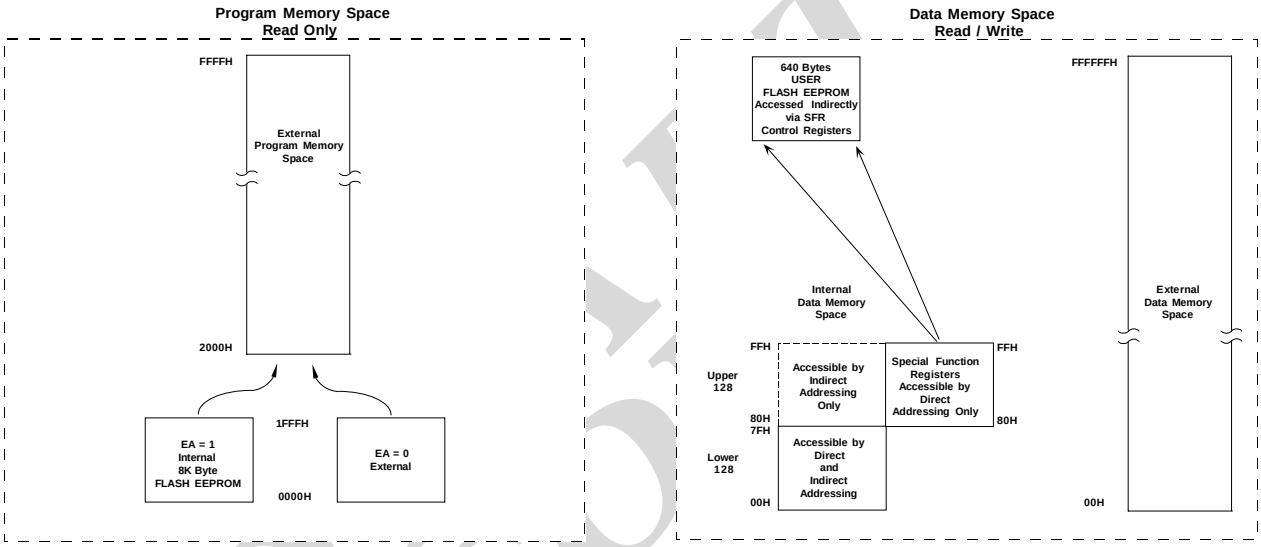


Figure 1. ADuC812 Program and Data Memory Maps

The lower 128 bytes of internal data memory are mapped as shown in Figure 2. The lowest 32 bytes are grouped into 4 banks of 8 registers addressed as R0 through R7. The next 16 bytes (128 bits) above the register banks form a block of bit addressable memory space at bit addresses 00H through 7FH.

The SFR space is mapped in the upper 128 bytes of internal data memory space. The SFR area is accessed by direct addressing only and provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the ADuC812 via the SFR area is shown in Figure 3.

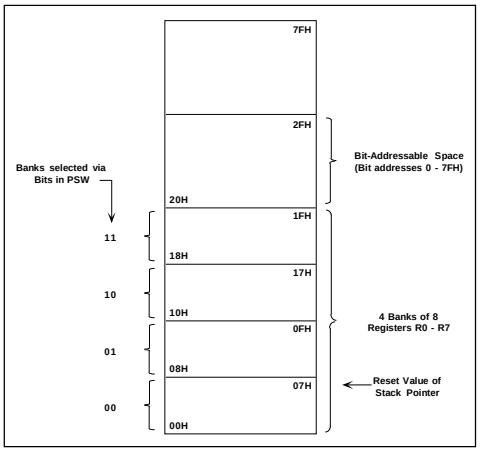


Figure 2. Lower 128 Bytes of Internal RAM

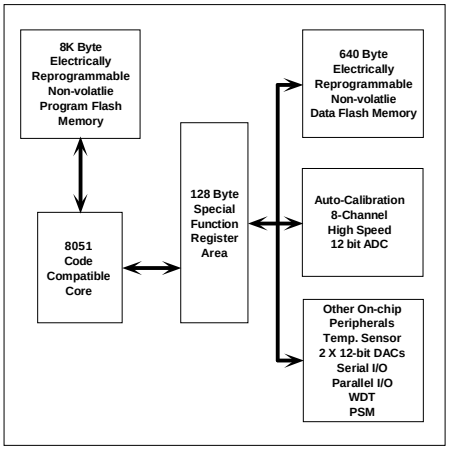


Figure 3. ADuC812 Programming Model.

ADC CIRCUIT INFORMATION

General Overview

The ADC conversion block incorporates a fast, multi-channel, 12-bit, single supply A/D converter. This block provides the user with multi-channel mux, track/hold, on-chip reference, calibration features and A/D converter. All components in this block are easily configured via the SFR interface from the core MCU.

The A/D converter section in this block consists of a conventional successive-approximation converter based around a capacitor DAC. The converter accepts an analog input range of 0 to $+V_{REF}$. A high precision, low drift 2.5V reference is provided on-chip. The internal reference may be overdriven via the external V_{REF} pin. This external reference can be in the range 2.3V to AV_{DD}.

Single step or continuous conversion modes can be initiated in software or alternatively by applying a convert signal to the an external pin. Timer 2 can also be configured to generate a repetitive trigger for ADC conversions. The ADC may also be configured to operate in a DMA Mode whereby the ADC block continuously converts and captures samples without any interaction from the MCU core.

The ADC core contains self-calibration and system calibration options to ensure accurate operation over time and temperature. A voltage output from an On-Chip bandgap reference proportional to absolute temperature can also be routed through the front-end ADC multiplexor facilitating a temperature sensor implementation.

Transfer Function

The analog input range for the ADC is 0 V to V_{REF}. For this range, the designed code transitions occur mid-way between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS –3/2 LSBs). The output coding is straight binary with 1 LSB = FS/4096 or 2.5 V/4096 = 0.61 mV when V_{REF} = 2.5 V. The ideal input/output transfer characteristic for the 0 to V_{REF} range is shown in Figure 8.

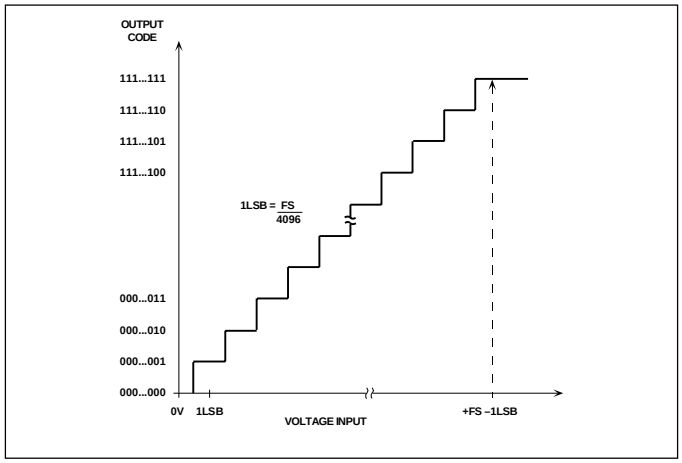


Figure 8. ADuC812 ADC Transfer Function

SFR Interface to ADC Block

The ADC operation is fully controlled via 3 SFR's, namely :

ADCCON1 - Controls acquisition and conversion times and powerdown modes as detailed in Figure 9.

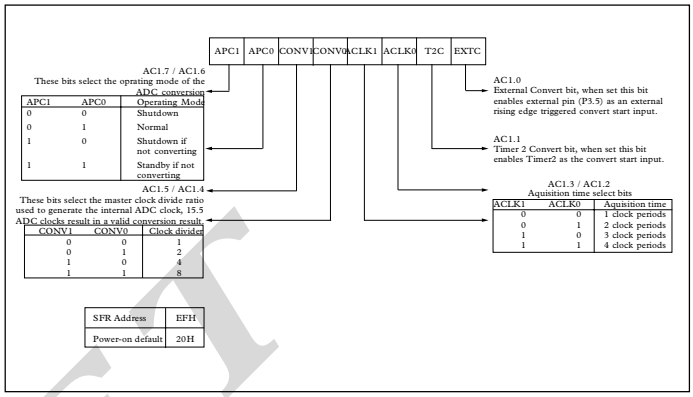


Figure 9. ADCCON1 SFR bit designations

ADCCON2 - Controls channel selection and conversion modes as detailed in Figure 10.

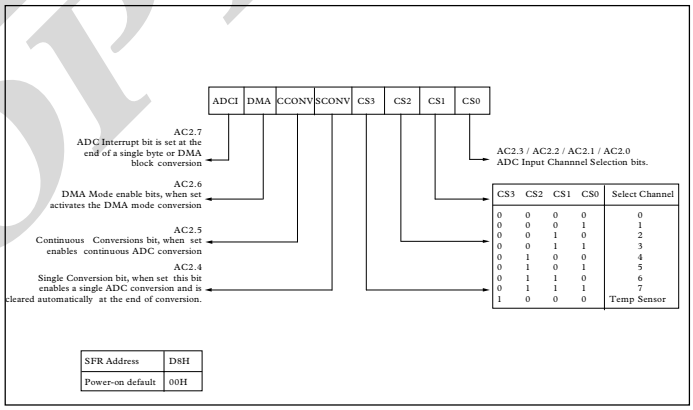


Figure 10. ADCCON2 SFR bit designations

ADCCON3 - Controls user calibration options and Busy status as detailed in Figure 11.

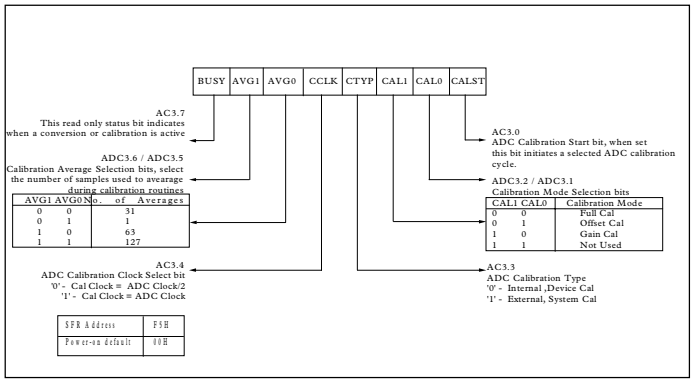


Figure 11. ADCCON3 SFR bit designations

NON-VOLATILE FLASH MEMORY

Flash Memory Overview

The ADuC812 incorporates Flash memory technology on-chip to provide the user with a non-volatile, in-circuit reprogrammable, code and data memory space.

Flash memory is the newest type of non-volatile memory technology and is based on a single transistor cell architecture. This technology is basically an outgrowth of EPROM technology and was developed through the late 1980's.

Flash memory takes the flexible in-circuit reprogrammable features of EEPROM and combines them with the space efficient/density features of EPROM (see Figure 16).

Like EEPROM, Flash memory can be programmed in system at a byte level, although it must be erased first; the erasure being performed in sector blocks (the ADuC812 incorporates the erase cycle into the program cycle thus making this operation transparent to a user accessing the data memory array).

Because Flash technology is based on a single transistor cell architecture, a Flash memory array, like EPROM can be implemented to achieve the space efficiencies or memory densities required by a given design.

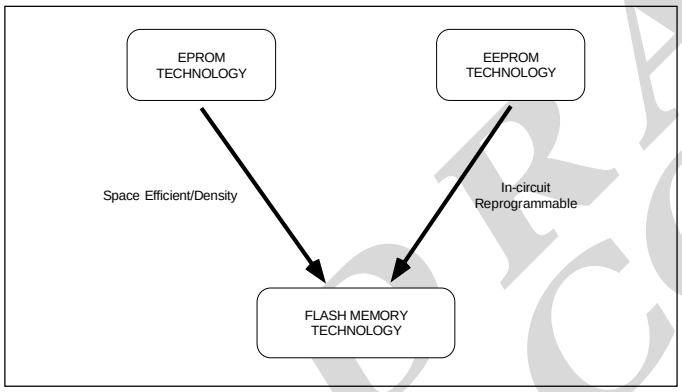


Figure 16. Flash Memory Development

Overall, Flash memory represents a step closer towards the ideal memory device that includes non-volatility, in-circuit programmability, high density and low cost. Incorporated in the ADuC812, Flash memory technology allows the user to update program code in circuit without the need to replace one time programmable (OTP) devices at remote operating nodes.

Flash Memory and the ADuC812

The ADuC812 provides 2 arrays of Flash memory for user applications.

8K bytes of program code space are provided on chip to facilitate program execution without any external discrete ROM device requirements. The Program memory can be programmed using conventional third party memory programmers. This array can also be programmed in-circuit, using the serial download mode provided.

A 640 Byte Data Flash memory space is also provided on-chip. This may be used by the user as a general purpose non-volatile scratchpad area. User access to this area is via a group of 6 SFR's. This space can be programmed at a byte level, although it must first be erased in 4 byte sectors.

ADuC812 Flash Memory Security Features

The ADuC812 provides comprehensive on-chip security features which may be used in any application where free access to the program memory space may be at issue.

Lock Mode : This mode locks code in memory allowing it to be verified but disabling programming unless the full program space is first erased.

Secure Mode : This mode locks code in memory and disables verification and programming unless the full program space is first erased.

Serial Safe Mode : This mode disables serial download mode on the device unless the full program space is first erased.

ADuC812 Flash, Program Memory

The ADuC812 also incorporates 8K Bytes of User program Flash memory. This program memory array is mapped into the lower 8K bytes of the 64K Bytes program space on the ADuC812 and will be used to hold user code in typical applications.

The program memory array can be programmed in one of two modes, namely :

Parallel Programming :

The parallel programming mode is fully compatible with conventional third party Flash or EEPROM device programmers. In this mode Ports P0, P1 and P2 operate as the external data and address bus interface, ALE operates as the Write Enable strobe and Port P3 is used as a general configuration port which configures the device for various program and erase operations during parallel programming. The high voltage (12V) supply required for Flash programming is generated using On-Chip charge pumps to supply the high voltage program lines.

Serial Downloading (In Circuit Programming) :

As part of its factory boot code, the ADuC812 facilitates serial code download via the standard UART serial port. Serial download mode is entered automatically on power-up if the external pin, $\overline{\text{PSEN}}$ is pulled low . Once configured the user can download code to the program memory array while the device is sited in its target application hardware. PC serial download code is provided as part of the ADuC812 development system.

ON-CHIP PERIPHERALS

The sections below give a brief overview of the various secondary peripherals also available on-chip.

2 X 12-Bit DAC's

The ADuC812 incorporates two 12-bit DACs On-Chip. DAC operation is controlled via three special function registers.

In normal mode of operation, each DAC is updated when the low DAC byte (DACxL) SFR is written. Both DACs can be updated simultaneously using the SYNC bit in the DACCON SFR. The DAC's can operate in 12 or 8-bit modes and have programmable output ranges of 0 -> 2.5V or 0 ->V_{DD}.

PARALLEL I/O PORTS 0 - 3

The ADuC812 uses four general purpose data ports to exchange data with external devices. In addition to performing general purpose I/O, some ports are capable of external memory operations; others are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral sharing a port pin is enabled, that pin may not be used as a general purpose I/O pin.

Ports 0,2 and 3 are bidirectional while Port 1 is an input only port. All ports contain an output latch and input buffer, the I/O Ports will also contain an output driver. Read and Write accesses to Port 0-3 pins are performed via their corresponding special function registers.

Each Port I/O line may be independently configured as an input or output via the corresponding individual Port SFR bits in one of four Port SFR's (PO - P3).

SERIAL I/O PORTS

UART Interface

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. However if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost.

The physical interface to the serial data network is via Pins RXD(P3.0) and TXD(P3.1) and the serial port can be configured into 1 of 4 modes of operation.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is an industry standard synchronous serial interface which allows eight bits of data to be synchronously transmitted and received simultaneously. The system can be configured for Master or Slave operation and typically consists of four pins, namely :

MISO :Master In, Slave Out Data I/O Pin
MOSI :Master Out, Slave In Pin
SCLOCK :Serial Clock I/O Pin
$\overline{SS}$:Slave Select I/O Pin

2 Wire Serial Interface (I2C Compatible)

The ADuC812 supports a 2 wire serial interface mode which is I2C compatible. This interface can be configured to be a Software Master or Hardware Slave. This port uses two pins in the interface

SADD : Serial data I/O Pin
SCLOCK : Serial Clock

TIMERS/COUNTERS

The ADuC812 has three 16-bit Timer/Counters, namely : Timer 0, Timer 1 and Timer 2. The Timer/Counter hardware has been included on-chip to relieve the processor core of the overhead inherent in implementing timer/counter functionality in software. Each Timer/Counter consists of two 8-bit registers THx and TLx (x = 0, 1 and 2). All three can be configured to operate either as timers or event counters.

In 'Timer' function, the TLx register is incremented every machine cycle. Thus one can think of it as counting machine cycles. Since a machine cycle consists of 12 oscillator periods, the maximum count rate is 1/12 of the oscillator frequency.

In 'Counter' function, the TLx register is incremented by a 1 to 0 transition at its corresponding external input pin, T0, T1 or T2.

ON-CHIP MONITORS

The ADuC812 integrates two on-chip monitor functions so as to minimize code or data corruption during catastrophic programming or other external system faults. Again, both monitor functions are fully configurable via the SFR space.

WATCHDOG TIMER

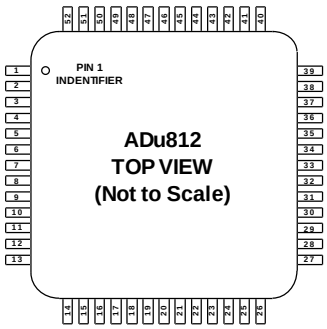
The purpose of the watchdog timer is to generate a device reset within a reasonable amount of time if the ADuC812 enters an erroneous state, possibly due to a programming error, electrical noise or RFI. The Watchdog function can be permanently disabled by clearing WDE (Watchdog Enable) bit in the Watchdog Control (WDCON) SFR. When enabled the watchdog circuit will generate a system reset if the user program fails to refresh the watchdog within a predetermined amount of time. The watchdog reset interval can be adjusted via the SFR pre-scale bits from 16 to 2048mS.

POWER SUPPLY MONITOR

The Power Supply Monitor generates an interrupt when the power supply to the ADuC812 drops below one of five user selectable voltage trip points from 2.6V to 4.6V. The interrupt bit will not be cleared until the power supply has returned above the trip point for at least 256mS.

This monitor function ensures both that the user can save working registers so as to avoid possible data corruption due to the low supply condition and that code execution will not resume until a 'safe' supply level has been well established. The supply monitor is also protected against spurious glitches triggering the interrupt circuit.

PIN CONFIGURATION



52 PIN PQFP

52 PQFP	Pin Name	52 PQFP	Pin Name
1	P1.0/ADC0/T2	27	SDATA/MOSI
2	P1.1/ADC1/T2EX	28	P2.0/A8/A16
3	P1.2/ADC2	29	P2.1/A9/A17
4	P1.3/ADC3	30	P2.2/A10/A18
5	AV_{DD}	31	P2.3/A11/A19
6	AGND	32	XTAL1
7	C_{REF}	33	XTAL2
8	V_{REF}	34	DV_{DD}
9	DAC0	35	DGND
10	DAC1	36	P2.4/A12/A20
11	P1.4/ADC4	37	P2.5/A13/A21
12	P1.5/ADC5/$\overline{SS}$[1]	38	P2.6/A14/A22
13	P1.6/ADC6	39	P2.7/A15/A23
14	P1.7/ADC7	40	$\overline{EA}/V_{PP}$
15	RESET	41	$\overline{PSEN}$
16	P3.0/RxD	42	ALE
17	P3.1/TxD	43	P0.0/AD0
18	P3.2/$\overline{INT0}$	44	P0.1/AD1
19	P3.3/$\overline{INT1}$/MISO	45	P0.2/AD2
20	DV_{DD}	46	P0.3/AD3
21	DGND	47	DGND
22	P3.4/T0	48	DV_{DD}
23	P3.5/T1/$\overline{CONVST}$	49	P0.4/AD4
24	P3.6/$\overline{WR}$	50	P0.5/AD5
25	P3.7/RD	51	P0.6/AD6
26	SCLOCK	52	P0.7/AD7

DEVELOPMENT TOOLS

The ADuC812 is supported by a complete set of tools for system development. The ADuC812 Development tools include :

ASM51: 8051- 2 pass, Assembler.

ADSIM812 : Windows Simulator for ADuC812 with full support for On-Chip analog I/O (ADC and DAC) peripherals.

DeBug812: Windows based, Serial Port Debugger for the ADuC812.

Dload812: In-Circuit Serial Port Downloader for On-Chip FLASH programming.

Flash Programming :

External programming of the Flash Memory program space supported by major third party PROM Programmer manufacturers.

QuickStart: Full ADuC812 Development System including application's board and the above development tools.

Emulation: Full featured, real time, non-intrusive and transparent In-Circuit Emulator from Metalink Corporation.

ORDERING INFORMATION

Part Number	Ambient Temperature Range	Package Description
	-40°C to +85°C	52-PQFP

Contact your local Sales office for latest pricing and availibility information.