3-Phase IMVP-II & IMVP-III Core Controller for Mobile CPUs

Preliminary Technical Data — ADP3204

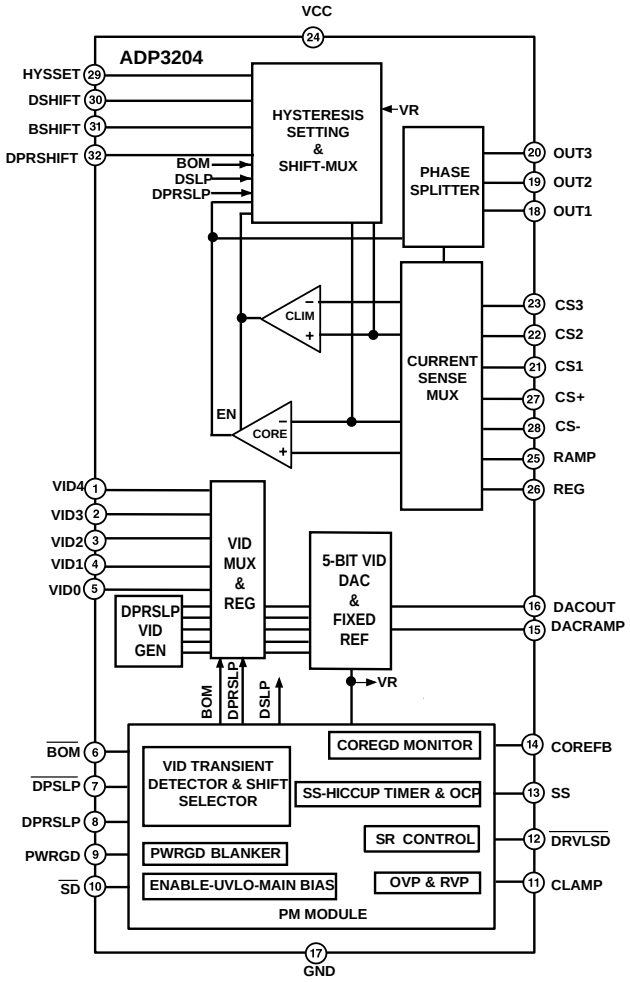
FEATURES

- Pin Selectable 1, 2, or 3-Phase Operation
- Excellent Current Sharing Characteristics
- Backward Compatible to IMVP-II
- Superior Load Transient Response with ADOPT™ Optimal Positioning Technology
- Noise-Blanking for Speed and Stability
- Synchronous Rectifier Control Extends Battery Life
- Smooth Output Transition During VID Code Change
- Cycle-by-Cycle Current Limiting
- Hiccup or Latched Overload Protection
- Transient-Glitch-Free Power Good
- Soft Start Eliminates Power-On In-Rush Current Surge
- Two-Level Over-Voltage and Reverse-Voltage Protection

APPLICATIONS

- IMVP-II and IMVP-III Core DC/DC Converters
- Fixed Voltage Mobile CPU Core DC/DC Converters
- Notebook/Laptop Power Supplies
- Programmable Output Power Supplies

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3204 is a 1, 2, or 3-phase hysteretic peak current DC-DC buck converter controller dedicated to power a mobile processor's core. The optimized low voltage design is powered from the 3.3 V system supply. The nominal output voltage is set by a 5-bit VID code. To accommodate the transition time required by the newest processors for on-the-fly VID changes, the ADP3204 features high-speed operation to allow a minimized inductor size that results in the fastest change of current to the output. To further allow for the minimum number of output capacitors to be used, the ADP3204 features active voltage positioning with ADOPT™ optimal compensation to ensure a superior load transient response. The output signals interface with a maximum of three ADP3415 MOSFET drivers that are optimized for high speed and high efficiency for driving both the top and bottom MOSFETs of the buck converter. The ADP3204 is capable of controlling the synchronous rectifiers to extend battery lifetime in light load conditions.

REV. PrF 1/02

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ADP3204–SPECIFICATIONS[1]

(T_A =25°C, High (H) = VCC, Low (L) = 0 V, VCC = 3.3 V, $\overline{SD}$ = H, V_{COREFB} = V_{DAC} (≡ V_{DACOUT}), V_{REG} = V_{CS-} = V_{VID} = 1.25 V, $C_{DACRAMP}$ = 100 pF, R_{OUT1} =R_{OUT2} = R_{OUT3} = 100 kΩ, C_{OUT1} = C_{OUT2} = C_{OUT3} =10 pF, C_{SS} = 47 nF, R_{PWRGD} = 680 Ω to 1.2 V, R_{CLAMP} = 5.1 kΩ to VCC, HYSSET, BSHIFT, DSHIFT, and DPRSHIFT are open, $\overline{BOM}$ = H, $\overline{DSLP}$ = H, DPRSLP = L, unless otherwise noted) Current sunk by a pin has a positive sign, sourced by a pin has a negative sign. Negative sign is disregarded for min and max values.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY-UVLO-SHUTDOWN						
Normal Supply Current	I_{CC}			7	15	mA
UVLO Supply Current	I_{CCUVLO}				425	µA
Shutdown Supply Current	I_{CCSD}	$\overline{SD}$ = L, 3.0 V ≤ VCC ≤ 3.6 V			10	µA
UVLO Threshold		$\overline{SD}$ = H				
	V_{CCH}	V_{CC} ramping up, V_{SS}= 0 V			2.9	V
	V_{CCL}	V_{CC} ramping down, V_{SS} floating	2.65			V
UVLO Hysteresis	V_{CCHYS}		50			mV
Shutdown Threshold (CMOS Input)	V_{SDTH}			V_{CC}/2		V
POWERGOOD						
Core Feedback Threshold Voltage	$V_{COREFBH}$	0.9 V < V_{DAC} < 1.675 V				
		V_{COREFB} ramping up	1.12V_{DAC}	1.14V_{DAC}		V
		V_{COREFB} ramping down	1.10V_{DAC}	1.12V_{DAC}		V
		V_{COREFB} ramping up	0.88V_{DAC}	0.90V_{DAC}		V
		V_{COREFB} ramping down	0.86V_{DAC}	0.88V_{DAC}		V
Power Good Output Voltage	V_{PWRGD}	V_{COREFB} = V_{DACOUT}	0.95V_{CC}		V_{CC}	V
(open drain output)		V_{COREFB} = 0.8 V_{DACOUT}	0		0.8	V
Masking Time[2]	$t_{PWRGDMSK}$[6]			100		µs
SOFT-START/HICCUP TIMER						
Charge/Discharge Current	I_{SS}	V_{SS} = 0 V		55		µA
		V_{SS} = 0.5 V		15		µA
Soft-Start Enable/Hiccup Termination Threshold	V_{SSEN}	V_{REG} = 1.25 V, V_{RAMP} = V_{COREFB} = 1.27 V				
		V_{SS} ramping down		80	200	mV
		V_{SS} ramping up[8]		150		mV
Soft-Start Termination/Hiccup Enable Threshold	V_{SSTERM}	V_{RAMP} = V_{COREFB} = 1.27 V, V_{SS} ramping up	1.75	2.00	2.25	V
VID DAC						
VID Input Threshold (CMOS Inputs)	$V_{VID0.4}$			V_{CC}/2		V
VID Input Current (Internal Active Pull-up)	$I_{VID0.4}$	VID 0..4 = L		90		µA
Output Voltage	V_{DAC}	See VID Code Table 1	0.600		1.750	V
Accuracy	$\Delta V_{DAC}/V_{DAC}$	0.750 V < V_{DAC} < 0.850 V	–1.0		+1.0	%
		0.825 V < V_{DAC} < 0.600 V	–8.5		+8.5	mV
Settling Time[2]	t_{DACS}[3]	$C_{DACRAMP}$ = 100 pF		3.5		µs
		$C_{DACRAMP}$ = 1 nF		35		µs
DACRAMP Inner Resistance[7]	$R_{DACRAMP}$			10		kΩ

Notes:

[1] All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

[2] Guaranteed by characterization.

[3] Measured from 50% of VID code transition amplitude to the point where V_{DACOUT} settles within ±1% of its steady state value.

[4] 40 mV_{PP} amplitude impulse with 20 mV overdrive. Measured from the input threshold intercept point to 50% of the output voltage swing.

[5] Measured between the 30% and 70% points of the output voltage swing.

[6] Two test conditions: 1)PWRGD is OK but forced to fail by applying an out-of-the-CoreGood-window voltage ($V_{COREFB,BAD}$ = 1.0 V at V_{VID} = 1.25 V setting) to the COREFB pin right after the moment that $\overline{BOM}$ or DPRSLP is asserted/de-asserted. PWRGD should not fail immediately only with the specified blanking delay time. 2) PWRGD is forced to fail ($V_{COREFB,BAD}$ = 1.0 V at V_{VID} = 1.25 V setting) but gets into the CoreGood-window ($V_{COREFB,GOOD}$ = 1.25 V) right after the moment that $\overline{BOM}$ or DPRSLP is asserted/de-asserted. PWRGD should not go high immediately only with the specified blanking delay time.

[7] Measured between DACRAMP and DACOUT pins.

[7] Guaranteed by design.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CORE COMPARATOR						
Input Offset Voltage (Ramp-Reg)	V_{COREOS}	V_{REG} = 1.25 V		±1.5		mV
Input Bias Current	I_{REG}, I_{RAMP}	V_{REG} = V_{RAMP} = 1.25 V		±1		µA
Output Voltage (OUT1, OUT2, and OUT3)	V_{OUT_H}	V_{CC} = 3.0 V	2.5		3.0	V
	V_{OUT_L}	V_{CC} = 3.6 V	0		0.8	V
Propagation Delay Time[2]	t_{RMPOUT_PD}[4]	T_A = 25°C			30	ns
		T_A = Full Range			40	ns
Rise and Fall Time[2]	t_{OUT_R}[5]			7	10	ns
(OUT1, OUT2, and OUT3)	t_{OUT_F}[5]			7	10	ns
Noise Blanking Time[2]	t_{BLNK}	OUT L-H transition		80		ns
		OUT H-L transition		120		ns
CURRENT LIMIT COMPARATOR						
Input Offset Voltage	V_{CLIMOS}	V_{CS-} = 1.25 V		±4	±6	mV
Input Bias Current	I_{CS+}	V_{CS+} = 1.25 V		–5	–3	µA
Propagation Delay Time[2]	t_{CLPD}[4]	T_A = 25° C		30	60	ns
		T_A = Full Range		50	100	ns
CURRENT SENSE MULTIPLEXER						
Trans-Resistance	$R_{CS1\text{-}CS+}$, $R_{CS2\text{-}CS+}$, $R_{CS3\text{-}CS+}$	Switch is ON		150		Ω
		Switch is OFF		10		MΩ
Common Mode Voltage Range		V_{CS1} = V_{CS2}, = V_{CS3}	0		2	V
HYSTERESIS SETTING						
Hysteresis Current	I_{RAMP_H}, $-I_{CSP\_H}$	V_{REG} = 1.25 V				
		V_{RAMP} = 1.23 V, $\overline{BOM}$ = H				
		I_{HYSSET} = 10 µA	–8	–10	–12	µA
		I_{HYSSET} = 100 µA	–80	–100	–120	µA
		V_{RAMP} = 1.27 V, $\overline{BOM}$ = H				
		I_{HYSSET} = 10 µA	8	10	12	µA
		I_{HYSSET} = 100 µA	80	100	120	µA
		V_{RAMP} = 1.23 V, $\overline{BOM}$ = L				
		I_{HYSSET} = 10 µA	–6.4	–8	–9.6	µA
		I_{HYSSET} = 100 µA	–64	–80	–96	µA
		V_{RAMP} = 1.27 V, $\overline{BOM}$ = L				
		I_{HYSSET} = 10 µA	6.4	8	9.6	µA
		I_{HYSSET} = 100 µA	64	80	96	µA
Hysteresis Reference Voltage	V_{HYSSET}		1.53	1.7	1.87	V
CURRENT LIMIT SETTING						
Hysteresis Current	I_{CS-}	V_{RAMP} = 1.23 V				
		V_{REG} = V_{CS-} = V_{COREFB} = 1.25 V				
		V_{CS+} = 1.23 V $\overline{BOM}$ = H				
		I_{HYSSET} = 10 µA	–27	–31.5	–36	µA
		I_{HYSSET} = 100 µA	–268	–301.5	–335	µA
		V_{CS+} = 1.27 V, $\overline{BOM}$ = H				
		I_{HYSSET} = 10 µA	–18	–21.5	–25	µA
		I_{HYSSET} = 100 µA	–178	–201.5	–225	µA
		V_{CS+} = 1.23 V, $\overline{BOM}$ = L				
		I_{HYSSET} = 10 µA	–21	–25.5	–30	µA
		I_{HYSSET} = 100 µA	–212	–241.5	–271	µA
		V_{CS+} = 1.27 V, $\overline{BOM}$ = L				
		I_{HYSSET} = 10 µA	–14	–17.5	–21	µA
		I_{HYSSET} = 100µA	–140	–161.5	–183	µA

ADP3204–SPECIFICATIONS[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SHIFT SETTING						
Battery-Shift Current	I_{RAMPB}, I_{CS+B}	V_{VID} = 1.25 V R_{BSHIFT} = 12.5 k, $\overline{BOM}$ = L $\overline{DSLP}$ = H	–90	–100	–110	µA
Battery-Shift Reference Voltage	V_{BSHIFT}			V_{DAC}		V
DeepSleep-Shift Current	I_{RAMPD}, I_{CS+D}	V_{VID} = 1.25 V R_{DSHIFT} = 12.5 k, $\overline{BOM}$ = H $\overline{DSLP}$ = L	–90	–100	–110	µA
DeepSleep-Shift Reference Voltage	V_{DSHIFT}			V_{DAC}		V
DeeperSleep-Shift Current	I_{REGDPR} , $-I_{COREFBDPR}$	V_{VID} = 1.25 V, $I_{DPRSHIFT}$ = 100 µA, DPRSLP = H	-90	-100	-110	µA
DeeperSleep-Shift Reference Voltage	$V_{DRPSHIFT}$			V_{DAC}		V
SHIFT CONTROL INPUTS						
$\overline{BOM}$ Threshold (CMOS Input)	V_{BOM}			$V_{CC}/2$		V
$\overline{DSLP}$ Threshold CMOS Input)	V_{DSLP}			$V_{CC}/2$		V
DPRSLP Mode Threshold (CMOS Input)	V_{DPRSLP}			$V_{CC}/2$		V
LOW-SIDE DRIVE CONTROL						
Output Voltage (CMOS Output)	V_{DRVLSD}	DPRSLP = H	0		0.4	V
		DPRSLP = L	0.7 V_{CC}		V_{CC}	V
Output Current	I_{DRVLSD}	DPRSLP = L, V_{DRVLSD} = 1.5 V	0.5			mA
		DPRSLP = H	–0.5			mA
OVER/REVERSE VOLTAGE PROTECTION-CORE FEEDBACK						
Over-Voltage Threshold	$V_{COREFB,OVP}$	V_{COREFB} rising		2.0		V
		V_{COREFB} falling		1.95		V
Reverse-Voltage Threshold	$V_{COREFB,RVP}$	V_{COREFB} falling		–0.3		V
		V_{COREFB} rising		–0.1		V
Output Voltage (open drain output)	V_{CLAMP}		0.7 V_{CC}		V_{CC}	V
Output Current	I_{CLAMP}	V_{CLAMP} = 1.5 V, V_{VID} = 1.25 V V_{COREFB} = V_{DAC}			10	µA
		V_{COREFB} = 2.2 V	1	4		mA

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP3204JCP-Reel	0°C to 100°C	LFCSP-32	CP-32
ADP3204JCP-Reel7	0°C to 100°C	LFCSP-32	CP-32

ABSOLUTE MAXIMUM RATINGS*

Input Supply Voltage (VCC) ..... -0.3 V to +7 V
UVLO Input Voltage ..... -0.3 V to +7 V
All Other Inputs/Outputs ..... VCC + 0.3 V
Operating Ambient Temperature Range ..... 0°C to +100°C
Junction Temperature Range ..... 0°C to +150°C
θ_{JA} ..... 98°C/W
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

TABLE1. VID CODE

VID4	VID3	VID2	VID1	VID0	VOUT
0	0	0	0	0	1.750
0	0	0	0	1	1.700
0	0	0	1	0	1.650
0	0	0	1	1	1.600
0	0	1	0	0	1.550
0	0	1	0	1	1.500
0	0	1	1	0	1.450
0	0	1	1	1	1.400
0	1	0	0	0	1.350
0	1	0	0	1	1.300
0	1	0	1	0	1.250
0	1	0	1	1	1.200
0	1	1	0	0	1.150
0	1	1	0	1	1.100
0	1	1	1	0	1.050
0	1	1	1	1	1.00
1	0	0	0	0	0.975
1	0	0	0	1	0.950
1	0	0	1	0	0.925
1	0	0	1	1	0.900
1	0	1	0	0	0.875
1	0	1	0	1	0.850
1	0	1	1	0	0.825
1	0	1	1	1	0.800
1	1	0	0	0	0.775
1	1	0	0	1	0.750
1	1	0	1	0	0.725
1	1	0	1	1	0.700
1	1	1	0	0	0.675
1	1	1	0	1	0.650
1	1	1	1	0	0.625
1	1	1	1	1	0.600

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1–5	VID[4:0]	Voltage Identification Inputs. These are the VID inputs for logic control of the programmed reference voltage that appears at the DACOUT pin, and, via external component configuration, is used for setting the output voltage regulation point. The VID pins have a specified internal pullup current such that, if left open, the pins will default to a logic high state. The VID code does not set the DAC output voltage directly but through a transparent latch which is clocked by the $\overline{\text{BOM}}$ pin's GMUXSEL signal rising and falling edge.
6	$\overline{\text{BOM}}$	Battery Optimized Mode Control (active low). This is a digital input pin that corresponds to the system's GMUXSEL signal that corresponds to Battery Optimized Mode of the CPU operation in its active low state and Performance Optimized Mode (POM) in its deactivated high state. The signal also controls the optimal positioning of the core voltage regulation level by offsetting it downwards in Battery Optimized Mode according to the functionality of the BSHIFT and RAMP pins. It is also used to initiate a masking period for the PWRGD signal whenever a GMUXSEL signal transition occurs.
7	$\overline{\text{DPSLP}}$	Deep Sleep Mode Control (active low). This is a digital input pin corresponding to the system's $\overline{\text{STP CPU}}$ signal which, in its active state, corresponds to Deep Sleep mode of the CPU operation, which is a subset operating mode of either BOM or POM operation. The signal controls the optimal positioning of the core voltage regulation level by offsetting it downwards according to the functionality of the DSHIFT and RAMP pins.
8	DPRSLP	Deeper Sleep Mode Control (active high). This is a digital input pin corresponding to the system's DPRSLPVR signal corresponding to Deeper Sleep mode of the CPU operation. The signal when it is activated controls the DAC output voltage by disconnecting the VID signals from the DAC input and setting a specified internal Deeper Sleep code instead. At de-assertion of the DPRSLPVR signal, the DAC output voltage returns to the voltage level determined by the external VID code. The DPRSLPVR signal is also used to initiate a blanking period for the PWRGD signal to disable its response to a pending dynamic core voltage change corresponds to the VID code transition.
9	PWRGD	Power Good (active high). This is an open drain output pin which, via the assistance of an external pull-up resistor to the desired voltage, indicates that the core voltage is within the specified tolerance of the VID programmed value or else in a VID transition state as indicated by a recent state transition of either the $\overline{\text{BOM}}$ or DPRSLP pins. PWRGD is deactivated (pulled low) when the IC is disabled or in UVLO mode or starting up, or the COREFB voltage is out of the core powergood window. The open drain output allows external wired ANDing (logical NORing) with other open drain/collector power-good indicators.
10	$\overline{\text{SD}}$	Shutdown (active low). This is a digital input pin coming from a system signal which, in its active state, shuts down the IC operation, placing the IC in its lowest quiescent current state for maximum power savings.
11	CLAMP	Clamp (active high). This is an open drain output pin which, via the assistance of an external pull-up resistor, indicates that the core voltage should be clamped for its protection. To allow the highest level of protection, the CLAMP signal is developed using both a redundant reference and a redundant feedback path with respect to those of the main regulation loop. The signal is timed out using the softstart capacitor, so an external current protection mechanism (e.g., fuse or AC adapter's current limit) should be tripped within ~3 times the programmed soft start time (e.g. 5~10 ms). In a PrFferred and more conservative configuration, the core voltage is clamped by an external FET. The initial protection function is served when it is activated by detection of either an over-voltage or a reverse-voltage condition on the COREFB pin. A backup protection function due to loss of the latched signal at IC power-off is served by connecting the pull-up resistor to a system "ALWAYS" regulator output (e.g., V5_ALWAYS). If the external FET is used, this implementation will keep the core voltage clamped until the ADP3422 has power re-applied, thus keeping protection for the CPU even after a hard-failure power-down and restart (e.g., a shorted top or bottom FET).

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
12	$\overline{\text{DRVLSD}}$	Drive-Low Shutdown (active low). This is a digital output pin which, in its active state, indicates that the lower FET of the core VR should be disabled. In the suggested application schematic this pin is directly connected to the pin of the same name on the ADP3415 or other driver IC. Drive-low shutdown is normally activated by the DPRSLP signal, corresponding to a light load condition, but a number of dynamic conditions can override the control of this pin as needed.
13	SS	Soft Start. This is an analog I/O pin whose output is a controlled current source used to charge or discharge an external grounded capacitor and whose input is the detected voltage that is indicative of elapsed time. The pin controls the soft start time of the IC as well as the hiccup cycle time during overload including but not limited to short circuit, over voltage, and reverse voltage. Hiccup operation is a feature that was added to reduce short circuit power dissipation by more than an order of magnitude, while still allowing an automatic restart when the failure mode ceased. The hiccup operation can be overwritten and changed to latched-off operation by clamping the SS pin voltage to a voltage level somewhere above ~ 0.2 V. In this configuration, the controller does not restart after a hiccup cycle is initiated, but stays latched off.
14	COREFB	Core Feedback. This is a high-impedance analog input pin that is used to monitor the output voltage for setting the proper state of the PWRGD and CLAMP pins. It is generally recommended to RC-filter the ripple and noise from the monitored core voltage, as suggested by the application schematic.
15	DACRAMP	DAC Output Ramp Rate Setting. The rate at which the DAC output voltage can ramp up or down from one voltage to another when the VID code changes can be controlled by an external DACRAMP capacitor connected from this pin to the DACOUT pin. The time constant of the DACOUT voltage variation is determined by the internal resistance appearing across the DACRAMP and DACOUT pins, and the capacitance of the DACRAMP capacitor. Not having any DACRAMP capacitor connected to these pins results in the fastest rate. Use of the DACRAMP rate control and the Deeper Sleep Shift adjustment features are exclusive.
16	DACOUT	Digital-to-Analog Converter Output of the VID input. This output voltage is the VID-controlled reference voltage whose primary function is to determine the output voltage regulation point.
17	GND	Ground.
18-20	OUT1-3	Outputs to Drivers 1-3. These are digital output pins which are used to command the state of the switched nodes via the drivers. They should be connected to the IN pin of the drivers of the appropriate channels.
21	CS1	Current Sense Channel 1. This is a high -impedance analog input pin which is used for providing negative feedback of the current informaiton for the first channel.
22	CS2	Current Sense, Channel 2. This is a high-impedance analog input pin which is used for providing negative feedback of the current information for the second channel. The pin is also used to determine whether the chip is acting as a single or dual-phase controller. If both CS2 and CS3 pins are tied to VCC but not to sense resistors then dual and three-phase operation is disabled; the chip works as a single phase controller. In this condition, the second and third phase's output signals (OUT2 and OUT3) are not switching but stay static low. The CS2 pin alone should not be connected to VCC but always with CS3 together to activate single phase operation.
23	CS3	Current Sense, Channel 3. This is a high-impedance analog input pin which is used for providing negative feedback of the current information for the third channel. The pin is also used to determine whether the chip is acting as a single, dual, or three-phase controller. If the pin is tied to VCC but not to a sense resistor then three-phase operation is disabled; the chip works as a dual-phase controller. In this condition the third phase's output signal (OUT3) is not switching but stays static low.

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
24	VCC	Power supply. This should be connected to the system's 3.3 V power supply output.
25	RAMP	Regulation Ramp Feedback Input. The RAMP pin voltage is compared against the REG pin for cycle-by-cycle switching response. Several switched current sources also appear at this input, the cycle-by-cycle hysteresis-setting switched current programmed by the HYSSET pin, the BOM shift current programmed by the BSHIFT pin, and the Deep Sleep shift current programmed by the DSHIFT pin. The external resistive termination at this pin sets the magnitude of the hysteresis applied to the regulation loop.
26	REG	Regulation Voltage Summing Input. This is a high-impedance analog input pin into which the voltage reference of the feedback loop allows the summing of both the DACOUT voltage and the core voltage for programming the output resistance of the core voltage regulator. This is also the pin at which an optimized transient response can be tailored using Analog Devices' patented ADOPT design technique.
27	CS+	Current Limit Positive Sense. This is a high-impedance analog input pin that is multiplexed between either of the three current-sense inputs during the high state of the OUT pin of the respective channel. During the common off-time of both channels the pin's voltage reflects the average of the three channels. The multiplexed current sense signal is passed to the core comparator through an external resistive termination connected from this pin to the RAMP pin. The external (RAMP) resistor sets the magnitude of the hysteresis applied to the regulation loop.
28	CS-	Current Limit Negative Sense. This is a high-impedance analog input pin which is normally Kelvin connected via a current-limit programming resistor to the negative node of the current sense resistor(s). A hysteretically-controlled current - three times the current programmed at the HYSSET pin - also flows out of this pin and develops a current-limit-setting voltage across that resistor which then must be matched by the inductor current flowing in the current sensing resistor in order to trigger the current limit function. When triggered, the current flowing out of this pin is reduced to two-thirds of its PrFvious value, producing hysteresis in the current limiting function.
29	HYSSET	Hysteresis Set. This is an analog I/O pin whose output is a fixed voltage reference and whose input is a current that is programmed by an external resistance to ground. The current is used in the IC to set the hysteretic currents for the Core Comparator and the Current Limit Comparator. Modification of the resistance will affect both the hysteresis of the feedback regulation and the current limit set point and hysteresis.
30	DSHIFT	Deep Sleep Shift. This is an analog I/O pin whose output is the VID reference voltage and whose input is a current that is programmed by an external resistance to ground. The current is used in the IC to set a switched bias current out of the RAMP pin, depending on whether it is activated by the DSLP# signal. When activated, this added bias current creates a downward shift of the regulated core voltage to a PrFdetermined optimum level for regulation corresponding to Deep Sleep mode of CPU operation. The use of the VID code as the reference makes the Deep Sleep offset a fixed percentage of the VID setting, as required by specifications.
31	BSHIFT	Battery Optimized Mode ($\overline{\text{BOM}}$) Shift. This is an analog I/O pin whose output that is the VID reference voltage and whose input current is programmed by an external resistance to ground. The current is used in the IC to set a switched bias current out of the RAMP pin, depending on whether it is activated by the $\overline{\text{BOM}}$ signal. When activated, this added bias current creates a downward shift of the regulated core voltage to a PrFdetermined optimum level for regulation corresponding to Battery Optimized Mode of CPU operation. The use of the VID code as the reference makes the DSHIFT a fixed percentage of the VID setting, as required by specifications.

Pin	Mnemonic	Function
32	DPRSHIFT	Deeper Sleep Shift. This is an analog I/O pin whose output is a fixed voltage reference and whose input current is programmed by an external resistor to ground. The current is used to set two switched bias currents that flow into both the REG and COREFB pins, depending on the DPRSLP signal. When activated, the REG pin bias current creates an upward shift of the regulated core voltage from the internally set (default) Deeper Sleep value to the voltage level specified by the CPU Deeper Sleep operation. The COREFB bias current creates the same amount of downward shift of the COREFB voltage is. The shifted back COREFB voltage is compared against the internally set Deeper Sleep voltage to create Power Good information. Use of the Deep Sleep Shift adjustment and the DACRAMP rate control features are exclusive.

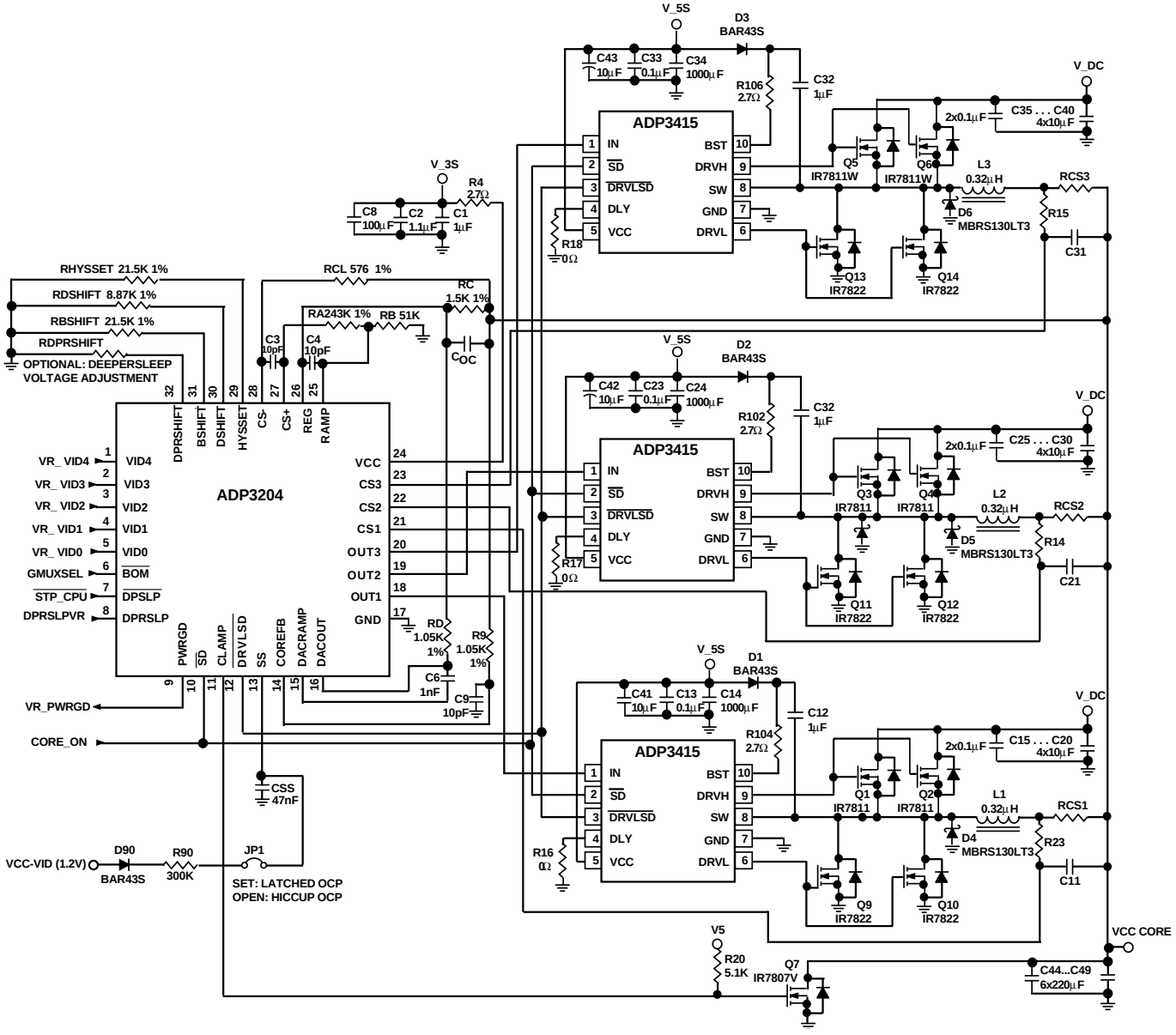
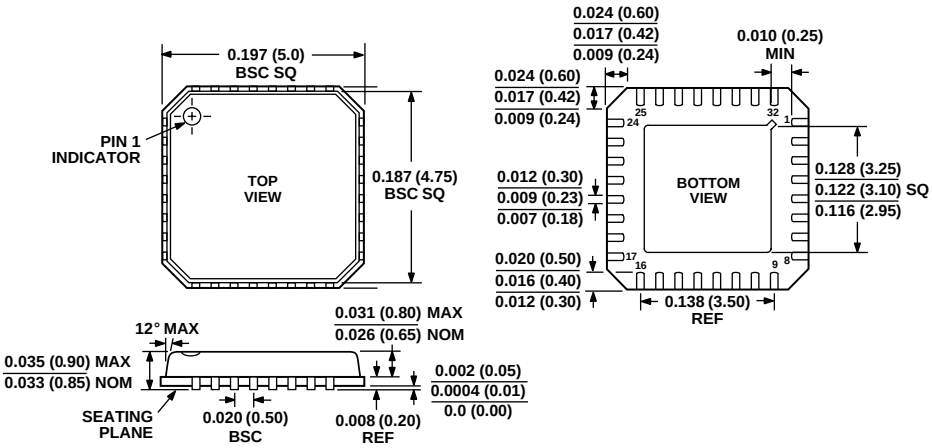


Figure 1. Typical Application

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



CONTROLLING DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS MEET JEDEC MO-220-VHHD-2