10.709 Gb/s LASER DIODE DRIVER Chipset

Preliminary Technical Data — ADN2843

FEATURES

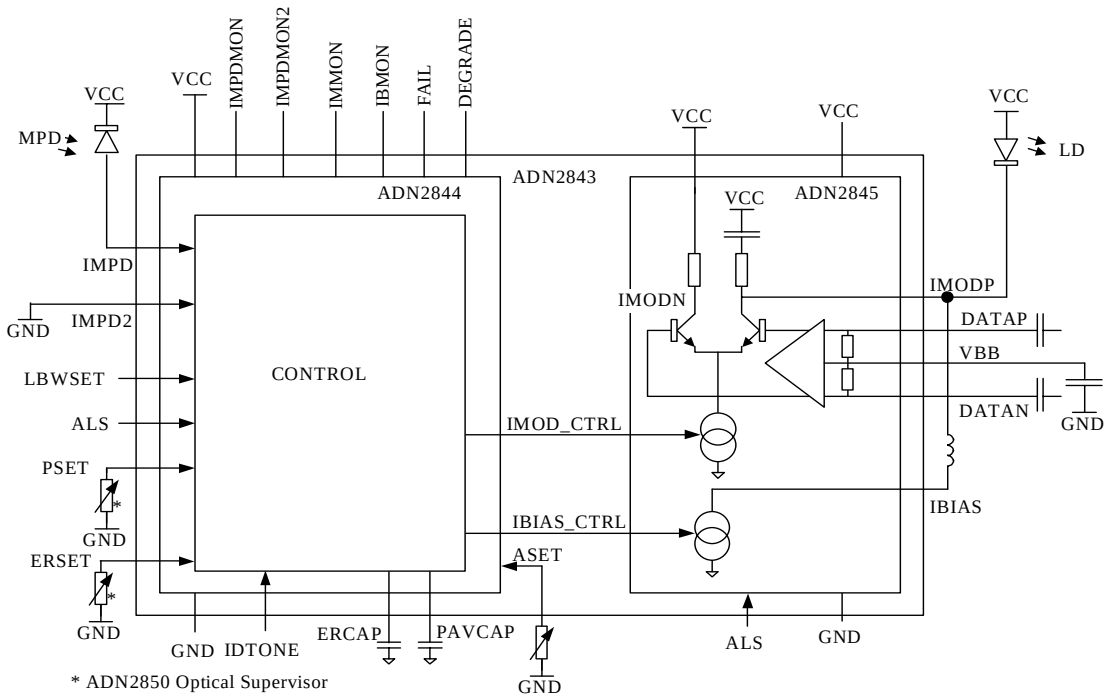
Data Rates from 50Mb/s to 10.709 Gb/s
Typical rise/fall-time 30ps
Bias Current range 3mA to 80mA
Modulation Current range 5mA to 80mA
Monitor Photo Diode Range 50µA to 1100µA
Closed Loop Control of both average optical power and extinction ratio
Programmable loop BW for both loops
Laser fail and laser degrade alarms
Automatic laser shutdown, ALS
Dual MPD functionality for wavelength control
CML data inputs
50Ω internal data terminations
+3.3V single supply operation
Driver supplied in dice format.

APPLICATIONS

SONET OC-192, SDH STM-64
Suports 10.667Gbp/s and 10.709Gb/s FEC rates
10GbEthernet IEEE802.3

GENERAL DESCRIPTION

The ADN2843 chipset uses a unique control algorithm to control both average power and extinction ratio of the laser diode, LD, after initial factory set-up. The chipset consists of two components. The ADN2844 contains the control loops, and the ADN2845 is the 10.7Gb/s data switch. The ADN2845 is available in dice format, and ADN2844 is available in packaged or dice format. External component count and PCB area are low as both power and extinction ratio control are fully integrated. Programmable alarms are provided for laser fail (end of life), and laser degrade (impending fail).



Functional Block Diagram

REV. PrA 14-Jan-2002

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ADN2843

(Vcc=3.3V±10%, All specifications Tmin to Tmax unless otherwise noted. Typical values specified at 25°C)

Parameter	MIN	TYP	MAX	UNITS	Condition
LASER BIAS (IBIAS)					
Output current Ibias	3		80	mA	
Ibias during ALS			10	uA	
ALS shutdown response time		10		us	
Compliance voltage	1.2		Vcc-1.0	V	
MODULATION CURRENT (IMODP)					
Output Current Imod	5		80	mA	
Compliance Voltage	1.2		Vcc	V	
Imod during ALS			10	uA	
Rise time		30		ps	
Fall time		30		ps	
Random Jitter		0.75		ps RMS	
Deterministic Jitter		10		ps Pk-Pk	
Monitor PD (MPD, MPD2)					
Input Current	50		1100	uA	
Input Voltage			1.6	V	
POWER SET INPUT (PSET)					
Capacitance			80	pF	
Voltage	1.15		1.35	V	
EXTINCTION RATIO INPUT (ERSET)					
Allowable Resistance Range	1k		25k	Ω	
Voltage	1.15		1.35	V	
ALARM SET (ASET)					
Allowable Resistance Range	1.15k		13.5k	Ω	
Voltage	1.15		1.35	V	
CONTROL LOOP					
Time Constant		0.22		s	
		2.25		s	LBWSET= Vcc
DATA INPUTS (DATAP, DATAN)					
Vpk-pk (single ended)	300		800	mV	
Input impedance		50		Ohm	
LOGIC INPUTS (ALS)					
Vih	2.4			V	
Vil			0.8	V	
ALARM OUTPUTS (internal 30kΩ to Vcc)					
Voh	2.4			V	
Vol			0.4	V	
IDTONE					
Fin	10		1000	KHz	
Input Current Range	50		4000	uA	
Voltage on IDTONE pin	VCC-1.5			V	
IBMON, IMMON, IMPDMON, IMPDMON2					
IBMON, IMMON Division Ratio		100		A/A	
IMPDMON, IMPDMON2 Division Ratio		1			
IMPDMON to IMPDMON2 Matching			1	%	
Compliance Voltage	0		1.5	V	
SUPPLY					
Vcc	3.0	3.3	3.6	V	
Icc (ADN2844)		36		mA	
Icc (ADN2845)		40		mA	Note 1

Note 1: IBIAS=0, IMOD=0. See section on Power Dissipation for calculation of complete power dissipation.

ABSOLUTE MAXIMUM RATINGS

(Ta = + 25 °C unless otherwise stated)

Vcc to GND ……..TBD
Operating Temperature Range
Industrial …….-40 °C to +85 °C
Storage Temperature Range..-65 °C to +150 °C
Junction Temperature Range (Tj max) ….+125 °C

Ordering Guide

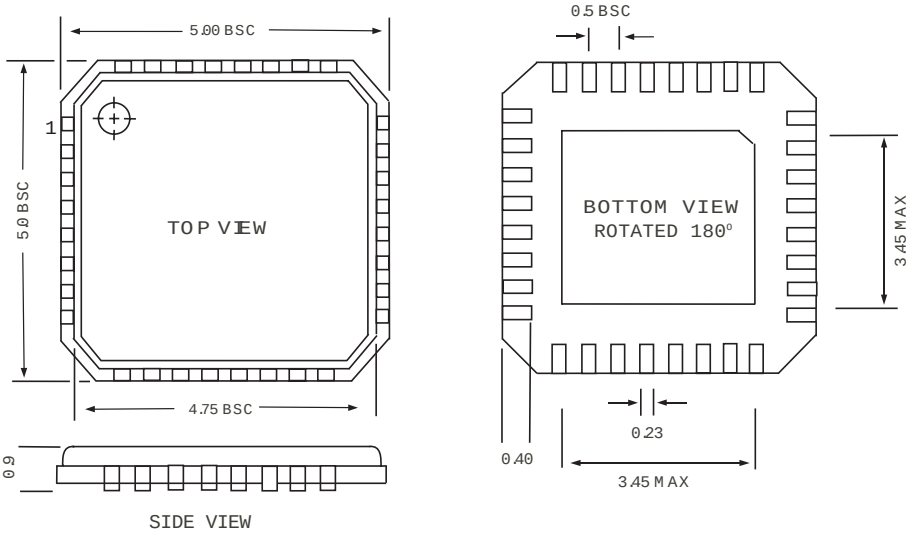
Model	Temperature Range	Package Description
ADN2843XXX(1) Chipset	-40'C to +85'C	ADN2844 Control Loop: 32-Lead LFCSP
		ADN2845 Data Switch: Dice
ADN2843XXX(2) Chipset	-40'C to +85'C	ADN2844 Control Loop: Dice
		ADN2845 Data Switch: Dice

OUTLINE DIMENSIONS

Dimensions shown in mm.

32-Lead (5x5) LFCSP (Exposed Paddle)

Exposed Paddle should be soldered to the most negative supply of the ADN2844
(ADN2844 also available as bare die)



GENERAL

Laser diodes have current-in to light-out transfer functions as shown in Figure 2. Two key characteristics of this transfer function are the threshold current and the slope in the linear region beyond the threshold current, referred to as slope efficiency, LI.

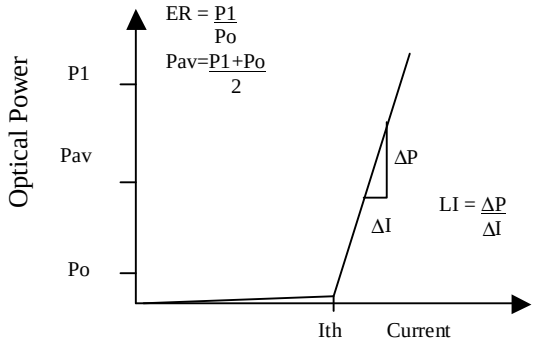


Figure 2: Laser Transfer Function

CONTROL

A monitor photo diode, MPD, is required to control the LD. The MPD current is fed into the ADN2843 to control the power and extinction ratio, continuously adjusting the bias current and modulation current in response to the laser's changing threshold current and light to current, LI, slope (slope efficiency).

The ADN2843 uses automatic power control, APC, to maintain a constant power over time and temperature.

The ADN2843 uses closed loop extinction ratio control to allow optimum setting of extinction ratio for every device. Hence SONET/SDH interface standards can be met over device variation, temperature and time. Closed loop modulation control eliminates the need to either over modulate the laser diode or include external components for temperature compensation, thus reducing R&D and second sourcing issues.

Power and Extinction Ratio are set using the PSET and ERSET pins respectively. A resistor is placed between the pin and GND to set the current flowing in each pin. The internal control loops force the PSET and ERSET pins to 1.23V above GND.

The ratios of current-in-to-current-out are given by the following formulae:

$$R_{PSET} = \frac{1.23}{I_{AV}}$$

I_{AV} is the average MPD current.

$$R_{ERSET} = \frac{1.23}{\frac{I_{MPD\_CW}}{P_{CW}} \times \frac{ER-1}{ER+1}}$$

P_{CW} is the DC optical power specified on the laser datasheet at which I_{MPD_CW} is specified.

Note that I_{ERSET} and I_{PSET} will change from laser diode to laser diode, therefore R_{ERSET} and R_{PSET} need to be adjusted for each Laser Diode**.** When tuning the Laser Diode, R_{PSET} should be adjusted first with R_{ERSET} at 25kΩ. Once the average power is set, R_{ERSET} is adjusted to set the desired extinction ratio. Once the values R_{PSET} and R_{ERSET} have been adjusted to set the desired average power and extinction ratio, the control loops maintain these values of average power and extinction ratio over environmental conditions and time.

LOOP TIME-CONSTANT SELECTION

The control loop time constant can be optimised for operation at data-rates of 2.5GB/s and above by setting the LBWSET pin low. This results in a faster loop time constant. The required value for the PAVCAP/ERCAP capacitors is 22nF in this case.

For multi-rate operation, the LBWSET pin should be set high and the required value for the PAVCAP/ERCAP capacitors is 820nF. This results in a slower loop time constant.

The PAVCAP/ERCAP capacitors are connected between the respective pins and GND. The capacitors should be low leakage multi-layer ceramic capacitors with an insulation resistance >100GΩ or an RC >1000s, whichever is the lower.

ALARMS

The ADN2843 alarms are designed to allow interface compliance to ITU-T-G958 (11/94) section 10.3..1.1.2 (transmitter fail) and section 10.3.1.1.3 (transmitter degrade).

The ADN2843 has two alarms, DEGRADE and FAIL. These alarms are raised when IBIAS exceeds the respective DEGRADE and FAIL thresholds. These alarms are active high. A resistor between ground and the ASET pin is used to set the current at which these alarms are raised. The current through the ASET resistor is a ratio of 1:100 to the FAIL alarm threshold. The DEGRADE alarm will be raised at 90% of the FAIL threshold.

Example: I_{FAIL} = 50mA so
$I_{DEGRADE}$ =45mA

$$I_{ASET} = \frac{Ibiastrip}{100} = \frac{50mA}{100} = 500uA$$

$$R_{ASET} = \frac{1.23\ V}{I_{ASET}} = \frac{1.23}{500uA} = 2.46\ k\Omega$$

The laser degrade alarm, DEGRADE, is provided to give a warning of imminent laser failure if the laser diode degrades further or environmental conditions continue to stress the LD, e.g. increasing temperature.

The laser fail alarm, FAIL, is activated when the transmitter can no longer be guaranteed to be SONET/SDH compliant. This occurs when one of the following conditions arise:

- The ASET threshold is reached.
- The ALS pin is set high. This shuts off the modulation and bias currents to the LD, resulting in the MPD current dropping to zero. This gives closed loop feedback to the system that ALS has been enabled.

ALARM INTERFACE

The alarm voltages are open collector outputs. An internal pull up resistor of 30k is used to pull the logic high value to VCC. However this can be over driven with an external resistor allowing alarm interfacing to non-VCC levels. **Non-VCC alarm output levels must be below the VCC used for the ADN2843.**

MONITOR CURRENTS

IBMON and IMMON mirror the bias, modulation currents at a ratio of 1:100 for increased monitoring functionality. IMPDMON and IMPDMON2 mirror the current in IMPD and IMPD2 respectively with a ratio of 1.
All monitors source current from VCC.

ID_TONE

The IDTONE pin is used for fibre identification / supervisory channels, or for control purposes. This pin modulates the optical one level by adding a current to IMOD over a possible range of 2% of min IMOD to 10% of max IMOD. The IDTONE current is set by an external current sink connected to the IDTONE pin. There is a gain of two between the IDTONE pin and the IMOD current.
To ratio the IDTONE current to IMOD, the input current can be derived from the IMMON output current.

If the IDTONE function is not being used, this pin must be tied to VCC to properly disable it.

Note that using ID tones during transmission may cause optical eye degradation.

AUTOMATIC LASER SHUTDOWN

The ADN2843 ALS allows compliance to ITU-T-G958 (11/94), section 9.7.

When ALS is asserted, both bias and modulation currents are turned off.

Correct operation of ALS can be confirmed by the fail alarm being raised when ALS is asserted. Note this is the only time that DEGRADE will be low while FAIL is high.

DUAL MPD DWDM FUNCTION

The MPD function mirrors the current in IMPD to the PSET pin and to the IMPDMON pin with a ratio of 1. If the MPD monitor function is not required, the Monitor Photo-Diode can be directly connected to the PSET pin, and the IMPD pin tied to GND.

A second Monitor Photo-Diode can be connected to the IMPD2 pin. Its current is mirrored to MODMON2 and also to the PSET pin where it is summed with the current mirrored from IMPD.

The two MPD monitor currents can be used as inputs to a wavelength control function when used in combination with various optical filtering techniques. If the IMPD2 pin is not being used, it should be tied to GND.

POWER DISSIPATION

The power dissipation of the ADN2845 can be calculated using the following expressions.

$$Icc = 40mA + 1.7 \times IMOD + 0.6 \times IBIAS$$

$$P = Vcc \times Icc + V_{IMOD} \times \frac{IMOD}{2} + V_{IBIAS} \times IBIAS$$

where V_{IMOD} is the average voltage on the IMOD pin, and V_{IBIAS} is the average voltage on the IBIAS pin.

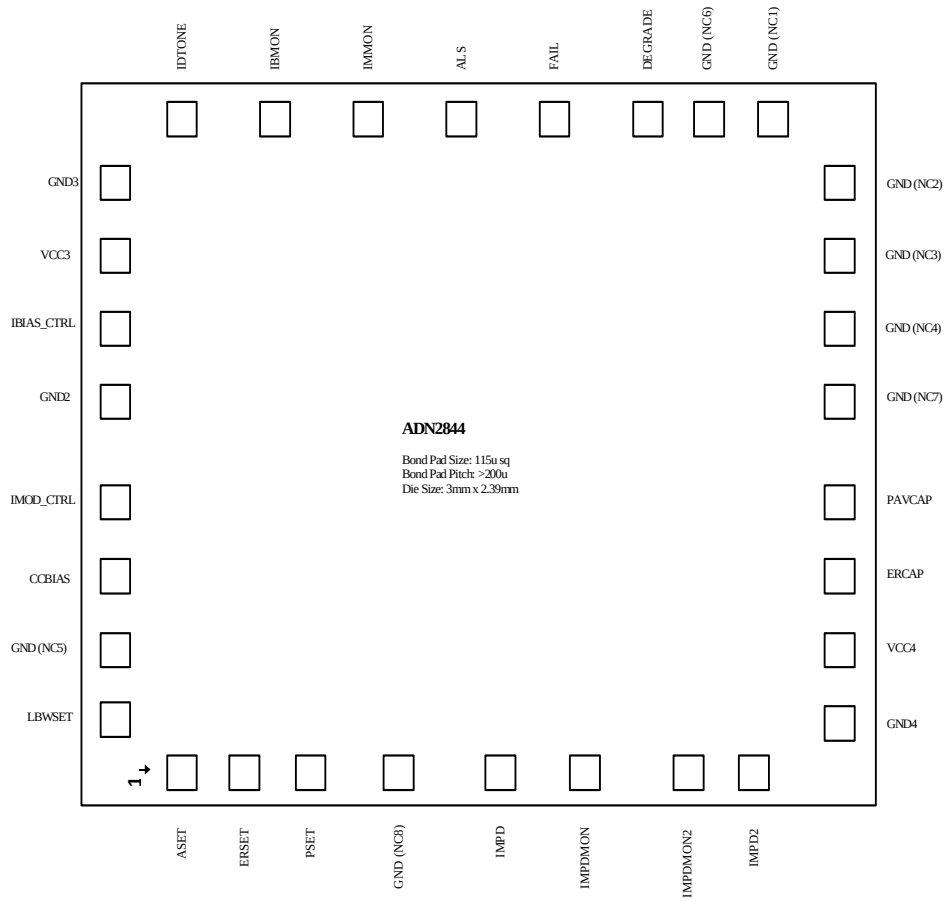
PIN FUNCTION DESCRIPTION

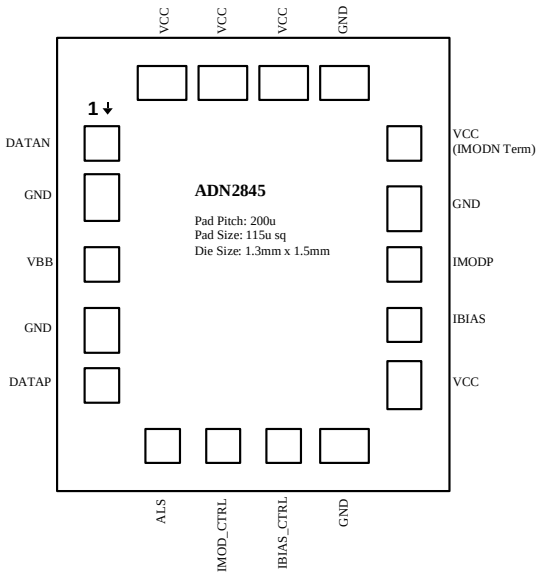
Pin	ADN2844	FUNCTION
1	ASET	Alarm current threshold set
2	ERSET	Extinction Ratio Current Set
3	PSET	Average Optical Power set pin.
4	GND	Test Input (nc8)
5	IMPD	Monitor Photo Diode current input.
6	IMPDMON	Mirrored current from IMPD
7	IMPDMON2	Mirrored current from IMPD2 (For optional use with two MPDs)
8	IMPD2	Optional second MPD current input
9	GND4	Negative supply
10	VCC4	Positive supply
11	ERCAP	Extinction Ratio loop capacitor
12	PAVCAP	Average Power Loop capacitor
13	GND	Test Input (nc7)
14	GND	Test Input (nc4)
15	GND	Test Input (nc3)
16	GND	Test Input (nc2)
17	GND	Test Input (nc1)
18	GND	Test Input (nc6)
19	DEGRADE	DEGRADE Alarm output, open collector, active high
20	FAIL	FAIL Alarm output, open collector, active high
21	ALS	Automatic Laser Shutdown Logic Input
22	IMMON	Modulation current mirror output, current source from VCC
23	IBMON	Bias current mirror output, current source from VCC
24	IDTONE	Id Tone input current.
25	GND3	Negative supply
26	VCC3	Positive supply
27	IBIAS_CTRL	Control output current sink.
28	GND2	Negative supply
29	IMOD_CTRL	Control output current sink.
30	CCBIAS	Connected to Laser diode side of cap when AC coupling used, otherwise, tie to VCC.
31	GND	Test Input (nc5)
32	LBWSET	Select Low Loop Bandwidth Mode (Active=VCC)

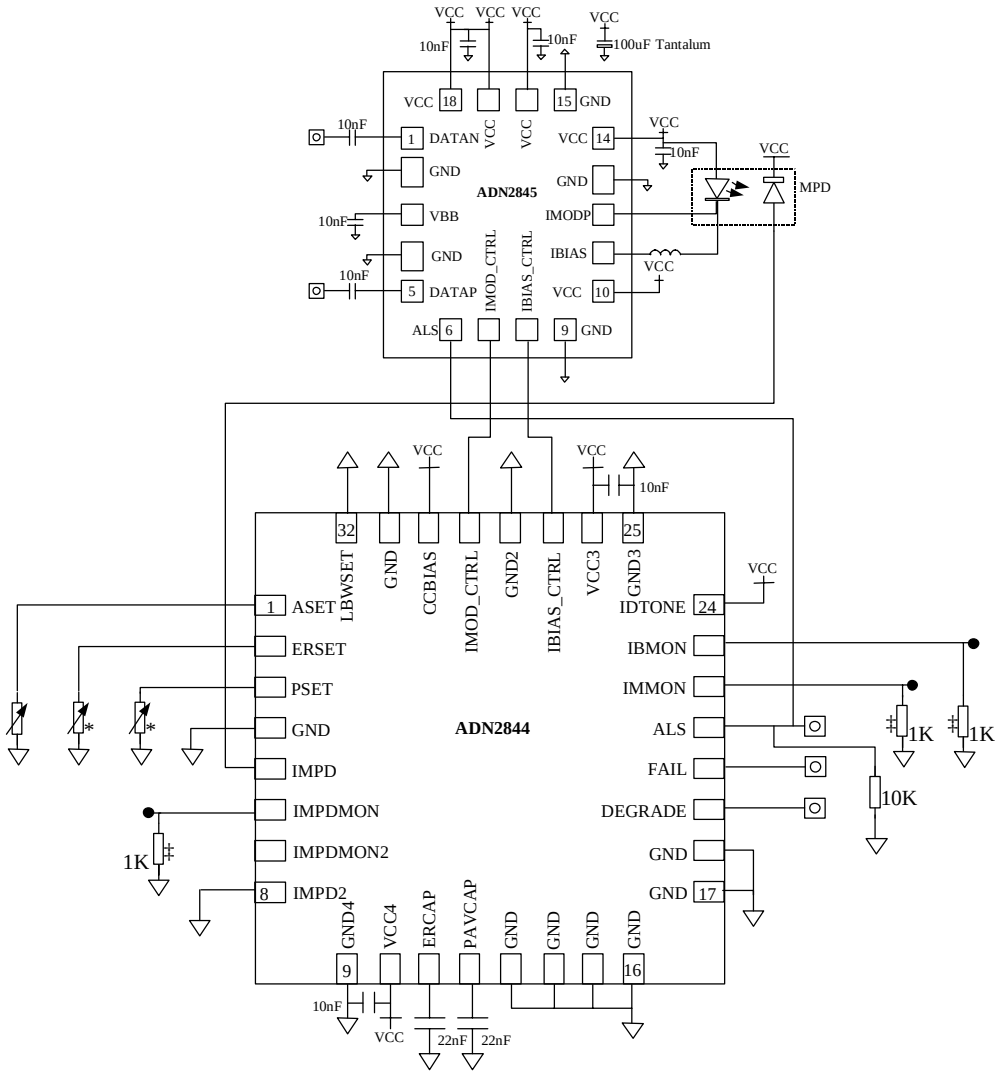
Pin	ADN2845	FUNCTION
1	DATAN	AC Coupled CML Data, negative differential terminal
2	GND	Negative Supply
3	VBB	CML Data termination voltage output.
4	GND	Negative Supply
5	DATAP	AC Coupled CML Data, positive differential terminal
6	ALS	Automatic Laser Shutdown Logic Input
7	IMOD_CTRL	Modulation current control input (Control circuit sinks IMOD/10 from pin to GND)
8	IBIAS_CTRL	Bias current control input (Control circuit sinks IBIAS/10 from pin to GND)
9	GND	Negative Supply
10	VCC	Positive supply.
11	IBIAS	Bias current
12	IMODP	Modulation current
13	GND	Negative Supply
14	VCC	VCC connection for IMODN termination resistor
15	GND	Negative Supply
16	VCC	Positive supply
17	VCC	Positive supply
18	VCC	Positive supply

PACKAGE OUTLINE

Both the ADN2844 and the ADN2845 are available as bare die.
The ADN2844 is also available in 5mm x 5mm 32 pin LFCSP.







* For digital programming, the ADN2850 optical supervisor can be used.
‡ Optional monitoring of currents.

ADN2843 application circuit.

- Best high frequency board layout techniques including power and ground planes should be used.
- To minimize inductance, keep the connections between the ADN2845 and the laser diode as short as possible.
- Place bypass capacitor on laser anode as close to laser as possible.
- Minimise bond lengths for ADN2845 pads to achieve low inductance.
- Ribbon bonding can be used to reduce bond inductance.
- Critical bonds are IMODP and VCC(pin14).
- Connecting to AN2845 GND(pin 13) is optional if it allows inductance on VCC(pin 14) to be further reduced.
- Bypass capacitors should be placed as close as possible to VCC pads.
- 50Ω controlled impedance interconnects should be used on the DATA inputs.
- Value of the AC coupling capacitors on the DATA inputs depends on the frequency content of the data.
- Parasitic capacitance on IBIAS_CTRL and IMOD_CTRL interconnects should be less than 100pF. If decoupling caps are used on IBIAS_CTRL and IMOD_CTRL, they should be to VCC rather than GND.